Design and Optimisation of Large 4T Pixel

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Abstract – Image lag and slow charge transfer are the key challenges to be overcome for large 4T pixels. This paper presents several designs of 50μm pixels that have been manufactured using X-FAB's 0.18μm CIS process. The measured results of image lag are compared. The best design has an image lag <1/500th of the conventional rectangular shaped pinned photo diode. Compared to other published solutions, the best design is more easily scalable to larger sizes and requires no extra processing steps, above those of a standard CIS process.

I. Introduction

Many scientific, medical and industrial CMOS image sensor (CIS) applications require larger sized pixels, ranging between 10μm to 200μm [1, 2]. Many still use three transistor (3T) pixels. As an alternative, four transistor (4T) pixels are increasingly adopted, owing to the many benefits they can offer, such as lower noise and dark current.

Using 4T pinned photo diode (PPD) pixels, one of the major advantages is that the presence of the transfer gate device helps to enable the correlated double sampling (CDS) to eliminate reset noise. However, compared to 3T pixels, their use can worsen image lag, a problem that becomes worse as pixel size increases. Larger pixels also face slower charge transfers [3]. To solve these problems several methods have been investigated, such as in [4, 5, 6] for 6μm - 12μm pixels and [7] for 40μm pixels. These investigations resulted in extra implant steps being required or difficulties in scaling to larger sizes.

In this paper, several pixel designs for 50μm 4T CIS pixel are discussed (Fig. 1), their image lag results compared and the most promising designs identified.

II. Image Lag and Solution

It is known that if there is a potential barrier or well between the PPD and the floating diffusion (FD) region, it will cause image lag [3, 5]. This is true for either small or large pixels. Thus the PPD and transfer gate (TG) layout design and process optimization, to eliminate this potential barrier or well, is essential for a lag free 4T pixel. However, even if process and transfer gate design is optimized for smaller pixels, it is still possible for a potential barrier to arise for larger ones using the same conditions, due to the absence of the fringe field influence that is present for smaller pixels. Fig. 2 shows the maximum potential from PPD to FD for a smaller pixel of 3.6μm and a bigger pixel of 20μm. Thus a process optimised for smaller pixels may not be optimal for larger pixels.

Another source of image lag is directly related to the charge transfer speed. Large pixels have a "flat" potential in the PPD, where charge transfer is dominated by the diffusion process [3].

Consequently, to reduce the image lag, two methods can be employed. One is to create extra electrical field in the direction of the charge transfer. The other is to reduce the electron diffusion distance of a PPD. These two methods can be used separately or combined. Published works so far seem to have focused mainly on the first method.

III. 4T Pixel Design

Based on the principles of the two methods mentioned, first of all, the process and layout were optimised to ensure the elimination of the potential barrier or well. Then, several pixel designs have been carried out. They either aim to create extra electrical field in the direction of the charge transfer and / or reduce the electron diffusion distance of a PPD.

In this paper, as shown in Fig.1 and listed in Table I, several types of pixel designs will be discussed.

In (a), a 4T pixel with a conventional square shaped PPD with TG on one side is shown. It is used as the reference.

In (b), a 4T pixel with a U-shaped TG gate [6] is shown. Compared with the pixel design in (a), the U-shaped TG will reduce the electron diffusion distance in the PPD. It offers smaller FD capacitance, thus larger conversion gain. It also has less shallow trench isolation (STI) edge, thus lower dark current for FD. Two different FD sizes have been evaluated.

In (c), 4T pixels with tapered multi-finger PPD are shown. The tapered fingers utilise the narrow width effect to create the extra electrical field in the direction of the charge transfer. Its working principle is similar to the W-shaped PPD [5], but is considered better for bigger pixels.

In (d), the tapered fingers are placed in alternating directions. This way, larger total area of PPD NWELL can be placed. The TG and FD are connected to form a single TG and FD nodes, respectively. As a more complex design, it is not so desirable.

In (e), by placing the TG in the middle of the PPD, the electron diffusion distance is reduces. Additionally, it has less STI edge for the FD, and so is a further improvement to (c).

In (f), a 4T pixel with varying pinning voltage PPD and a central TG is shown. A 4T pixel with centre TG has been used in radiation hardness pixel of 11.25μm [8]. It has the advantages of both reduced electron diffusion distance and less STI edge for the FD. However, for bigger pixels, varying the pinning voltage to create the extra electrical field is necessary. In [4] the junction depth of the PPD NW is varied. In [7] the PPD NW doping is varied. The pinning layer junction depth is varied here. PPD with two different sizes of FD were evaluated. Also a PPD without the varying pinning voltage (f1) was checked for reference.

In (g), a 4T pixel with Multi-TG is shown. The TG and FD are connected to form a single TG and FD nodes, respectively. Two variations exist, with and without PWELL between the TG. 10μm and 25μm pitches of TG were checked as well. Compared to binning, this is simpler for circuit design. It also allows the pixel to scale up to bigger sizes without having to re-optimize the process.

A hybrid of pixel (e) and (f1), i.e. tapered multi-fingers PPD arranged in a circle around a central TG, could also offer good image lag. However, this has not been tested to be presented in this paper.

All the trial pixel designs shared the same design of reset device, source follower and row select device. Some effort was also spent trying to have the same total FD capacitance through the use of extra MIM (metal insulator metal) capacitor.

IV. Measurement and Results

Wafer level testing was performed for pixel evaluation. Each of the 50μm pixel variants were arranged in a 3x3 array, connected in a way that only the middle pixel was active.

A current mirror was connected to the middle pixel's output node, allowing a reference current to be forced. As the test was carried out at wafer level, very fast screening of the most promising pixels was possible.

Fig. 3 shows the image lag test timing diagram. Pre-conditioning was applied at first, with 10 frames in the dark to ensure the pixels' PPD were empty before the data record commence. After that, output signal was read for 3 frames in dark. The LED light was then switched on and off. The light level and duration were chosen so that the output level was at ~50% of the pixel's saturation level. Over the next 7 frames the output signal was recorded. Fig. 4 shows the measured image lag with a transfer time of 60ns. Fig. 5 shows the image lag at frame 1 for each pixel with transfer time of 60ns, 100ns and 1μs, respectively.

It is clear from Fig. 4 and Fig. 5 that for the U-shaped TG 50μm pixels (b1) and (b2), their image lag have not improved compared to the conventional squared shaped PPD pixel (a). In fact, the variant with smaller FD, (b1) has worst image lag. We hypothesize this is due to the narrower channel width of the TG device.

For the tapered multi-figured PPD variants, the best improvement was found to be pixel (e). At 60ns t_{TG} (TG ON time), its lag is <0.9%, $1/70^{th}$ of pixel (a); at 100ns t_{TG}, its lag is <0.1%, $<1/500^{th}$ of pixel (a). The other two variants, (c) and (d), also showed significant improvement over pixel (a). At 1μs t_{TG}, their lags are 1.4% and 1.9% respectively, $1/75^{th}$ and $1/50^{th}$ of the pixel (a).

Pixel (f1) has the TG in the centre of the PPD, without varying pinning voltage. Its image lag for all 3 t_{TG} showed limited improved of around 10% compared to pixel (a). The variants (f2) and (f3) with varying pinning voltage showed greater improvement. Pixel (f3) has a bigger FD, resulting in a wider TG width and also shorter electron diffusion distance, so demonstrated lower lag than pixel (f2) at 60ns and 100ns t_{TG}. Both (f2) and (f3) lags at 1μs are <0.1%, $1/150^{th}$ of pixel (a).

For multi-TG pixel (g1) and (g2) with 25μm TG pitch, pixel (g2) with PWELL stripe between the TG has lower lag than (g1) at 60ns and 100ns t_{TG}. At 1μs t_{TG}, lags for both are about 0.1%.

For multi-TG pixel (g3) and (g4) with 10μm TG pitch, both without and with PWELL stripe have similar image lag of around 0.1% for all three t_{TG}. It is $<1/500^{th}$ of pixel (a) at 60ns and 100ns t_{TG}.

In summary, multi-TG pixels (g3) and (g4) have good image lag for all three t_{TG} of 60ns, 100ns and 1µs.

For t_{TG} of >=100ns, the tapered multi-figured PPD pixel (e) is also a good candidate.

For t_{TG} of >=1µs, another tapered multi-figured PPD pixel (c) is possible. So are the central TG with varying pinning voltage pixel (f2) and (f3), as well as the multi-TG pixels (g1) and (g2) are also options.

V. Conclusion

In this paper, we have presented several pixel designs which create extra electrical field in the direction of the charge transfer and/or reduce the electron diffusion distance of a PPD. Measured image lag results for 50µm sized pixels were compared. The best design has an image lag <1/500th of the conventional rectangular shaped pinned photo diode. It is also easily scalable to larger sizes and requires no extra processing steps, above those of a standard CIS process.

Acknowledgement

The authors would like to acknowledge Alexander Rolapp of IMMS for carrying out the measurements.

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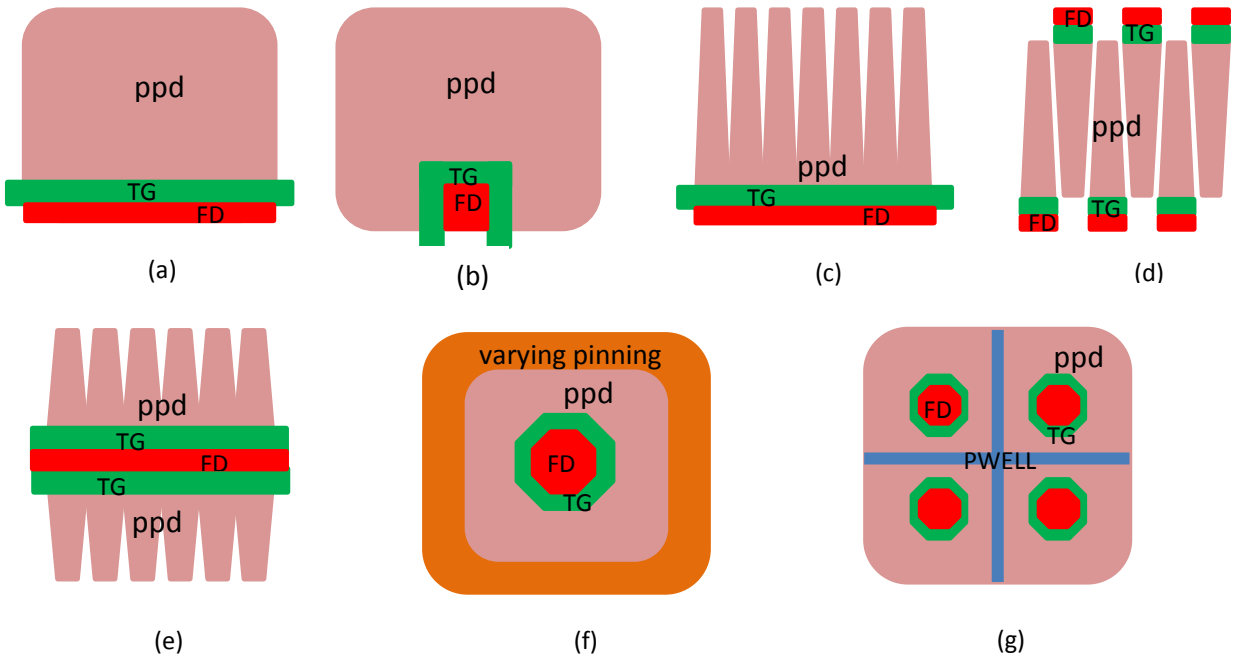

Figure 1 Diagram of the different pixel designs

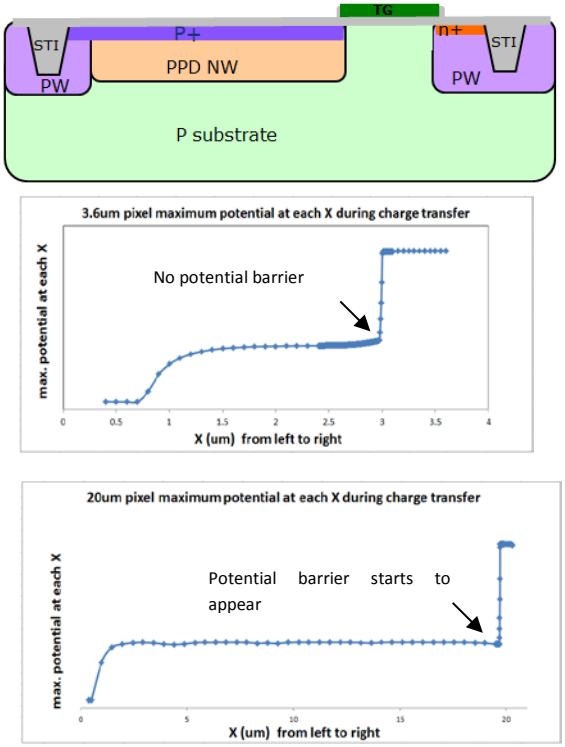

Fig. 2 Schematic of PPD structure, with maximum potential from TCAD, left to right of a 3.6μm and 20μm

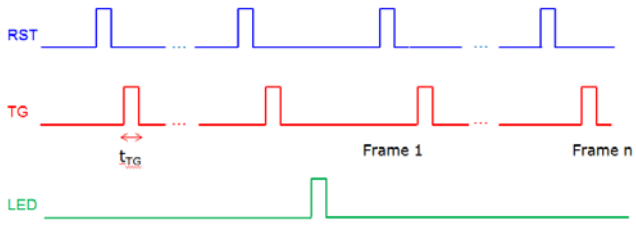

Fig. 3 Image lag test timing diagram

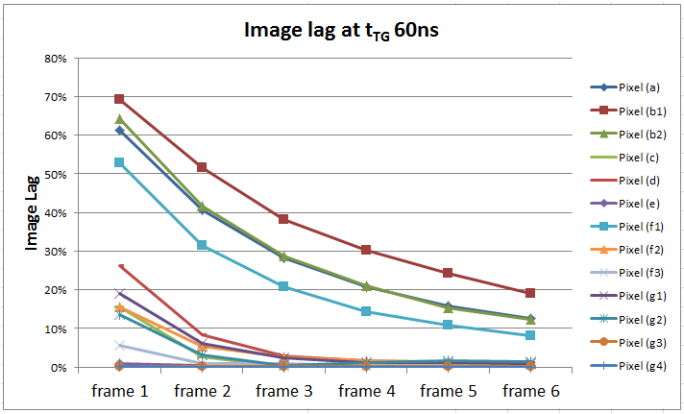

Fig. 4 Image lag test results

Pixel (a)	Fig. 1 (a)	Square shaped conventional PPD	reference pixel
Pixel (b1)	Fig. 1 (b)	U-shaped TG PPD	FD 4.8x4.8 um2
Pixel (b2)	Fig. 1 (b)	U-shaped TG PPD	FD 9.6x9.6 um2
Pixel (c)	Fig. 1 (c)	tapered multi-finger PPD	-
Pixel (d)	Fig. 1 (d)	tapered multi-finger PPD	taper in alternating direction
Pixel (e)	Fig. 1 (e)	tapered multi-finger PPD	PPD in two halves, FD in the middle
Pixel (f1)	Fig. 1 (f)	Central TG PPD, without varying pinning voltage	FD 4.8x4.8 um2
Pixel (f2)	Fig. 1 (f)	Central TG with varying pinning voltage PPD	FD 0.96x0.96 um2
Pixel (f3)	Fig. 1 (f)	Central TG with varying pinning voltage PPD	FD 4.8x4.8 um2
Pixel (g1)	Fig. 1 (g)	Multi-TG PPD	without PW, TG pitch 25um
Pixel (g2)	Fig. 1 (g)	Multi-TG PPD	with PW, TG pitch 25um
Pixel (g3)	Fig. 1 (g)	Multi-TG PPD	without PW, TG pitch 10um
Pixel (g4)	Fig. 1 (g)	Multi-TG PPD	with PW, TG pitch 10um

Table I.
List of Pixels

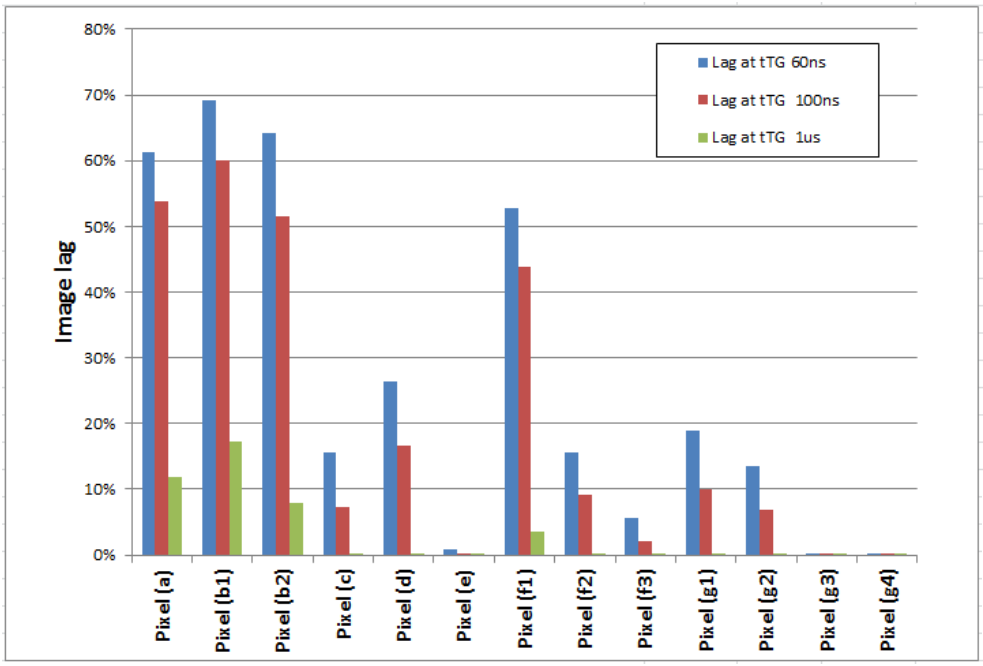

Fig. 5
Image lag test results at frame 1