Panel

Mixed Signals on Mixed-Signal: the Right Next Technology

Chair: Rob A. Rutenbar, Carnegie Mellon University

Organizers: James Spoto & Rob A. Rutenbar

Panelists: David Harame, IBM Corp., Kurt Johnson, Cadence Design Systems, Paul Kempf, Jazz Semiconductor, Teresa Meng, Stanford Univ./Atheros Communications, Reza Rofougaran, Broadcom, James Spoto, Applied Wave Research

Abstract

CMOS dominates digital microelectronics. However, wireless applications require RF circuits at 1-5GHz, and exotic higher frequency applications are on the horizon. Silicon-Germanium (SiGe) is a growing choice for these designs. But is it "the" answer? Some argue that scaled CMOS will handle all tomorrow's RF ICs. Others argue that one-chip SoC solutions will never be the winning strategy for these highly heterogeneous designs, and place their bets on system-in-package (SiP) technologies. Is there a right answer here? Is CMOS the "only" way, or just "another" way?

Position Statements

Kurt Johnson

Cadence Design Systems, San Jose, CA

The CMOS vs. SiGe and system in package debate rages on. To evaluate any integration approach, one must consider not only the technical challenges in all proposed approaches across multiple applications, but also the business aspects, time to market, and risk associated with each approach. Questions such as "what are my costs to iterate a single chip solution?", "what is the time to market estimate?", and "what is the best way to respond to my customer's needs?" need to be evaluated.

From an EDA perspective, it is important for the industry to enable both approaches; in fact the EDA industry benefits by diverse approaches to problems. With so many variables to consider, and intense competition amongst suppliers, differentiation is key. CMOS may evolve one day as the dominant technology, however SiGe is evolving as well, and so are the applications that these technologies support, making CMOS "another" way. When and if these factors align to produce a truly dominant approach is anyone's guess, until then we need to support and gain the most from each of these approaches discussed.

Paul Kempf

Jazz Semiconductor, Newport Beach, CA

The growth of end-market applications that require devices optimized for RF and high-speed electronic functions has created demand for technologies that have been, to date, dominated by captive suppliers. Historically high prices and significant entrance barriers for SiGe BiCMOS have created the common view that CMOS is the cheapest solution. This situation has led to the mantra: "Do it in CMOS," disregarding important factors related to inefficient implementation of RF circuits, limitations of analog performance, and yield loss resulting from integration of RF functions with digital logic. As SiGe availability improves through foundries, many of the perceived advantages of CMOS disappear. Optimization of process modules in SiGe BiCMOS is improving the performance and functional density for analog and mixed-signal products. This provides designers with a path to achieve lower cost solutions, much the same way CMOS scaling has continued to provide generations of functional density improvement for digital devices.

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Teresa Meng

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As technology scaling continues, analog components are beginning to take up a disproportionate amount of silicon area. As a result, the yield of a chip, and therefore its cost, highly depends on the tolerance of the analog circuitry to processing variations. A solution to reduce these manufacturing costs is to exploit the capability of digital circuitry to compensate for the ever more tenuous or imprecise realization of analog circuits. Such a design strategy requires an increasing amount of digital circuitry on the analog chip, which requires CMOS mixed-signal integration.

Another major drawback of multi-chip solutions is the noise and area penalty due to large numbers of I/O pins if the analog and digital circuitry is separated. As long as integration is feasible, eliminating unnecessary pin count and off-chip communication significantly improves the power and noise performance. Therefore the question is not whether CMOS is the chosen technology for mixed-signal design, but rather can any non-CMOS pure-analog design ever survive in the future under the dual pressures of cost reduction and technology scaling?

Reza Rofougaran

Broadcom, El Segundo, CA

Over the past few years there have been tremendous achievements in development of full system_on-chip products in standard logic CMOS technology. Products include radios and single-chip solutions for Bluetooth, Wireless LAN, GSM and GPRS from

Broadcom, silicon labs and other companies. CMOS does offer a lower cost solution with the highest level of integration.

System-on-chip product's success is mainly due to two factors, CMOS process maturity and improved EDA tools. Long term research and development in CMOS process, originally developed for digital IC design, has advanced the process for analog and RF IC designs. CMOS has also been improved for the integration of all digital/RF and analog blocks. By integrating the baseband with the radio on one chip, new approaches to adaptive transceiver calibration can be applied that compensate for the deficiencies of CMOS. These adaptive architectures would be very difficult or impossible to accomplish in hybrid approaches.

EDA tools have also been a big factor on the success of SOC in the past few years. The tools have improved and are more capable of simulating and modeling of high frequency blocks as well as their integration with digital blocks on the same chip. Although, not fully optimized yet for simulating the substrate noise coupling on the silicon, the tools have advanced enough to provide first level information of how all the blocks can work on the same chip. A combination of CMOS process maturity, new adaptive radio design techniques and EDA tool advancement has paved the path for many more SOC products today and in the future.

Raminderpal Singh
IBM Corp., Burlington, VT

SiGe leads CMOS for RF transistor performance, and always will. The HBT's are highly linear and very easy to design with, and cheaper than analogous FET's. For example, SiGe is relatively cheap at the 0.18um and 0.25um nodes, when compared to complex, costly, and immature 0.09um and 0.13um CMOS technologies. CMOS continues to challenge SiGe in many of areas of wireless design, especially when the standards are mature allowing for stable integration of the RF sub-system with the digital back-end. However, complex advanced design techniques are often needed to circumvent inherent linearity and noise problems. No wonder that SiGe RF designs are abundant in the marketplace, and that RF solutions in pure CMOS are still emerging. Interestingly, RF-CMOS technologies offer an interesting and tempting balance. These are typically derivatives of their CMOS counterparts, with analog metal back-ends and advanced passives.

The key is for the design team to pick the correct technology based on specific product, schedule, and cost needs - while factoring in the design team's expertise and possible reuse of residual IP. Initially, this may be SiGe, based on time-to-market pressures and the initial lack of digital integration in the product. But, as the product market and CMOS-equivalent technology mature, the cost balance may lean towards RF-CMOS, and then possibly pure CMOS.

James Spoto
Applied Wave Research, El Segundo, CA

The battle for dominance in RF wireless application between integrated RF CMOS and specialty technologies (like SiGe, GaAs, InP,…) will depend upon advances and roadblock created by EDA. Issues such as device model accuracy, simulation capacity, and inadequate layout automation and extraction are limiting RF design effectiveness. Poor integration of electrical and physical design at the system and circuit level is also impeding "RF closure" for all technologies.

Integrating RF CMOS cores into systems-on-chip or SoCs will be complicated by the ability to co-design and verify the electrical and physical implementation of the baseband working with the RF transceiver. Competing product implementations incorporating separate CMOS, SiGe and III/V components have their own set of design challenges driven primarily by mixing multiple technologies, analog and digital signal processing in multi-chip modules or MCMs. A summary of the EDA accelerators and inhibitors to SoC and MCM RF implementation will be presented and debated.