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Authors : Huai WANG*, *Member, IEEE*
Henry Shu-hung CHUNG† (Corresponding author), *Senior Member, IEEE*
Wenchao LIU†

Address : * Center of Reliable Power Electronics (CORPE)
Department of Energy Technology
Aalborg University
Pontoppidanstraede 101, DK-9220 Aalborg
Denmark

† Centre for Smart Energy Conversion and Utilization Research (CSCR)
City University of Hong Kong
Tat Chee Avenue, Kowloon Tong
Kowloon, Hong Kong

Tel. : (852) 3442 7807

Email : eeshc@cityu.edu.hk

Use of a Series Voltage Compensator for Reduction of the DC-Link Capacitance in a Capacitor-Supported System

Huai WANG*, Henry Shu-hung CHUNG† and Wenchao LIU†

Abstract - A technique for reduction of the dc-link capacitance in a capacitor-supported system is presented. The concept is based on connecting a voltage source in series with the dc bus line to compensate the ripple voltage on the dc-link capacitor, so as to make the output have a near zero ripple voltage. Since the voltage compensator processes small ripple voltage on the dc link and reactive power only, it can be implemented with low-voltage devices. The overall required energy storage of the dc-link, formed by a reduced value of dc-link capacitor and the voltage compensator, is reduced, allowing the replacement of popularly used electrolytic capacitors with alternatives of longer lifetime, like power film capacitors, or extending the system lifetime even if there is a significant reduction in the capacitance of electrolytic capacitors due to the aging effect. Comprehensive analysis on the static and dynamic characteristics of the system, and hold-up time requirement will be discussed. The proposed technique is exemplified on an ac-dc-dc power conversion system. Theoretical predictions are favorably verified by experimental results.

Keywords- dc-link capacitor, power conversion system, capacitance reduction, voltage compensator

NOMENCLATURE

C	Dc-link capacitor
C_{DC}	Input capacitor of the voltage compensator
L_f	Output filter inductance of the voltage compensator
C_f	Output filter capacitance of the voltage compensator
v_{ab}	Output voltage of the voltage compensator
V_{ab}	Amplitude of v_{ab}
$V_{ab,rms}$	Root-mean-square value of v_{ab}
v_C	Dc-link voltage
V_C	Dc component of v_C
$v_C(0)$	Voltage of v_C in the event of an input power outage of the front-end converter [$v_C(0) = V_C - \lvert \Delta v_C \rvert$]
Δv_C	Ac component of v_C
$\Delta V_{C,rms}$	Root-mean-square value of Δv_C
$\lvert \Delta v_C \rvert$	Amplitude of Δv_C
v_{con}	Control signal in the control stage of the voltage compensator
V_{con}	Amplitude of v_{con}
v_d	Output voltage of the dc-link module
$V_{d,\min}$	Specified minimum dc-link voltage during the hold-up time period
V_D	Dc component of v_d
$\lvert \Delta v_d \rvert$	Amplitude of the voltage ripple component of v_d
v_{DC}	Input voltage of the voltage compensator

$V_{DC,ref}$	Input voltage reference of the voltage compensator
$v_{DC,\min}$	Minimum value of v_{DC}
$v_{DC}(0)$	Voltage of v_{DC} in the event of an input power outage of the front-end converter [$v_{DC}(0) = v_{DC,ref}$]
$\lvert \Delta v_{DC} \rvert$	Amplitude of the voltage ripple component of v_{DC}
v_{os}	Offset voltage in the control stage of the voltage compensator
V_{os}	Dc component of v_{os}
$\lvert \Delta v_{os} \rvert$	Amplitude of the voltage ripple component of v_{os}
v_{out}	Output voltage of the phase-shifted full-bridge dc-dc converter
v_{tri}	Carrier signal of the PWM of the voltage compensator
V_{tri}	Amplitude of v_{tri}
i_a	Current flowing through the input side of the dc-link capacitor/module bus line
I_A	Dc component of i_a
Δi_a	Ac component of i_a
$\lvert \Delta I_a \rvert$	Amplitude of Δi_a
i_C	Current following through the dc-link capacitor C
$\lvert \Delta I_C \rvert$	Amplitude of i_C
i_{Cf}	Current flowing through C_f
i_d	Current flowing through the output side of the dc-link capacitor/module bus line
$I_{d,rms}$	Root-mean-square value of i_d
I_D	Dc component of i_d

Δi_d	Ac component of i_d
$\lvert \Delta I_d \rvert$	Amplitude of Δi_d
i_{out}	Output current of the phase-shifted full-bridge dc-dc converter
f_{rip}	Frequency of Δv_C
M	Modulation index of ratio V_{con} / V_{tri}
P_{ab}	Average power absorbed by the voltage compensator
S_{ab}	Apparent power handled by the voltage compensator
S_m	Apparent power handled by the main circuit
T	Least common multiple of $2\pi / \omega_1$ and $2\pi / \omega_2$
α	Scaling factor of v_C in the control stage to the PWM controller
β	Ratio between $\lvert \Delta I_C \rvert$ and I_D
γ	Ratio between $v_{DC}(0)$ and $\lvert \Delta v_C \rvert$
δ_1	Phase of Δi_a
δ_2	Phase of Δi_d
λ	Ratio between C and C_{DC}
μ	Ratio between $\lvert \Delta v_C \rvert$ and V_C
ρ	Ratio between $V_{d,\min}$ and V_C
ω	Angular frequency of the capacitor ripple current ($\omega = 2\pi f_{rip}$)
ω_1	Frequency of Δi_a
ω_2	Frequency of Δi_d
N	Number of hold-up cycles with respect to the period of the dc-link voltage ripple with the proposed dc-link module

I. Introduction

A capacitor-supported system consists of multiple power converters interconnected by a dc link. The dc-link voltage is maintained by a capacitor bank that absorbs instantaneous power difference between the input source and output load, minimizing voltage variation on the dc link, and providing sufficient energy during the hold-up time of the system. Among different types of capacitor, aluminum electrolytic capacitors (E-Caps) are the most popular choice because of their high volumetric efficiency and low cost. However, they suffer from the drawbacks of high equivalent series resistance (ESR); low ripple current capability; bottleneck of the voltage rating; relatively short lifetime compared to other components and considerable maintenance work.

Advances in power film capacitor technology are emerging for dc-link filtering [1]-[2]. Power film capacitors outperform aluminum E-Caps in terms of ESR, self-healing capability, life expectancy, environmental performance, dc-blocking capability, ripple current capability and reliability. Although low-voltage and high-value film capacitors are available, the capacitance of the high-voltage film capacitors still cannot compete with E-Caps, due to their relatively low volumetric efficiency and high cost. To lessen the dependency of the dc-link capacitance, there are many prior-art methods, based on the following approaches:

1) *Performance trade-off* - This method allows a larger voltage ripple across the dc-link with a smaller capacitance. However, it is practically less impressive as the system performance will be degraded. It is more suitable for certain applications, like the ones in [3]-[5]. A set of design procedure is given in [6] for the optimization of capacitor bank.

2) *Reduction of the dc-link capacitor current with sophisticated control.* The concept is based on reducing the ripple current flowing through the dc-link capacitor [7]-[12]. The front-stage converter is an active rectifier in [7]-[10], and a step-up dc-dc converter in

[11]-[12], while the output is an inverter. Their key advantage is that no additional circuit is needed. However, those control methods cannot be applied to systems with front-end diode-bridge rectifier. Apart from requiring a sophisticated controller, some of them also rely on specific relationship in the operating frequency between the converters connected [7], [10], and [11]. The method given in [8] is limited to three-phase systems. The controller described in [7] is based on assuming an ideal energy conversion. Thus, the actual input current would be distorted unless multiple cell load inverters are used. The performance of those controllers is greatly dependent on the accuracy of the computations [9], [12] and affected by the overall time delays of the control loops.

3) *Increase in the frequency of the dc-link voltage ripple.* A double frequency front-end converter with multi-phase switching is proposed in [13] to reduce the ripple voltage. However, the approach cannot reduce the dc-link capacitance significantly.

4) *Ripple cancellation circuit with a coupled element.* In [14], a coupled inductor is applied to cancel the voltage ripple of the dc input, dc output or dc-link of a power converter. The concept is based on assuming that the capacitor used in the storage tank is infinite. But, in reality, the capacitance has a finite value, and the coupled inductor filter and the capacitor form a low pass filter. To avoid large-sized coupled windings, the technique is more suitable for filtering high-frequency ripples or noise, such as switching ripple, EMI filtering. Moreover, the dynamic response of the capacitor may be degraded due to the series-connected coupled winding.

Apart from the aforementioned methods, active power filters can also be used for reduction of the dc-link capacitance as presented in [15]-[28]. It is based on connecting an auxiliary circuit in parallel with the dc-link capacitor. The added circuit serves as an active

impedance or energy source. Different methods of implementing the auxiliary circuit are given. In [16], the auxiliary circuit has a single switch with a dissipative resistor. In [20], a relay is placed at the input line and is activated, depending on the dc-link voltage level, resulting in a stable dc-link voltage, but at the expense of reducing the input power factor of the entire system. In [15], [17] and [22], an H-bridge circuit with a current source (inductor) is used to minimize the ripple current of the dc-link capacitor. However, the high inductor current stress and high switching frequency requirement in [22] are the major practical challenges of the method. A current injection method was applied in [18]-[19], [21] and [23] by a half-bridge structure. In [24]-[25], a two-switch converter that can operate bi-directionally in both buck and boost modes is used for the H-bridge front-end and dc current electrical load application. In [26], a series-connected dual boost converter is as the shunt active filter for a three-phase diode rectifier front-end conversion system. In [27], the ripple reduction circuit allows an additional power port for enhancing the dynamic response of the whole system. In [28], a single switch, diode and capacitor circuit is added in parallel with the input capacitor of a microinverter to reduce the overall capacitance requirement. The common challenge of all these methods is that the components used in the auxiliary circuit are under a high voltage stress, which could be as high as the dc-link voltage. Moreover, the impact of the active filters on the hold-up behavior of the dc-link has not been explored in [15]-[28].

This paper presents a module that can reduce the required dc-link capacitance. Its operating principle is based on connecting a series voltage source between the dc-link capacitor and the load. The energy storage in the whole system is reduced, making it possible to replace the high-value E-Caps with low-value high-performance capacitors. The voltage compensator is of low voltage and low power rating, as it only produces low voltage and handles reactive power.

II. Proposed Module for DC-Link Capacitance Reduction

Fig. 1 illustrates the basic concept of the module for reducing the dc-link capacitance. The module is composed of a capacitor *C* and a voltage source v_{ab}. The module is connected between two converters, namely Converter 1 and Converter 2. The capacitor voltage v_C has dc component V_C and ripple voltage Δv_C. The peak-to-peak value and ripple frequency of Δv_C are $2|\Delta v_C|$and, f_{rip} respectively. v_{ab} is connected in series between the capacitor *C*, v_C, and the input of Converter 2, v_d. It generates a voltage counteracting Δv_C with its dc component equal to zero (i.e., $v_{ab} = \Delta v_C$). Thus, v_d has the same dc value as that across *C*, but with a zero ripple voltage in the ideal condition. Such architecture allows a high voltage ripple on *C*, implying that the value of *C* can be made smaller, but at the expense of increasing the magnitude of v_{ab}.

v_{ab} is a dc-ac converter with a full-bridge (FB) circuit and an output filter formed by the inductor L_f and the capacitor C_f. A half-bridge circuit can also be used if the current i_d is unidirectional. The dc side of the FB is connected to a dc voltage source, like a capacitor or a voltage source, with voltage v_{DC}. The gate signals for the switches $S_1 \sim S_4$ in the FB are generated by a PWM modulator. Depending on the type of the dc source used, the control signal v_{con} is obtained by sensing different parameters. There are two possible configurations. The first one utilizes a capacitor for the dc source while the second one has an external supply connected to it. Since the first configuration gives a simpler solution, it will be studied in this paper.

Fig. 2 shows the control mechanism. The dc-link voltage v_C and the input voltage of the voltage compensator v_{DC} are sensed. The scaling factor α, as will be shown later, is equal to the ratio between V_{tri} and $V_{DC,ref}$. The difference between $V_{DC,ref}$ and v_{DC} is averaged by a low-pass

filter $F(s)$ and processed by a PI controller $G(s)$ to give an offset voltage v_{os}. The control signal v_{con} is derived by combining $\alpha\, v_C$ with v_{os}. The dc component of $\alpha\, v_C$ is ideally cancelled in v_{con} by v_{os} as $V_{os} = -\alpha V_C$, where V_{os} and V_C are the dc component of v_{os} and v_C, respectively. With such arrangement, it is unnecessary to use a high-pass filter to extract the ac component of v_C. At the same, the dc component of v_{ab} can be eliminated so that the added voltage source only handles ac component. During steady-state operation, v_{con} equals the conditioned ac component of $\alpha\, v_C$. It is then used to compare with the triangular carrier waveform in the PWM modulator to generate the voltage v_{ab} having the same phase and amplitude of Δv_C. Without any external supply, the power consumed by the module (i.e. power losses) is obtained from the ac side of the bridge, that is, Converter 1. Practically, instead of a pure ac voltage, v_{ab} and thus v_{con} have a small dc component.

A dc analysis of the circuit shown in Fig. 1 gives

$$V_D = V_C \tag{1}$$

$$I_D = I_A \tag{2}$$

Δi_a and Δi_d are expressed as

$$\Delta i_a(t) = |\Delta I_a| \sin(\omega_1 t + \delta_1) \tag{3}$$

$$\Delta i_d(t) = |\Delta I_d| \sin(\omega_2 t + \delta_2) \tag{4}$$

Δi_a and Δi_d can be of any periodic form with multiple frequency components. Without loss of generality, only sinusoidal components of frequencies ω_1 and ω_2 are considered for Δi_a and Δi_d, respectively. Δv_C and v_{ab} can be expressed as

$$
\begin{aligned}
v_{ab}(t) = \Delta v_C(t) &= \frac{1}{C}\int [i_a(t) - i_d(t)]\, dt \\
&= \frac{|\Delta I_a|}{\omega_1 C}\sin(\omega_1 t + \delta_1 - 90^o) - \frac{|\Delta I_d|}{\omega_2 C}\sin(\omega_2 t + \delta_2 - 90^o)
\end{aligned}
\tag{5}
$$

Based on (4) and (5), P_{ab} in a period T is given by

$$
\begin{aligned}
P_{ab} &= \frac{1}{T}\int_0^T v_{ab}(t)\, i_d(t)\, dt \\
&= \frac{|\Delta I_d|\,|\Delta I_a|}{2\,\omega_1 C\, T}\int_0^T \sin[(\omega_1 - \omega_2)\, t + (\delta_1 - \delta_2)]\, dt
\end{aligned}
\tag{6}
$$

The proof of (6) is given in appendix. It can be noted that P_{ab} equals zero except in a special case when $\omega_1 = \omega_2$ and $\delta_1 \neq \delta_2$. Therefore, the voltage compensator ideally handles reactive power only in all of the other cases. For the special case concerned, the dc-link capacitance can be reduced by the synchronization control of the phases δ_1 and δ_2 [10].

The apparent power S_{ab} handled by the voltage compensator is

$$
\begin{aligned}
S_{ab} &= V_{ab,rms}\, I_{d,rms} = \Delta V_{C,rms}\, I_{d,rms} \\
&= \frac{1}{2\,\omega_1 C}\sqrt{[|\Delta I_a|^2 + (\frac{\omega_1}{\omega_2})^2 |\Delta I_d|^2](2{I_D}^2 + |\Delta I_d|^2)}
\end{aligned}
\tag{7}
$$

where $\Delta V_{C,rms}$ is the root-mean-square (RMS) value of Δv_C.

Comparing with the apparent power of the main power conversion system $S_m = V_D\, I_{d,rms} = V_C\, I_{d,rms}$, the ratio between S_{ab} and S_m is

$$
\frac{S_{ab}}{S_m} = \frac{\Delta V_{C,rms}}{V_C}
\tag{8}
$$

As $\Delta V_{C,rms} << V_C$, the apparent power rating of the voltage compensator (i.e., S_{ab}) is much smaller than that of the main system.

The relationship between the steady-state value of V_{ab} and $V_{DC,ref}$ is expressed as

$$\begin{aligned} V_{ab} &= \frac{V_{con}}{V_{tri}} V_{DC,ref} \\ &= \frac{\alpha\,|\,\Delta v_C\,|+|\,\Delta v_{os}\,|}{V_{tri}} V_{DC,ref} \\ &= M\, V_{DC,ref} \end{aligned} \tag{9}$$

where $M = \frac{V_{con}}{V_{tri}} = \frac{\alpha\,|\,\Delta v_C\,|+|\,\Delta v_{os}\,|}{V_{tri}}$ and $|\,\Delta v_{os}\,|$ is the amplitude of the ripple voltage of v_{os}.

Ideally, v_{os} is a dc voltage. Thus, $|\,\Delta v_{os}\,| = 0$. As $V_{ab} = |\,\Delta v_C\,|$,

$$\alpha = \frac{V_{tri}}{V_{DC,ref}} \tag{10}$$

Consider the control mechanism in Fig. 2,

$$\begin{aligned} v_{ab}(t) &= \frac{\alpha\, v_C(t) + v_{os}(t)}{V_{tri}} v_{DC}(t) \\ &= [m_{a1} \sin(\omega_1 t + \delta_1 - 90^o) - m_{a2} \sin(\omega_2 t + \delta_2 - 90^o) + \frac{\alpha\, V_C + v_{os}(t)}{V_{tri}}]\, v_{DC}(t) \end{aligned} \tag{11}$$

where $m_{a1} = \frac{\alpha\,|\,\Delta I_a\,|}{\omega_1\, C\, V_{tri}}$ and $m_{a2} = \frac{\alpha\,|\,\Delta I_d\,|}{\omega_2\, C\, V_{tri}}$.

Fig. 3 shows the waveforms of the dc-link capacitor voltage v_C, modulating signal v_m, carrier signal v_{tri}, and the voltage across C_{DC}, v_{DC}. To study the voltage ripple across C_{DC}, t_0 and t_1 in Fig. 3 are defined as the two time instants when Δv_C is across zero within one period. During the time interval from t_0 to t_1, C_{DC} is being charged by the load current and its voltage increases from minimum to maximum. The introduction of the third term $\left[\alpha\, V_C + v_{os}(t)\right] / V_{tri}$ in (11) is related to the dc component of v_{ab} due to asymmetrical switching or power losses in the voltage compensator in practical operation, which has negligible impact on the steady-state

voltage ripple across C_{DC}. Therefore, it is neglected in the following analysis of the voltage ripple across C_{DC}. Based on Fig. 3 and the SPWM principle discussed in [29], the voltage across C_{DC} between t_0 and t_1 is given by

$$\begin{aligned} v_{DC}(t) &= v_{DC,\min} + \frac{1}{C_{DC}}\int_{t_0}^{t_1}[I_D + |\Delta I_d|\sin(\omega_2 t + \delta_2) - i_{Cf}(t)] \\ &\qquad \times [m_{a1}\sin(\omega_1 t + \delta_1 - 90^o) - m_{a2}\sin(\omega_2 t + \delta_2 - 90^o)]\,dt \qquad (12) \\ &= v_{DC,\min} + \frac{1}{C_{DC}}\left\{\begin{array}{l} I_D\int_{t_0}^{t_1}[m_{a1}\sin(\omega_1 t + \delta_1 - 90^o) - m_{a2}\sin(\omega_2 t + \delta_2 - 90^o)]\,dt \\ + m_{a1}|\Delta I_d|\int_{t_0}^{t}\sin(\omega_1 t + \delta_1 - 90^o)\sin(\omega_2 t + \delta_2)]\,dt \\ + m_{a2}|\Delta I_d|\int_{t_0}^{t}\sin(\omega_2 t + \delta_2)\cos(\omega_2 t + \delta_2)]\,dt \\ -\int_{t_0}^{t_1} i_{Cf}(t)\,[m_{a1}\sin(\omega_1 t + \delta_1 - 90^o) - m_{a2}\sin(\omega_2 t + \delta_2 - 90^o)]\,dt \end{array}\right\} \end{aligned}$$

From t_0 to t_1, the net charge of the filter capacitor C_f by i_{Cf} is zero, therefore, when $\omega_1 \neq \omega_2$, the voltage ripple on C_{DC}, $2|\Delta v_{DC}|$, is given by

$$\begin{aligned} 2|\Delta v_{DC}| &= \frac{1}{C_{DC}}\{I_D\int_{t_0}^{t_1}[m_{a1}\sin(\omega_1 t + \delta_1 - 90^o) - m_{a2}\sin(\omega_2 t + \delta_2 - 90^o]\,dt\} \\ &= -\frac{m_{a1} I_D}{\omega_1 C_{DC}}[\sin(\omega_1 t_1 + \delta_1) - \sin(\omega_1 t_0 + \delta_1)] + \frac{m_{a2} I_D}{\omega_2 C_{DC}}[\sin(\omega_2 t_1 + \delta_2) - \sin(\omega_2 t_0 + \delta_2)] \end{aligned} \qquad (13)$$

For practical applications when $\omega_1 << \omega_2$, the effect of the second terms of (5) and (13) are negligible, and $\sin(\omega_1 t_1 + \delta_1) = -1$, $\sin(\omega_1 t_0 + \delta_1) = 1$. Therefore,

$$2|\Delta v_{DC}| = \frac{2\, m_{a1} I_D}{\omega_1 C_{DC}} \qquad (14)$$

The above equation is also applicable for the case when ω_2 is even multiples of ω_1 as $\sin(\omega_2 t_1 + \delta_2) = \sin(\omega_2 t_0 + \delta_2)$. The voltage across C_{DC} is therefore presented by

$$v_{DC}(t) = V_{DC} + \frac{m_{a1}\, I_D}{\omega_1\, C_{DC}} \sin(\omega_1\, t + \delta_1) \tag{15}$$

The output voltage of the voltage compensator v_{ab} is

$$\begin{aligned} v_{ab}(t) &= [V_{DC} + \frac{m_{a1}\, I_D}{\omega_1\, C_{DC}} \sin(\omega_1 t + \delta_1)][m_{a1} \sin(\omega_1 t + \delta_1 - 90^o) - m_{a2} \sin(\omega_2 t + \delta_2 - 90^o] \\ &\approx V_{DC}[m_{a1} \sin(\omega_1 t + \delta_1 - 90^o) - m_{a2} \sin(\omega_2 t + \delta_2 - 90^o] - \frac{{m_{a1}}^2\, I_D}{2\,\omega_1\, C_{DC}} \sin(2\omega_1 t + 2\delta_1) \end{aligned} \tag{16}$$

The first term of (16) is used to cancel the dc-link voltage ripple while the second term is a double frequency ripple, generating voltage variation on v_d. Thus, the voltage ripple of v_d is

$$2\,|\,\Delta v_d\,| = \frac{{m_{a1}}^2\, I_D}{\omega_1\, C_{DC}} \tag{17}$$

III. Hold-up Time Analysis of the DC-Link Module

The hold-up time of the system with and without the proposed module are compared in the following. After a loss of the input power, the energy stored in the dc-link module (i.e., the dc-link capacitor and the capacitor connected to the dc source) will be solely delivered to the load. In the following analysis, the hold-up time t_h is defined as the time duration between the start of the supply outage (i.e., $i_a = 0$) and the voltage v_d reduces to the minimum dc bus voltage $V_{d,\min}$. Fig. 4 (a) shows the timing diagram of two consecutive hold-up intervals distinguished by value of the modulation index *M* of the PWM modulator in Fig. 1. Figs. 4(b) and 4(c) show the equivalent circuits of the two intervals $[0, t_{h1}]$ and $[t_{h1}, t_{h2}]$, respectively. For the sake of simplicity in the analysis, the power loss of the voltage compensator is neglected and the dc-link module is connected to a constant power load P_L.

1. Initial state (t = 0):

Consider the worst case scenario. The voltage across the dc-link capacitor at the supply outage time (i.e., $t = 0$) is $v_C(0) = V_C - |\Delta v_C|$. The voltage across C_{DC}, $v_{DC}(0)$, equals $V_{DC,ref}$. The voltage ripple across the dc-link capacitor is fully compensated by v_{ab}, implying

$$v_{ab}(0) = |\Delta v_C| = M\ v_{DC}(0) \tag{18}$$

where $M = \dfrac{\alpha\,|\Delta v_C(0)|}{V_{tri}}$.

2. Stage I [0, t_{h1}] - $M \le 1$

t_{h1} is the time instant at which $M = 1$. Thus,

$$\frac{\alpha\,\Delta v_C(t_{h1})}{V_{tri}} = 1 \tag{19}$$

$$v_{ab}(t_{h1}) = \Delta v_C(t_{h1}) = -v_{DC}(t_{h1}) \tag{20}$$

Based on (18)-(20),

$$\Delta v_C(t_{h1}) = v_{DC}(0) \tag{21}$$

$$\begin{aligned} v_d(t_{h1}) &= V_C - \Delta v_C(t_{h1}) - v_{ab}(t_{h1}) \\ &= V_C - v_{DC}(0) + v_{DC}(t_{h1}) \end{aligned} \tag{22}$$

In this stage, the variation of v_d is small. Thus, the current i_d is assumed to be constant and is equal to I_D. Thus,

$$\Delta v_C(t_{h1}) = |\Delta v_C| + \frac{I_D}{C}\,t_{h1} = v_{DC}(0) \tag{23}$$

and

$$t_{h1} = \frac{C}{I_D}[v_{DC}(0) - |\Delta v_C|] = \frac{\beta}{\omega}(\gamma - 1) \tag{24}$$

By applying the conservation of energy between the energy delivery from the whole dc-

link module and the load consumption,

$$\frac{1}{2}C\, v_C^2(0) + \frac{1}{2}\, C_{DC} v_{DC}^2(0) - \frac{1}{2}\, C\, v_C^2(t_{h1}) - \frac{1}{2}\, C_{DC}\, v_{DC}^2(t_{h1}) = P_L\, t_{h1} \tag{25}$$

Based on (25),

$$v_{DC}(t_{h1}) = \mu \sqrt{\gamma^2 - \lambda\,(\gamma^2 - 1)}\, V_C \tag{26}$$

By substituting (26) into (22),

$$\begin{aligned} v_d(t_{h1}) &= V_C + \mu \sqrt{\lambda + (1-\lambda)\,\gamma^2}\, V_C - v_{DC}(0) \\ &= [1 + \mu\sqrt{\gamma^2 - \lambda\,(\gamma^2 - 1)} - \mu\gamma]\, V_C \end{aligned} \tag{27}$$

3. Stage II [t_{h1}, t_{h2}]

In this stage, the capacitors C and C_{DC} are connected in series. At t_{h2}, the output voltage $v_d(t_{h2}) = V_{d,\min} = \rho\, V_C$. The final voltages across C and C_{DC} can be expressed as

$$\begin{aligned} \Delta v_C(t_{h2}) &= \Delta v_C(t_{h1}) + \frac{C_a}{C_a + C}[v_d(t_{h1}) - v_d(t_{h2})] \\ &= \Delta v_C(t_{h1}) + \Delta x\, V_C \end{aligned} \tag{28}$$

$$\begin{aligned} v_{DC}(t_{h2}) &= v_{DC}(t_{h1}) - \frac{C}{C_a + C}[v_d(t_{h1}) - v_d(t_{h2})] \\ &= \Delta v_C(t_{h1}) - \lambda \Delta x\, V_C \end{aligned} \tag{29}$$

where $\Delta x = \dfrac{1}{1+\lambda}\,\{(1-\rho) - \mu\,[\gamma - \sqrt{\gamma^2 - \lambda(\gamma^2 - 1)}]\}$.

By applying the conservation of energy,

$$\frac{1}{2}C\, v_C^2(t_{h1}) + \frac{1}{2}\, C_{DC} v_{DC}^2(t_{h1}) - \frac{1}{2}\, C\, v_C^2(t_{h2}) - \frac{1}{2}\, C_{DC}\, v_{DC}^2(t_{h2}) = P_L\, (t_{h2} - t_{h1}) \tag{30}$$

It can be derived from (30) that

$$t_{h2} - t_{h1} = \frac{\beta}{\omega}\,(\frac{\rho}{\mu}\,\Delta x + \frac{1+\lambda}{2\,\mu}\,\Delta x^2) \tag{31}$$

Based on (24) and (31), the hold-up time t_h and the number of hold-up cycle N are

$$t_h = \frac{\beta}{\omega}\left(\frac{\rho}{\mu}\Delta x + \frac{1+\lambda}{2\mu}\Delta x^2 + \gamma - 1\right) \tag{32}$$

$$N = \frac{\beta}{2\pi}\left(\frac{\rho}{\mu}\Delta x + \frac{1+\lambda}{2\mu}\Delta x^2 + \gamma - 1\right) \tag{33}$$

The hold-up time of the dc-link with only a capacitor bank storing the same amount of energy is derived as follows. Let the corresponding dc-link capacitance required, the hold-up time and hold-up cycle be C', t_h', and N' respectively. Thus, for the same amount of energy stored in C' as with the dc-link module,

$$C' = \frac{C V_C^{\,2} + C_{DC}\, v_{DC}^2(0)}{V_C^{\,2}} = \left(1 + \frac{\gamma^2\,\mu^2}{\lambda}\right) C \tag{34}$$

By assuming that the ripple currents following through the dc-link capacitors with and without the voltage compensator are the same,

$$\mu' = \frac{\Delta v_C'}{V_C} = \frac{\beta\, I_D}{\omega\, C' V_C} \tag{35}$$

Hence, by using (34) and (35),

$$\begin{aligned} t_h' &= \frac{C'[V_C - \Delta v_C(0)]^2 - C'(\rho V_C)^2}{2\,P_L} \\ &= \frac{\beta}{\omega}\,\frac{(\lambda + \gamma^2\,\mu^2)\left[\left(1 - \frac{\lambda\mu}{\lambda + \gamma^2\,\mu^2}\right)^2 - \rho^2\right]}{2\,\lambda\,\mu} \end{aligned} \tag{36}$$

$$N' = \frac{\beta}{2\pi}\,\frac{(\lambda + \gamma^2\,\mu^2)\left[\left(1 - \frac{\lambda\mu}{\lambda + \gamma^2\,\mu^2}\right)^2 - \rho^2\right]}{2\,\lambda\,\mu} \tag{37}$$

Equations (32), (33), (36) and (37) will be used to compare the hold-up time with and without the proposed dc-link module. The design guidelines will be given in the next section.

IV. Design Guidelines for the DC-link Module

The design guidelines for applications with and without hold-up time requirements are given below.

A. Applications without hold-up time requirement

Some applications, like electronic ballasts, do not have the hold-up time requirement. The dc-link module is used to balance the input and output power difference, and reduce the dc-link voltage ripple. Fig. 5 shows the energy storage E and instantaneous power p of the dc-link capacitor. The dc component of energy E_1 maintains a certain level of dc-link voltage. Only the ac component of E requires the power p for balancing the input and output power of the entire system. Therefore, with the proposed dc-link module, the energy storage elements are divided into two parts: one is stored in the reduced dc-link capacitor and the other one is stored in the voltage compensator. The theoretical minimum energy storage required is $E_{\min}$. In the practical design, the overall energy storage of the dc-link module is reduced to a certain level between E_1 and $E_{\min}$, for example E_2 as illustrated in Fig. 5.

The reduction of the dc-link capacitance is limited by the voltage stresses on the dc source capacitor and switching devices in the module. Assume that the load current i_d is constant in the module. Based on (5), the dc-link capacitor current i_C equals Δi_a. Thus,

$$i_C = C\frac{dv_C}{dt} = \Delta i_a \Rightarrow C\,|\Delta v_C| = constant \tag{38}$$

The product of the dc-link capacitance and its peak ripple voltage is a constant. Thus, the minimum value of v_{DC} equals $|\Delta v_C|$. Fig. 6 shows the relationship between the value of C and v_{DC}. Without the dc-link module, it requires a capacitance of C_{norm} for meeting the design

specification. Practically, the chosen value for C is larger than C_{norm} in order to sustain the ripple current stress. Due to the aging effect of the capacitor changing from C_{norm} to C_{norm}', the peak-to-peak dc-link voltage ripple will increase from $2|\Delta v_{C,norm}|$ to $2|\Delta v_{C,norm}'|$.

The design of the dc-link capacitance value C with the dc-link module is a compromise among the allowable voltage level of v_{DC}, and the stress on the capacitor C_{DC} and the MOSFETs $S_1 - S_4$. A smaller value of C requires higher voltage ratings of C_{DC} and $S_1 - S_4$. Moreover, a boundary capacitance C_{bd} can be determined based on specifications of power electronic systems, availability, cost and volume of different type of capacitors. It provides a guideline on the selection of capacitor type. For instance, power film capacitors can be applied in *Choice* 1 with a higher dc voltage on C_{DC}, $V_{DC,1}$, as compared to that of *Choice* 2 with lower voltage $V_{DC,2}$ in which E-Caps are used. Thus, with the aid of the dc-link module, the required dc-link capacitance can be reduced, making it possible to use capacitor of long lifetime, like power film capacitors, to ensure the lifetime of the entire power electronic system, or extend the performance lifetime even if there is a significant reduction in the capacitance of the dc-link capacitor due to the aging effect.

The value of C_{DC} is determined by using (17) to limit the voltage ripple of v_d. In the application example (a power factor corrector (PFC) front-end stage plus a dc-dc converter) discussed in Section V, with conventional E-Cap solution (without the voltage compensator),

$$2|\Delta v_C| = \frac{2 I_D}{\omega_1 C_{norm}} \tag{39}$$

According to (17) and (39), as $m_{a1} \le 1$, the voltage ripple across the output terminal of the dc-link module can be limited to lower than the one with conventional E-Cap solution by choosing

C_{DC} no less than half of the capacitance of the E-Cap, that is

$$C_{DC} \geq \frac{1}{2} C_{norm} \tag{40}$$

As the capacitor C_{DC} withstands a low voltage stress, there are several choices in practical implementation. One choice is to use low voltage E-Caps with high ripple current and long lifetime. Unlike the ones with high voltage ratings, they are available and cost-effective. Another choice is to use ceramic capacitor tank or low-voltage film capacitors.

B. Applications with hold-up time requirement

For this type of applications, the determining factor for the energy storage is the required hold-up time rather than the voltage ripple specification. The design guidelines discussed are based on the analysis in Sec. III.

Figs. 7 and 8 show the graphical representations of equations (33) and (37) with $\beta = 1$ (the amplitude of the dc link capacitor ripple current is equal to the value of the average load current), $\rho = 0.8$ ($V_{d,\min}$ is 80% of the dc-link voltage prior to the supply outage), and $\mu = 0.02$ (dc link ripple voltage is 2% of the average dc-link voltage). It should be noted in the comparison that the factors λ and γ are for the proposed dc-link module containing an additional energy storage capacitor C_{DC}. They appear in (37) as the comparison is based on the same energy storage. As depicted in Fig. 7, with proper choices of λ (ratio between C and C_{DC}) and γ (ratio between v_{DC} and $|\Delta v_C|$), the number of hold-up cycles with the dc-link module can be increased. The shaded area of the λ - γ selection curves shown in Fig. 8 represents an extended hold-up time (i.e., $N / N' > 1$). That means, with the same amount of energy storage in the dc link, the hold-up time with the dc-link module is longer than using a dc-link capacitor only.

Different curves showing the constant number of the hold-up cycles and N / N' ratios are plotted in dot lines and solid lines, respectively.

The illustrations given in Fig. 7 and Fig. 8 are with μ = 0.02, which is corresponding to a determined value of the dc-link capacitance *C* from the design perspective. Therefore, the trade-off design condition is between maximization of N / N' and minimization of C_{DC} and its voltage stress v_{DC}, meanwhile, achieving the required hold-up cycle *N*. Different figures can be plotted for other values of μ, corresponding to different values of *C*. By considering all of the values of λ and γ selected for different value of μ, it allows the selection of the optimal values of μ, λ and γ. Thus, the optimal values of C, C_{DC}, and v_{DC} are selected.

V. Experimental Verifications

An experimental ac-dc-dc converter test bed as shown in Fig. 9(a) has been built. It is constructed by connecting a 3kW PFC - STMicroelectronics STEVAL-ISF001V1 to a 600W phase-shifted full-bridge dc-dc converter - Texas Instruments UCC28950EVM-442. An input LC filter composed of 1.47μF film capacitors (1μF and 0.47μF in parallel) and a 20μH inductor is applied to smooth the input current i_d. The detailed circuit and operation of the phase-shifted full-bridge dc-dc converter are discussed in [30] except for that the 330μF input capacitor in the evaluation board is removed in the experiments. The PFC is supplied by an AC power source Kikusui PCR2000LA. The supply voltage is 220V, 50Hz. The output of the dc-dc converter is connected to an electronic load Kikusui PLZ1003W. The rated output voltage of the dc-dc converter is 12V. The output capacitor bank *C* in the PFC is formed by connecting two 330μF, 450V E-Cap capacitors in parallel. According to the manufacturer's datasheet, the lifetime of the

capacitors is 3,000 hours at 105°C (12,000 hours estimated at 85°C and rated ripple current). Figs. 10(a) and (b) show the startup transient and steady-state waveform of v_C when the output is full load. The average dc voltage is 400V and peak-to-peak ac ripple voltage (i.e., Δv_C) is 10.8V. The settling time of the startup process is 150ms. Fig. 10(c) shows the output current i_{out} and v_C when the output is suddenly changed from 10% load to full load. v_C is momentarily dropped by 45V and the settling time is 100ms. Fig. 10(d) shows the corresponding waveforms when the output is suddenly changed from full load to 10% load. v_C is momentarily jumped up by 37.7V and the settling time is 150ms. Fig. 10(e) shows the waveforms of v_C, PFC input voltage v_S and output current i_{out} when v_S is suddenly turned off. v_C reduces to 320V (80% of 400V) after 24.6ms. Within this period, the dc-dc converter is still in normal operation. The measured steady-state RMS value of capacitor current and ESR of the capacitor bank is 1.7A and 130mΩ, respectively. Thus, the total power loss of the capacitor bank is estimated to be 0.38W at full load.

The E-Cap bank is replaced by the proposed module. The circuit schematic of the module is shown in Fig. 9(b). The power stage design of the voltage compensator follows the way to design a typical full-bridge inverter as discussed in [29]. The input voltage level of the voltage compensator is selected according to the dc-link capacitance (as shown in Fig. 6) and the modulation index of the SPWM controller. In the prototype, the modulation index is 0.5 under full load condition to achieve a sufficient robustness margin and avoid over modulation. The dc-link capacitance is 120μF (in the case without hold-up time requirement) with a peak-to-peak voltage ripple of about 50V. Thus, the input voltage v_{DC} is regulated at 50V by setting a 5V reference in the control stage. The switching frequency of the voltage compensator is 50 kHz.

Components used in the power conversion stage and the key design parameters are listed in Table I. Two design cases are investigated. The first design has no hold-up time requirement while the second one has the hold-up requirement. They are discussed as follows.

A. Without hold-up time requirement

A 120μF (82% capacitance reduction) film capacitor with the lifetime of 100,000 hours at 85°C and rated ripple current is used to replace the capacitor bank. A 1000μF, 63V low-voltage E-Cap with the lifetime of 8,000 hours at 125°C (128,000 hours estimated at 85°C and rated ripple current, which is comparable with the lifetime of the film capacitor) is used for the module, i.e. C_{DC}. The voltage across C_{DC} is designed to be 50V. Fig. 11(a) shows the startup transient of the module output v_d. The dc value of v_d is 400V. The settling time of the startup process is 75ms. Fig. 11(b) shows the steady-state waveforms of the capacitor ripple voltage Δv_C and module output ripple voltage Δv_d, when the output is at full load. Their peak-to-peak ripple voltages are 49.1V and 3.9V, respectively. Figs. 11(c) and (d) show the transient waveforms of v_d, v_C, module output voltage v_{ab}, input current of the full-bridge dc-dc converter i_d, output voltage of the dc-dc converter v_{out} and output current of the dc-dc converter i_{out}, when the output is suddenly changed from 10% load to full load. v_d is momentarily reduced by 45.5V and its settling time is 100ms. Figs. 11(e) and (f) show the corresponding waveforms when the output is suddenly changed from full load to no load. v_d is momentarily increased by 37.7V and its settling time is 150ms. Compared Fig. 10(a) with Fig. 11(a), and Fig. 10(b) with Fig. 11(b), the startup time is shorter and the ripple voltage is smaller with the proposed module. As shown in Figs. 10(c) and (d), and Figs. 11(c) and (e), under the load change conditions, the transient

responses of the system with the module are similar to the ones with the E-Cap bank. The total power dissipation of the module is around 1.5W. From the perspective of the capacitor lifetime at 85°C with a same ripple current design margin, the proposed module is estimated to have a lifetime more than eight times of that of the E-Caps without the voltage compensator.

B. With hold-up time requirement

The module is designed to achieve the same hold-up time with the electrolytic capacitors. Based on the design method described in Section IV, a 450μF capacitor (32% capacitance reduction) is used for C and a 1000μF, 63V low-voltage electrolytic capacitors for C_{DC}, corresponding to an overall energy storage of 72% of that with E-Caps solution without the voltage compensator. Fig. 11(g) shows the waveforms of v_d, v_S, v_{ab}, and i_{out} after v_S is suddenly turned off under the full load condition. Compared Fig. 10(e) with Fig. 11(g), the proposed module gives a similar hold-up performance to the electrolytic capacitor bank with 28% energy storage reduction.

Thus, the experimental results reveal that the proposed dc-link module can reduce the required capacitance value for the dc-link capacitor without sacrificing the transient and steady-state responses of the whole system. Although the proposed module requires capacitors as the dc source, the voltage level is only 50V, allowing the use of low-voltage capacitors of long lifetime. The only drawback is that there is an increase in the overall power loss by 1.12W.

From the practical point of view, the use of E-Caps is still the low-cost solution. Then, even if the E-Cap bank is unchanged in the application, the proposed module allows a wide range of reduction in the dc-link capacitance (due to aging effect) without sacrificing the performance. For applications without the hold-up requirement, it allows the reduction of the dc-

link capacitance from 660μF to 120μF in the test. For applications with the hold-up time requirement, the module allows the reduction from 660μF to 450μF and 28% reduction of the overall energy storage in the dc-link module. The resulting effect will extend the life expectancy of the entire system from the perspective of reducing the chance of system failure due to aging of the dc link capacitors. The proposed method has a distinct advantage for high-voltage applications, due to the fact that the voltage rating of power film capacitors is usually higher than that of E-Caps. With the proposed module, the dc-link capacitance can be reduced and a fewer number of high-voltage power film capacitors are used to replace the E-Caps.

VI. Conclusions

An active series voltage compensator for reducing the dc-link capacitance in a capacitor-supported power electronic system has been proposed. The implementation requires low-voltage devices only, as the dc-link module only handles ripple voltage on the dc-link and reactive power flow between in the dc-link. A detailed study on the dc and ac characteristics, stability analysis, and hold-up time performance has been given. The design guidelines for the dc-link module for applications with and without the hold-up time requirement have been described. The proposed method has been demonstrated on a two-converter system with the front-stage power factor corrector and second-stage of dc-dc converter. The performances with the capacitor bank only and the proposed dc-link module have also been compared.

Appendix

A. Proof of Equation (6)

Based on equations (4) and (5), equation (6) is derived as follows:

$$
\begin{aligned}
P_{ab} &= \frac{1}{T}\int_0^T v_{ab}(t)\left[\Delta i_d(t) + I_D\right] dt \\
&= \frac{1}{T}\int_0^T v_{ab}(t)\,\Delta i_d(t)\,dt + 0 \\
&= \frac{1}{T}\int_0^T \left[\frac{|\Delta I_a|}{\omega_1 C}\sin(\omega_1 t + \delta_1 - 90^o) - \frac{|\Delta I_d|}{\omega_2 C}\sin(\omega_2 t + \delta_2 - 90^o)\right] |\Delta I_d| \sin(\omega_2 t + \delta_2)\, dt \\
&= \frac{|\Delta I_d|\,|\Delta I_a|}{2\,\omega_1 C\,T}\int_0^T \left\{\sin[(\omega_1 - \omega_2)t + (\delta_1 - \delta_2)] - \sin[(\omega_1 + \omega_2)t + (\delta_1 + \delta_2)]\right\} dt - 0 \\
&= \frac{|\Delta I_d|\,|\Delta I_a|}{2\,\omega_1 C\,T}\int_0^T \sin[(\omega_1 - \omega_2)t + (\delta_1 - \delta_2)]\, dt - \frac{|\Delta I_d|\,|\Delta I_a|}{2\,\omega_1 C\,T}\int_0^T \sin[(\omega_1 + \omega_2)t + (\delta_1 + \delta_2)]\, dt \\
&= \frac{|\Delta I_d|\,|\Delta I_a|}{2\,\omega_1 C\,T}\int_0^T \sin[(\omega_1 - \omega_2)t + (\delta_1 - \delta_2)]\, dt - 0 \\
&= \frac{|\Delta I_d|\,|\Delta I_a|}{2\,\omega_1 C\,T}\int_0^T \sin[(\omega_1 - \omega_2)t + (\delta_1 - \delta_2)]\, dt
\end{aligned}
$$

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Footnotes

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* The author is with the Center of Reliable Power Electronics (CORPE), Department of Energy Technology, Aalborg University, Pontoppidanstraede 101, DK-9220 Aalborg, Denmark.

† The authors are with the Centre for Smart Energy Conversion and Utilization Research (CSCR), City University of Hong Kong, Tat Chee Avenue, Kowloon Tong, Kowloon, Hong Kong.

Figure captions

Fig. 1 Basic concept of the proposed dc-link module.

Fig. 2 Control mechanism with a capacitor as the input source of the voltage compensator.

Fig. 3 Operation timing diagram of the voltage compensator.

Fig. 4 Operations during the hold-up time. (a) Waveforms. (b) Circuit during the time interval $[0, t_{h1}]$. (c) Circuit during the time interval $[t_{h1}, t_{h2}]$.

Fig. 5 Energy stored and instantaneous power handled by the dc-link capacitor.

Fig. 6 Relationship between the dc-link capacitance, ripple voltage, and v_{DC}.

Fig. 7 Hold-up time analysis with and without the dc-link module ($\beta = 1$, $\rho = 0.8$, $\mu = 0.02$).

Fig. 8 Design curves for selection of λ and γ ($\rho = 0.8$, $\mu = 0.02$).

Fig. 9 Experimental test bed. (a) System configuration. (b) Circuit schematic of the proposed module.

Fig. 10 Experimental waveforms with an electrolytic capacitor bank. (a) Startup transient under the full load condition (v_C: 100V/div, Timebase: 50ms/div). (b) Steady-state dc-link voltage waveform under the full load condition (Δv_C: 2V/div, Timebase: 10ms/div). (c) Transient waveforms when the output is changed from 10% load to full load (v_C: 100V/div, i_{out}: 50A/div, Timebase: 50ms/div). (d) Transient waveforms when the output is changed from full load to 10% load. (v_C: 100V/div, i_{out}: 50A/div, Timebase: 50ms/div). (e) Transient waveforms after a sudden supply outage under the full-load condition. (v_C:100V/div, v_S: 300V/div, i_{out}: 20A/div, Timebase: 10ms/div).

Fig. 11 Experimental waveforms with the proposed dc-link module. (a) Start-up transient under the full load condition. (v_d: 100V/div, Timebase: 50ms/div). (b) Steady-state

waveforms of v_C and v_d under the full load condition (Δv_C: 20V/div, Δv_d: 2V/div, Timebase: 10ms/div). (c) Transient waveforms of the dc-link module when the output is changed from 10% load to full load (v_d: 100V/div, v_C: 100V/div, v_{ab}: 40V/div, i_d: 2A/div, Timebase: 50ms/div). (d) Transient waveforms of the full-bridge dc-dc converter when the output is changed from 10% load to full load (v_d: 100V/div, i_d: 2A/div, v_{out}: 10V/div, i_{out}: 50A/div, Timebase: 50ms/div). (e) Transient waveforms of the dc-link module when the output is changed from full load to 10% load (v_d: 100V/div, v_C: 100V/div, v_{ab}: 40V/div, i_d: 2A/div, Timebase: 50ms/div). (f) Transient waveforms of the full-bridge dc-dc converter when the output is changed from full load to 10% load (v_d: 100V/div, i_d: 2A/div, v_{out}: 10V/div, i_{out}: 50A/div, Timebase: 50ms/div). (g) Transient waveforms after a sudden supply outage under the full-load condition (v_d :100V/div, v_S: 300V/div, v_{ab}: 20V/div, i_{out}: 50A/div, Timebase: 10ms/div).

Table captions

Table I Values of the components used in the module

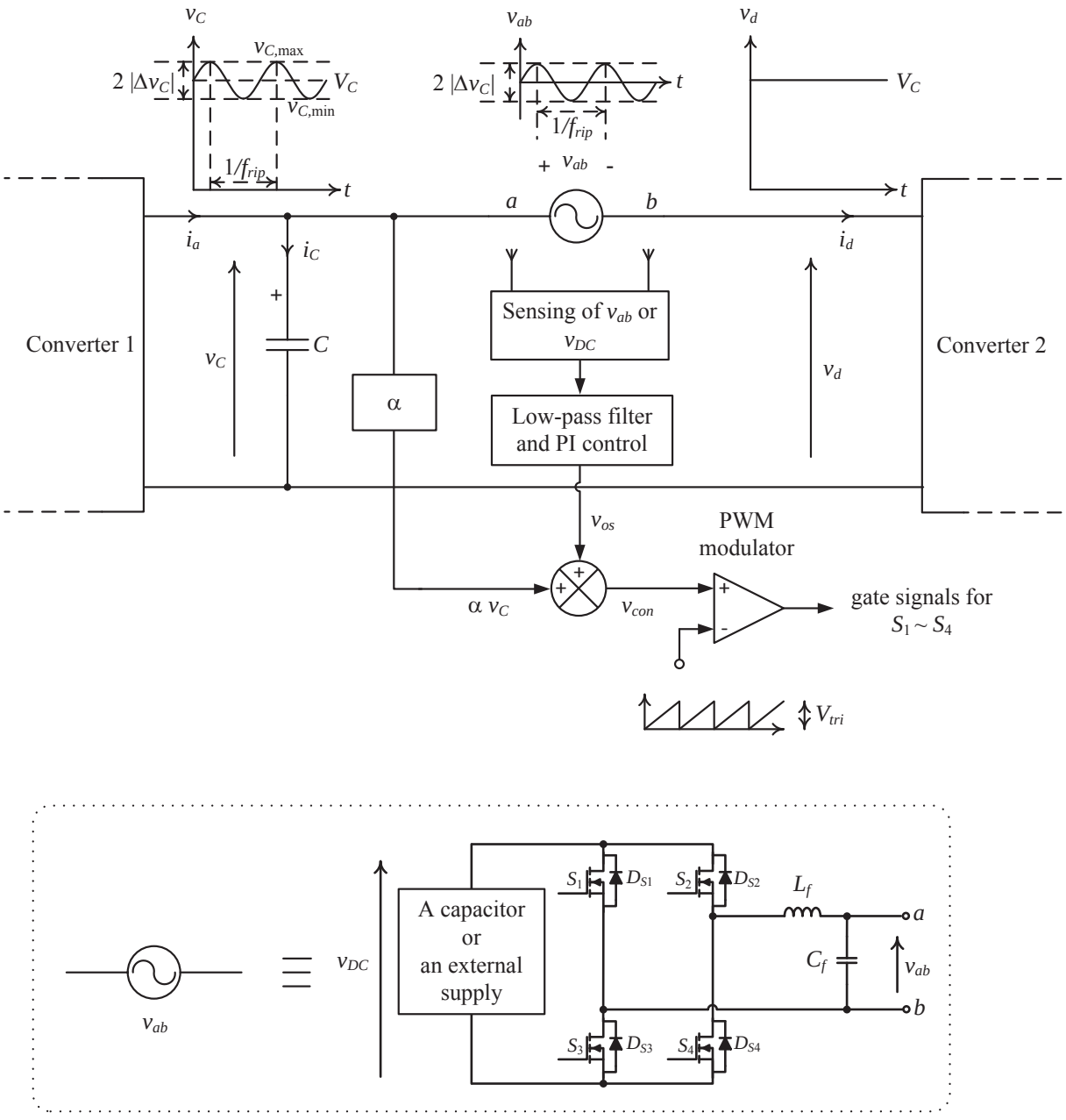


Fig. 1 Basic concept of the proposed dc-link module.

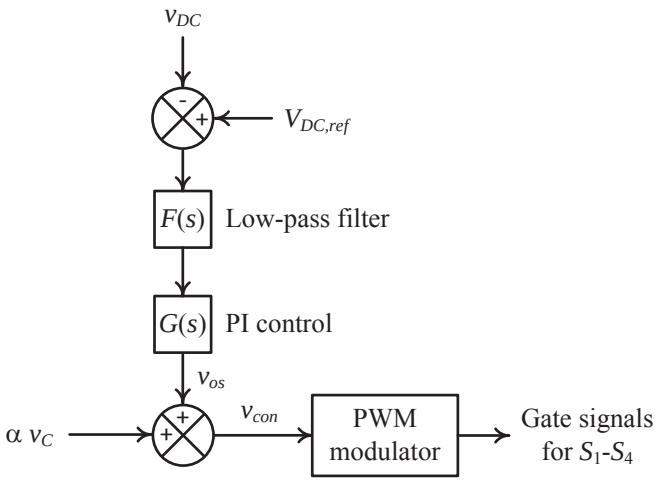


Fig. 2 Control mechanism with a capacitor as the input source of the voltage compensator.

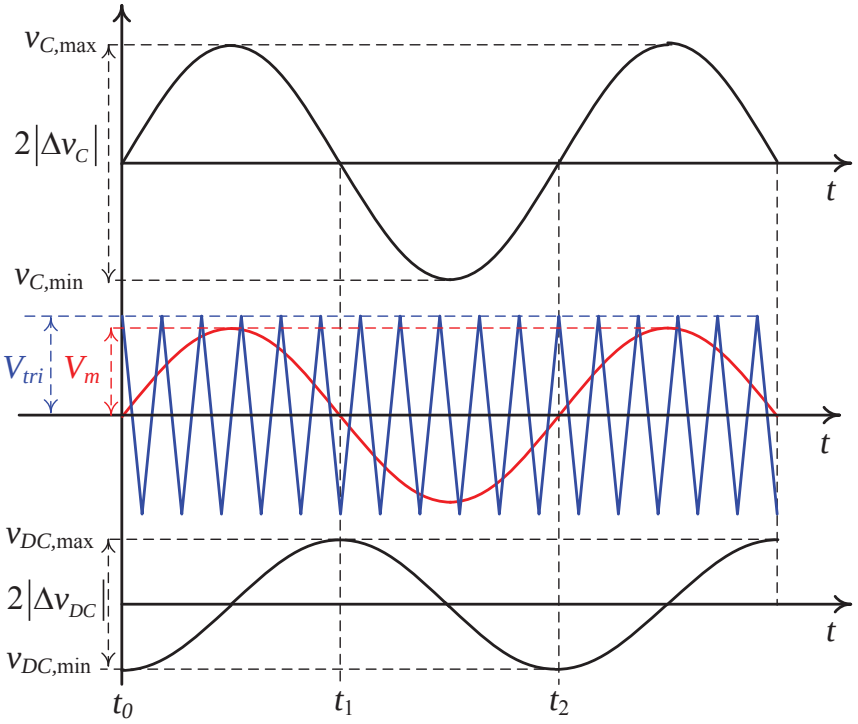
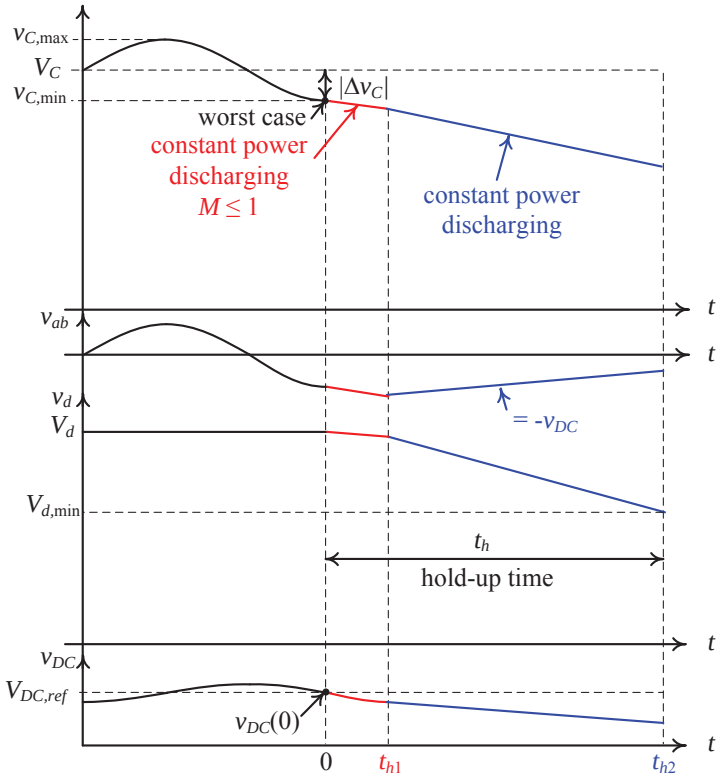
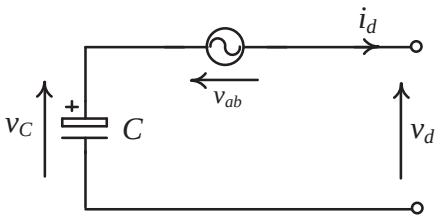


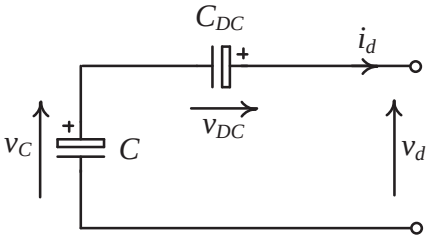
Fig. 3 Operation timing diagram of the voltage compensator.



(a) Waveforms.



(b) Circuit during the time interval $[0, t_{h1}]$.



(c) Circuit during the time interval $[t_{h1}, t_{h2}]$.

Fig. 4 Operations during the hold-up time.

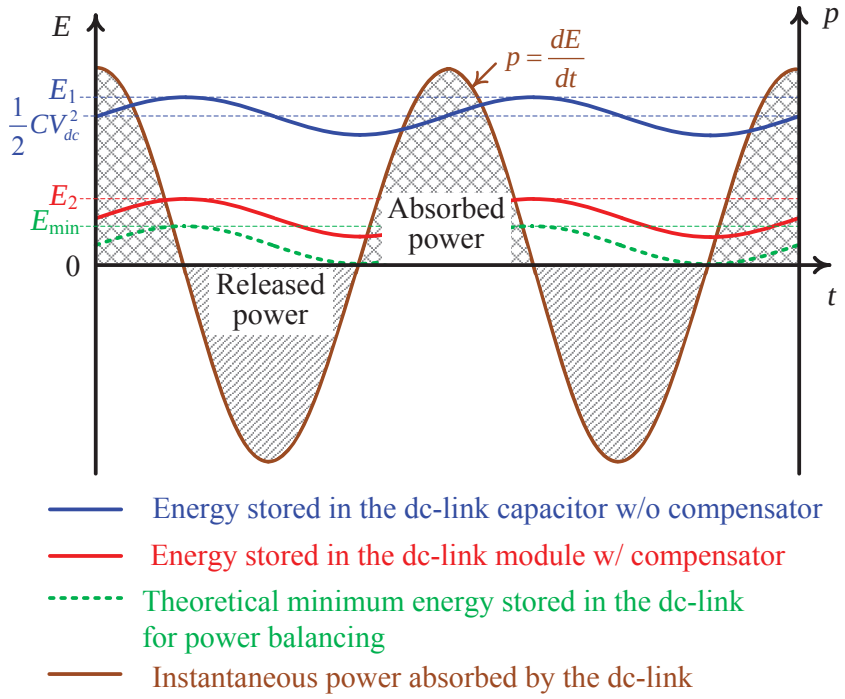


Fig. 5 Energy stored and instantaneous power handled by the dc-link capacitor.

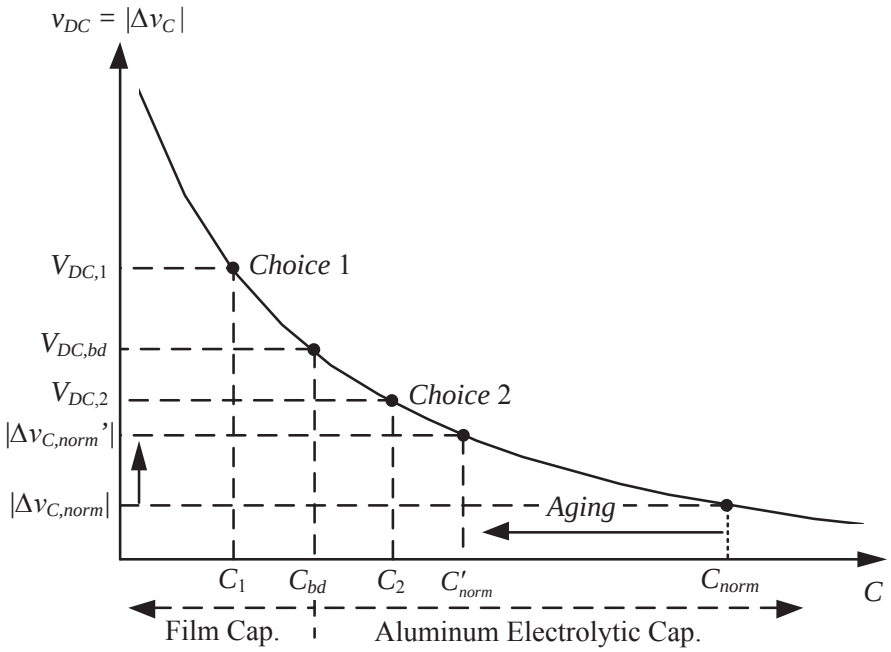


Fig. 6 Relationship between the dc-link capacitance, ripple voltage, and v_{DC}.

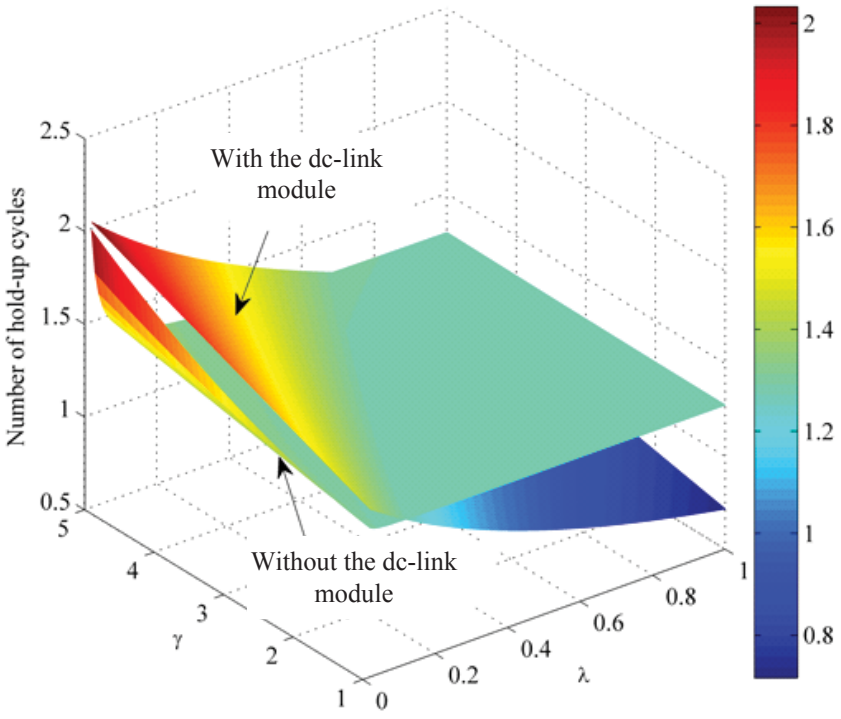


Fig. 7 Hold-up time analysis with and without the dc-link module (β = 1, ρ = 0.8, μ = 0.02).

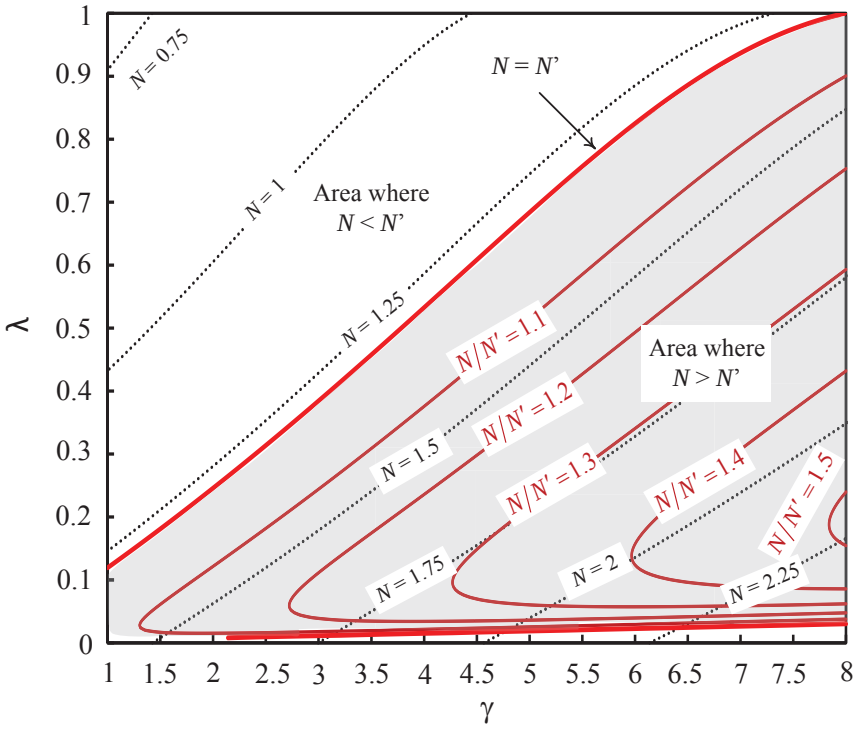
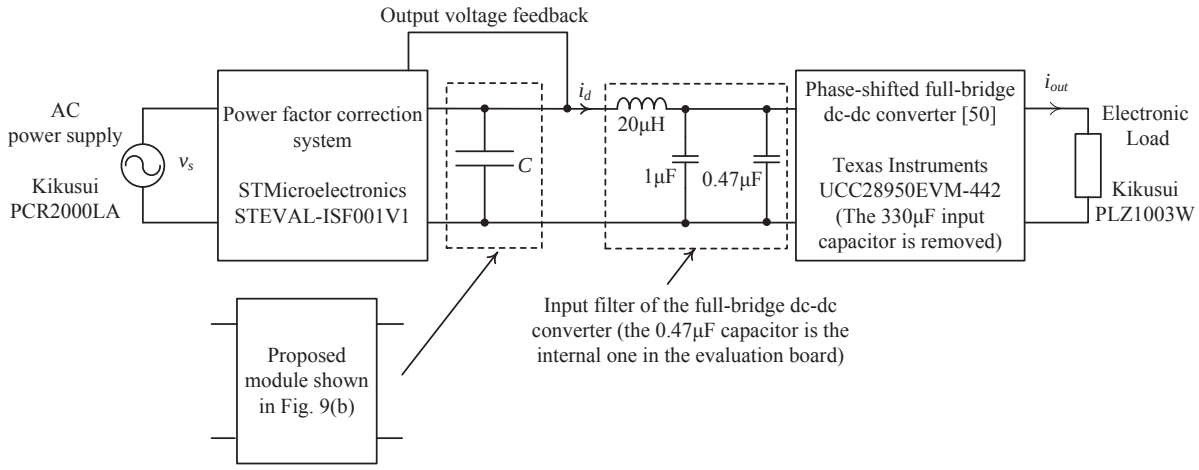
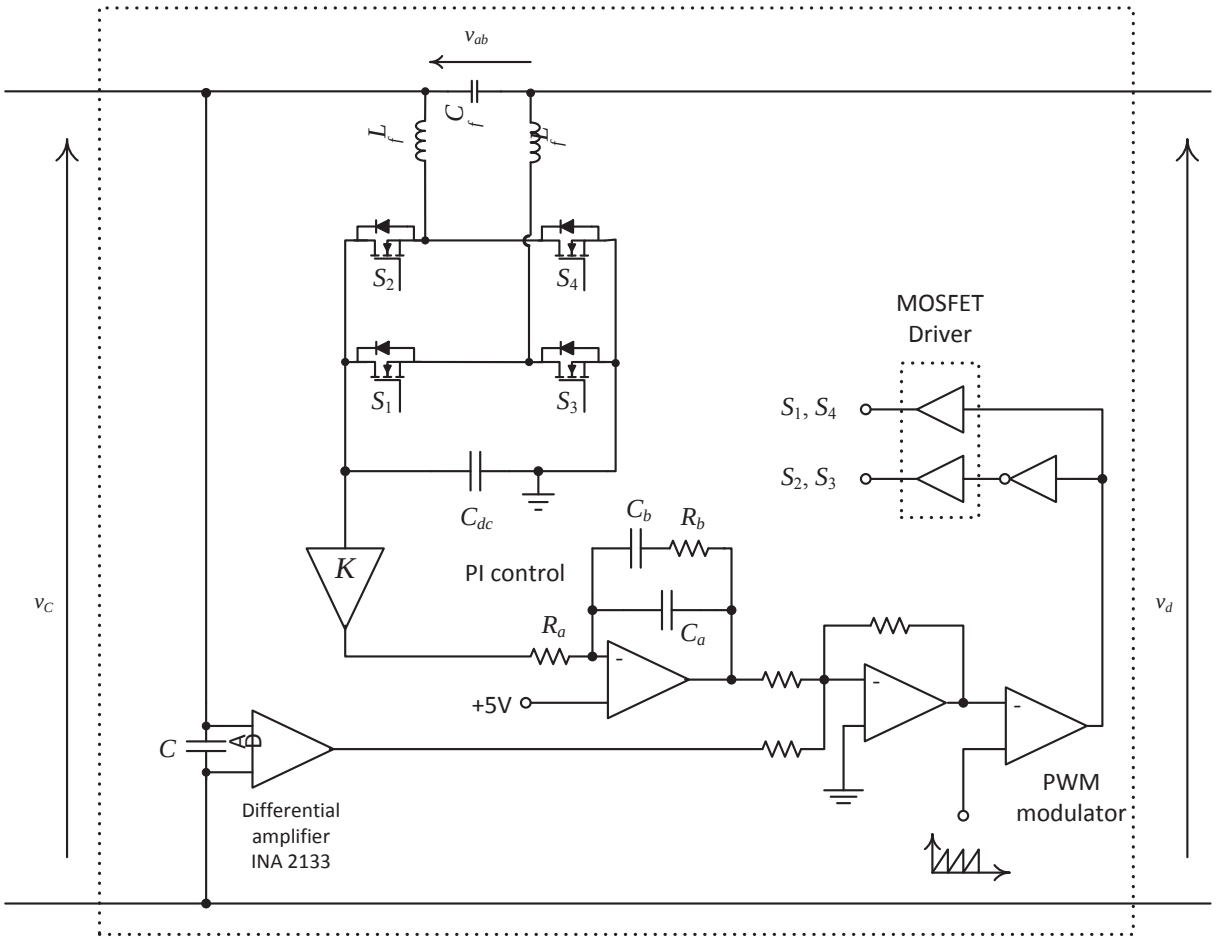


Fig. 8 Design curves for selection of λ and γ (ρ = 0.8, μ = 0.02).

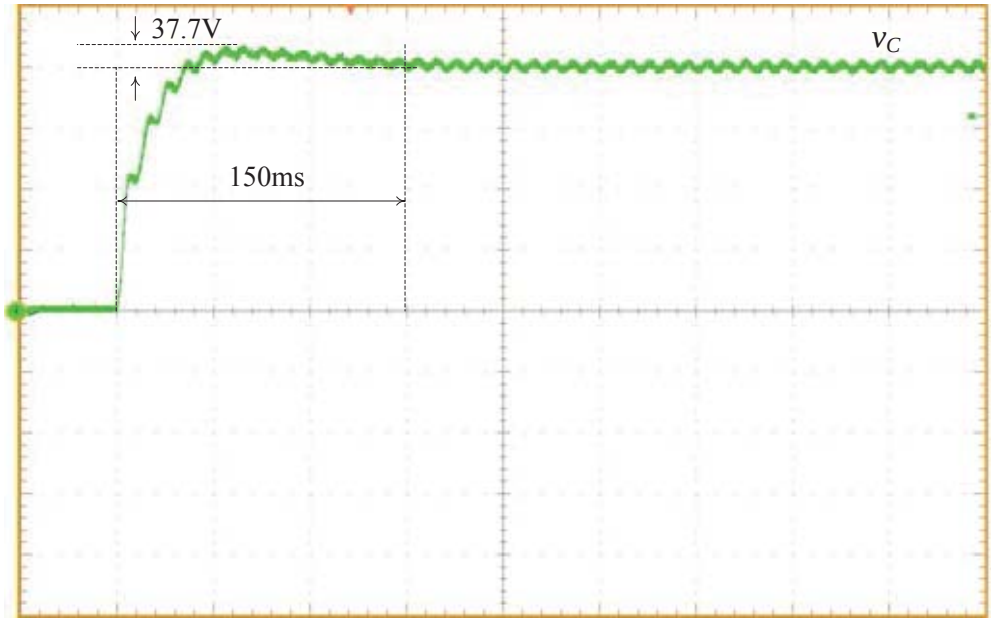


(a) System configuration.

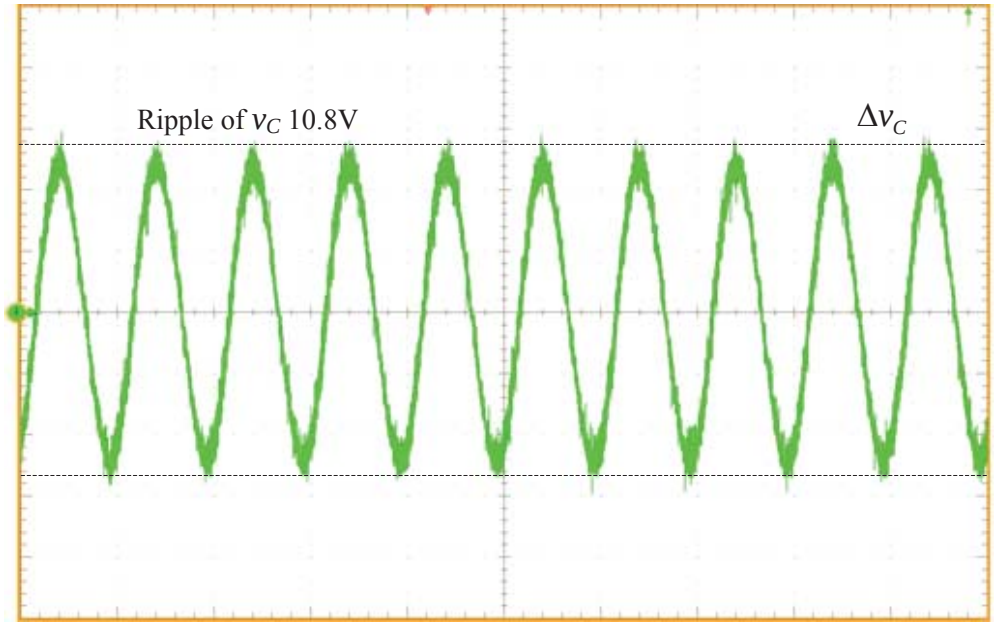


(b) Circuit schematic of the proposed module.

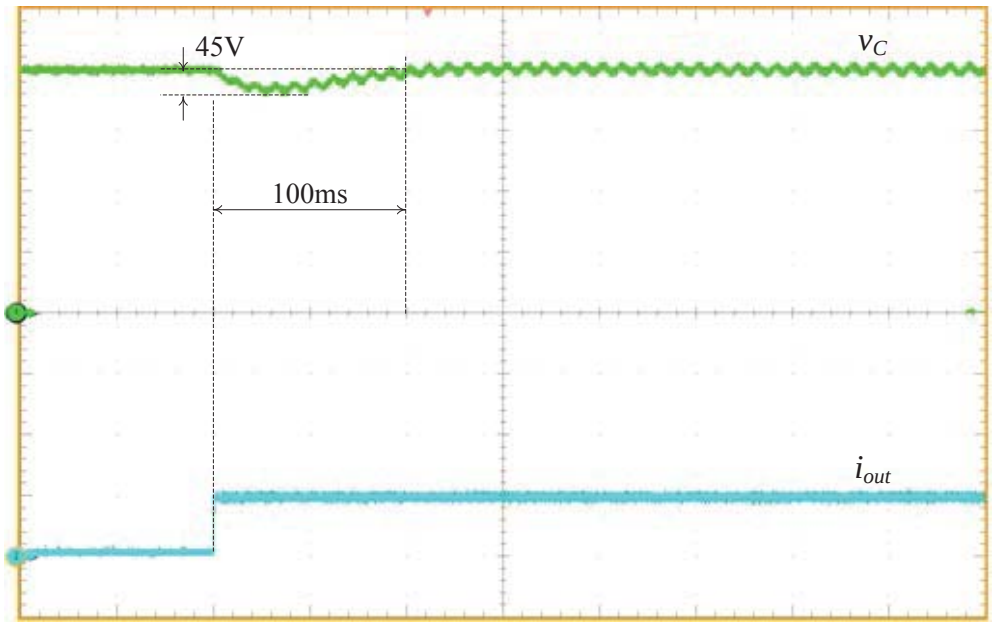
Fig. 9 Experimental test bed.



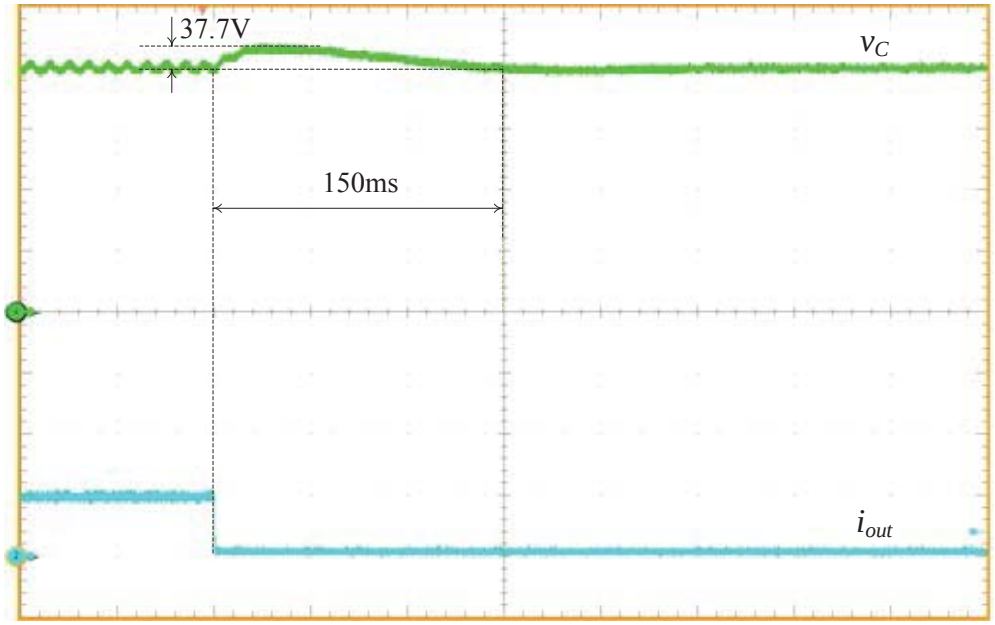
(a) Startup transient under the full load condition (v_C : 100V/div, Timebase: 50ms/div).



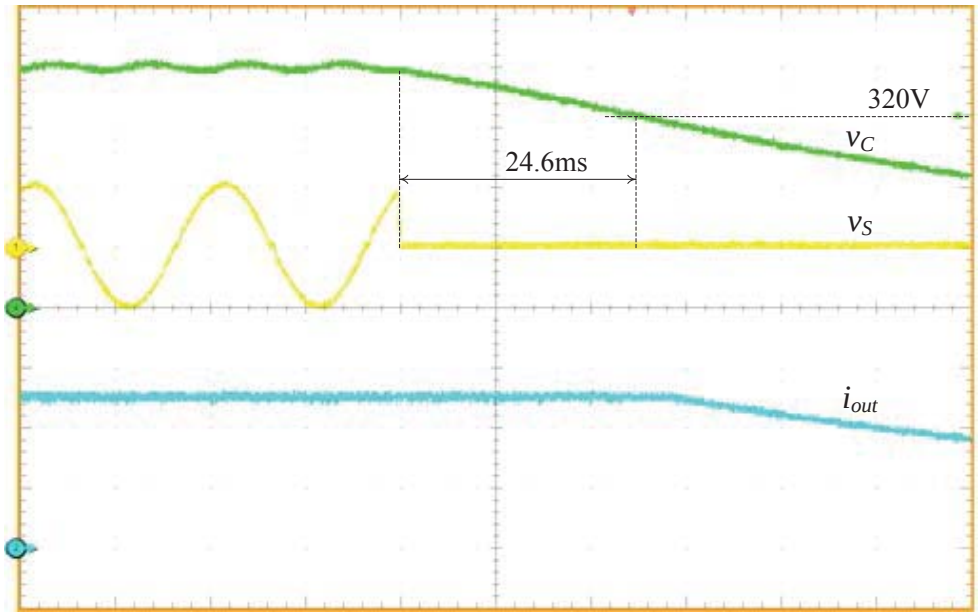
(b) Steady-state dc-link voltage waveform under the full-load condition
(Δv_C : 2V/div, Timebase: 10ms/div).



(c) Transient waveforms when the output is changed from 10% load to full load (v_C : 100V/div, i_{out} : 50A/div, Timebase: 50ms/div).

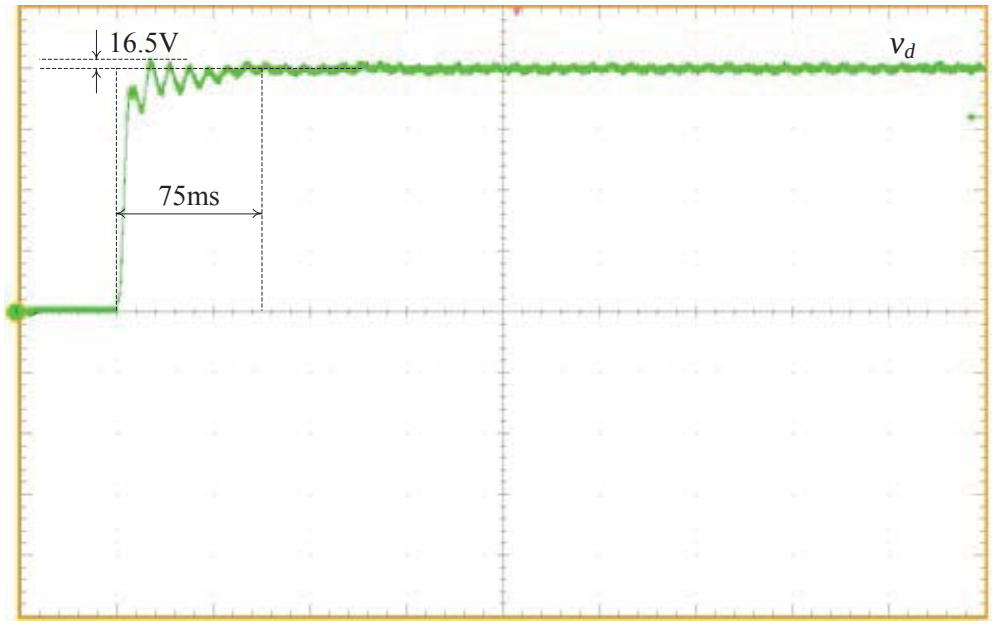


(d) Transient waveforms when the output is changed from full load to 10% load. (v_C : 100V/div, i_{out} : 50A/div, Timebase: 50ms/div).

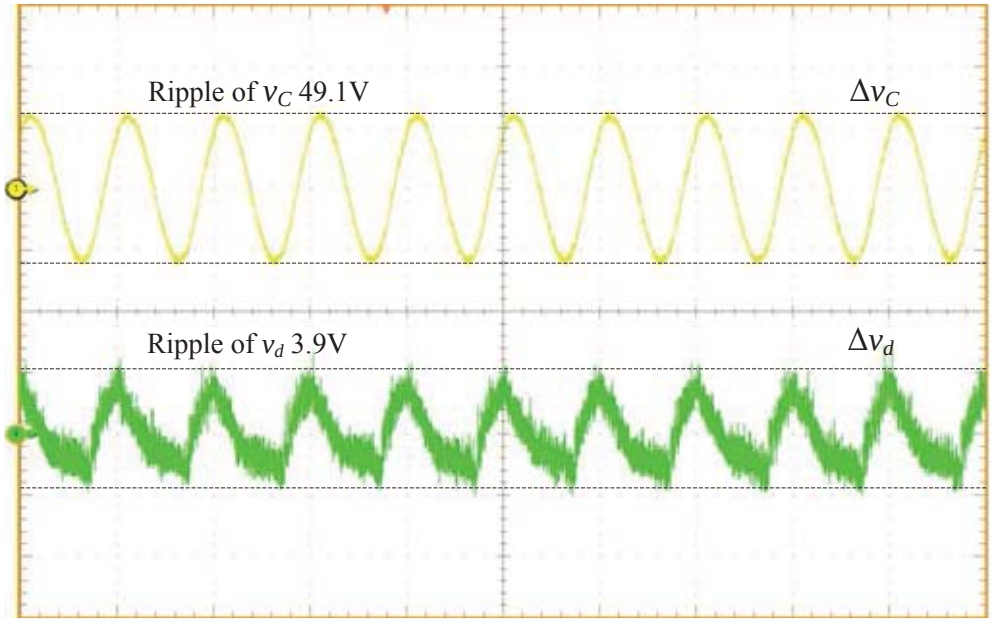


(e) Transient waveforms after a sudden supply outage under the full-load condition.
(v_C :100V/div, v_S : 300V/div, i_{out} : 20A/div, Timebase: 10ms/div).

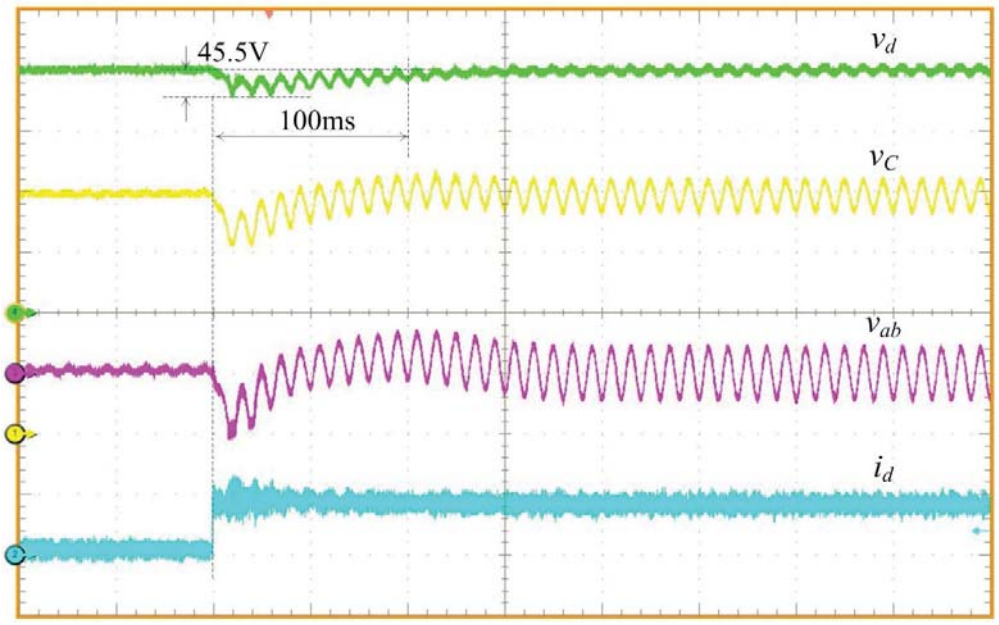
Fig. 10 Experimental waveforms with an electrolytic capacitor bank.



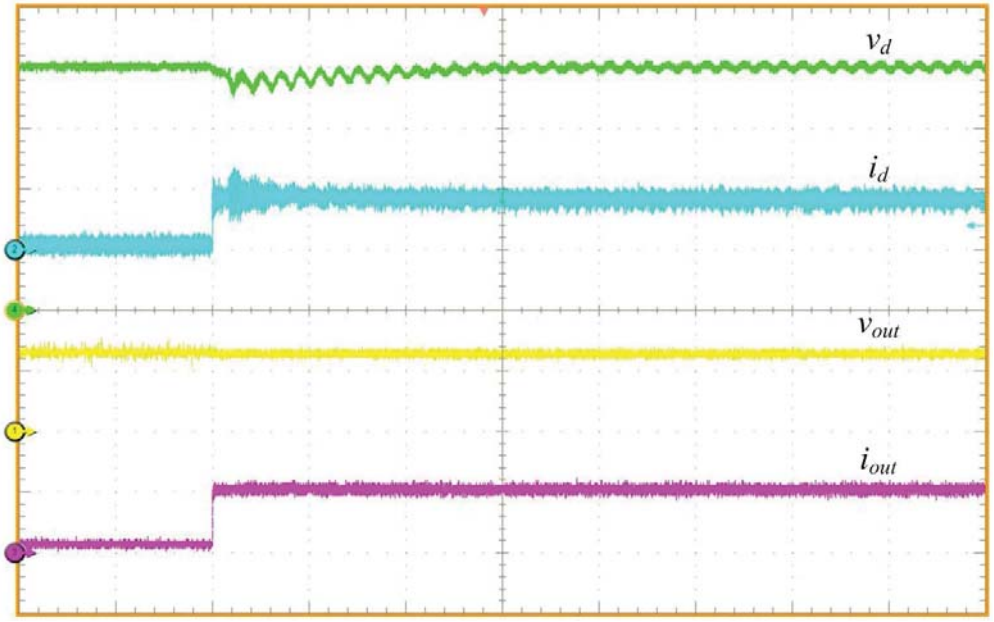
(a) Start-up transient under the full load condition. (v_d : 100V/div, Timebase: 50ms/div).



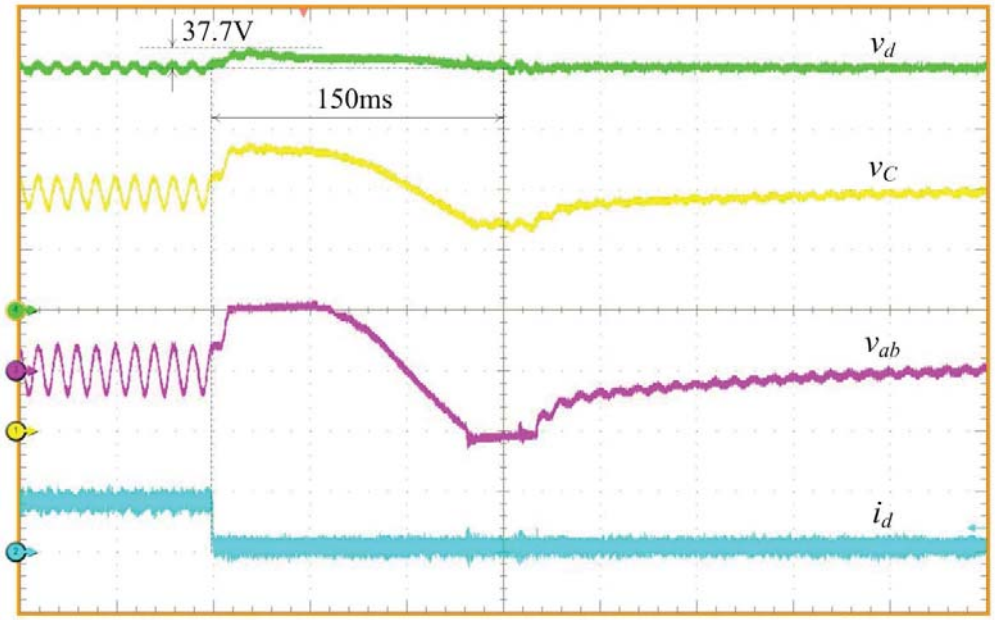
(b) Steady-state waveforms of v_C and v_d under the full-load condition (Δv_C : 20V/div, Δv_d : 2V/div, Timebase: 10ms/div).



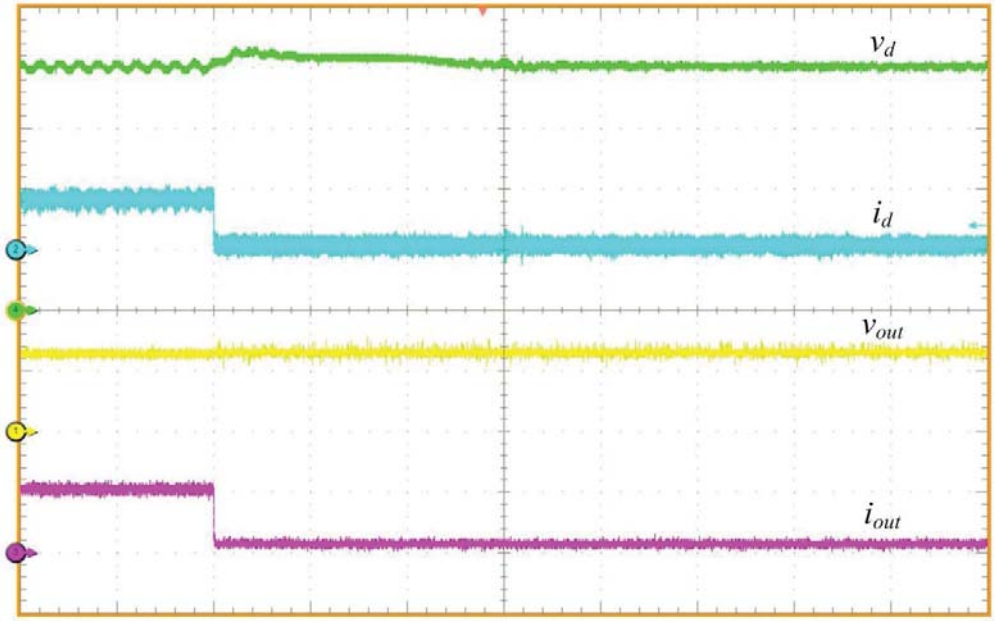
(c) Transient waveforms of the dc-link module when the output is changed from 10% load to full load (v_d : 100V/div, v_C : 100V/div, v_{ab} : 40V/div, i_d : 2A/div, Timebase: 50ms/div).



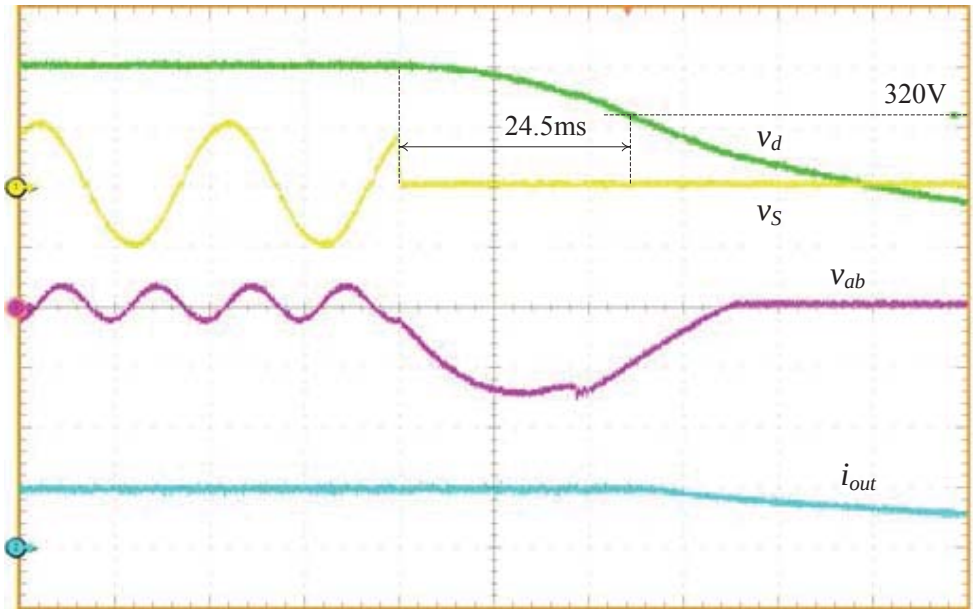
(d) Transient waveforms of the full-bridge dc-dc converter when the output is changed from 10% load to full load (v_d : 100V/div, i_d : 2A/div, v_{out} : 10V/div, i_{out} : 50A/div, Timebase: 50ms/div).



(e) Transient waveforms of the dc-link module when the output is changed from full load to 10% load (v_d : 100V/div, v_C : 100V/div, v_{ab} : 40V/div, i_d : 2A/div, Timebase: 50ms/div).



(f) Transient waveforms of the full-bridge dc-dc converter when the output is changed from full load to 10% load (v_d : 100V/div, i_d : 2A/div, v_{out} : 10V/div, i_{out} : 50A/div, Timebase: 50ms/div).



(g) Transient waveforms after a sudden supply outage under the full-load condition (v_d :100V/div, v_S : 300V/div, v_{ab} : 20V/div, i_{out} : 50A/div, Timebase: 10ms/div).

Fig. 11 Experimental waveforms with the proposed dc-link module.

Table I – Values of the components used in the module

Parameter	Value / part no.	Parameter	Value / part no.
C_f	3.3μF, 100V	L_f	120μH
C_a	10μF, 35V	R_a	100kΩ
C_b	0.1μF, 50V	R_b	33kΩ
$S_1 - S_4$	FDD86102	K	0.1