Supporting Information

Directional Ostwald ripening for producing aligned arrays of nanowires

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Experimental Section

VO_2 nanowire growth: For the growth of the VO_2 nanowires, thin V_2O_5 films were initially deposited onto a 200nm thick, thermally grown SiO_2 layer on a Si(100) single crystal substrate in an RF reactive sputtering chamber with a Vanadium target (99.99%), flowing argon/oxygen mixtures at an operating pressure of 2×10^{-6} torr and substrate temperature of 500°C. The thickness of the thin films was controlled in the approximate range 20 nm to 60 nm by adjusting the deposition time. The thin film was then transferred to the center of a horizontal quartz tube furnace to grow VO_2 nanowire growth at atmospheric pressure. Nanowire growth was carried out for 3 hours at 650°C with flowing high purity He (99.999%) at 200 sccm.

Fabrication of VO_2 nanowire array: V-grooved SiO_2/Si substrates were fabricated by potassium hydroxide (KOH) etching. The native oxide on the Si (100) substrates was removed by buffered oxide etchant (BOE) and 500 nm-thick SiO_2 layer was deposited by using plasma-enhanced chemical vapor deposition (PECVD) to be used as a shadow mask for the wet etching process. By using a photomask having line patterns of pitch size from 2 to 6 μm and conventional lithography process, line patterns of photoresist (PR) were obtained. By reactive ion etching (RIE) process, the SiO_2 was selectively etched away, resulted in the formation of the line patterned SiO_2 on Si substrate. The sample was dipped in 45 % KOH solution for 1 h at 80°C to carry out the anisotropic wet etching, producing V-groove templates with different angles of the grooves, as shown in Figure S5. By changing the etching time, the morphology of the templates could be also controlled. The etched sample was subsequently dipped in the diluted hydrofluoric acid (HF:H_2O = 1:1) at room temperature to remove the SiO_2 etch mask layer. SiO_2 and V_2O_5 thin films were deposited on the V-grooved Si substrate using PECVD and sputtering. (DC, 100W, Ar O_2 30:11 sccm, 5 mTorr, 400° C 2h 200nm); VO_2 nanowires were grown by CVD without using any catalysts. Before heating the source material, the furnace tube was evacuated to about 10^{-3} Torr; the furnace temperature was increased at a rate of 18°C/min to a final temperature of ~ 750°C which was maintained for 2 h. A constant flow of high purity helium (1000 sccm) was maintained in the chamber throughout the experiment. The optimal deposition temperature was found to be between 700 °C and 750°C. The size distribution, lattice structure, and crystal orientation of the as-synthesized products were

characterized by scanning electron microscopy (SEM), x-ray diffraction (XRD), and transmission electron microscopy (TEM).

Fabrication of strain sensor: In order to completely separate the VO_2 nanowire and the SiO_2 from the SiO_2/Si substrate, it was etched by BOE for 1 hour and rinsed with deionized water. The PDMS was prepared by mixing the liquid PDMS elastomer and a curing agent in the ratio 10:1 by weight. The liquid mixture was poured onto the VO_2 nanowire arrays grown on the Si substrates and thermally cured at 90°C for 30 min. After curing, the PDMS was peeled off the VO_2 nanowires array covered Si substrate, and Cr/Au (20/300 nm) electrodes were fabricated on the substrate across the VO_2 nanowires. A constant 1 V was applied to evaluate the performance of the strain sensor.

Molecular dynamical simulation: Molecular dynamical simulations were performed using the open source package, GROMACS v 4.5.4. Lennard-Jones (LJ) particles were assumed to interact via a LJ potential with a cutoff at 2.5σ and $\epsilon_{pp} = 2.0k_BT$. The surfaces were constructed by arranging LJ particles whose positions were fixed. The mobile LJ particles also interact with the surface particles via the LJ potential with a cutoff at 2.5σ but with $\epsilon_{ps} = 0.8k_BT$. (k_B is the Boltzmann constant, T is the absolute temperature, σ is an approximate diameter of LJ particles, which were set to 1, and k_BT is set to 1.0 using the V-rescale method.)

Characterization: The morphologies of the VO_2 nanowire was investigated using a cold field emission scanning electron microscope (FE-SEM, S-4800, Hitachi) with an accelerating voltage of 10 kV. Elemental analysis was carried out in the SEM using energy-dispersive X-ray spectroscopy (EDX). The high-resolution TEM images were collected using a Cs-corrected JEM-2100F operated at 200 kV. For EELS experiments, a dedicated scanning transmission electron microscope JEM-2100F was used. The microscope was operated at 200 keV. It is equipped with an electron energy-loss spectrometer (Gatan, Enfina). The energy resolution in EELS, as measured by the full width at half maximum of the zero-loss peak, was 0.8 eV.

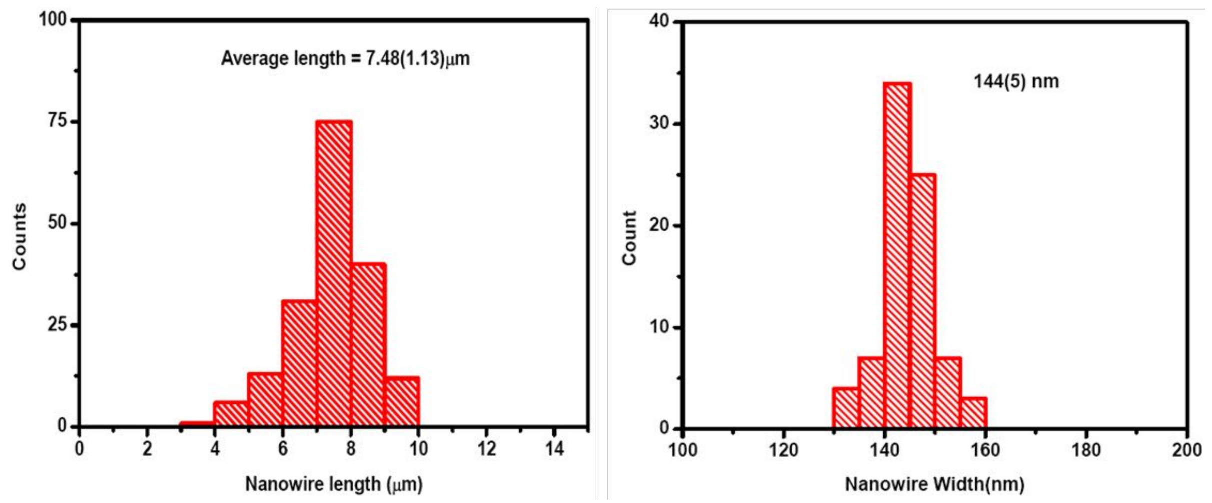


Figure S1. The histogram of length and width of randomly oriented VO_2 nanowires on a SiO_2/Si substrate.

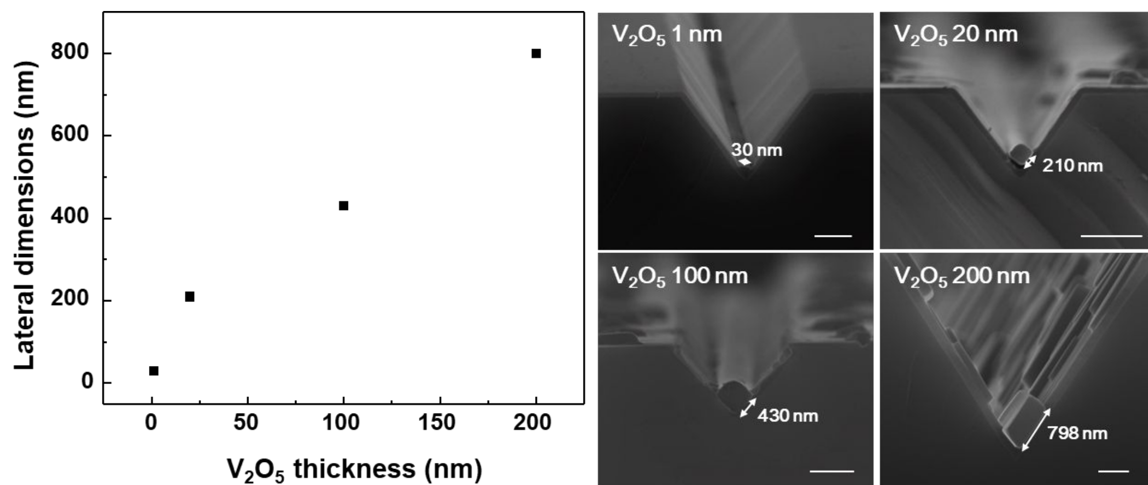


Figure S2. The VO_2 nanowire growth as a function of the V_2O_5 thin film thickness. Scale bars,

500 nm.

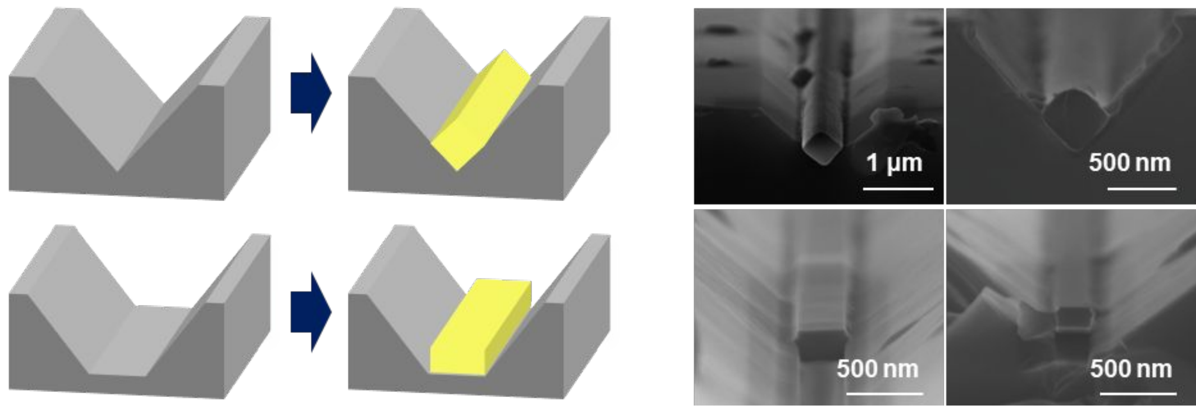


Figure S3. The cross-sectional images of the grown VO_2 with the shape of the V-grooved surface.

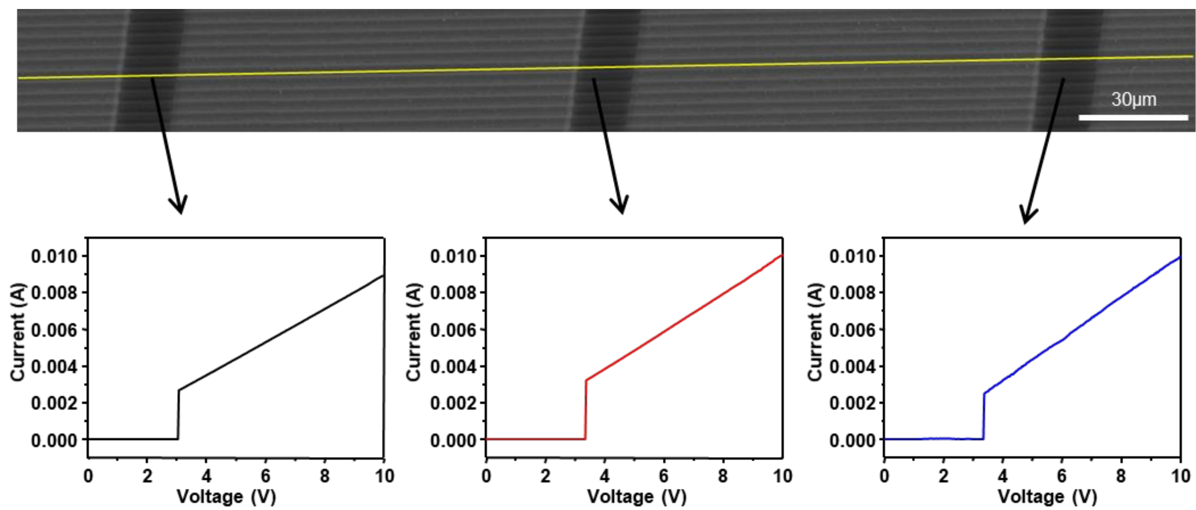


Figure S4. The millimeter-long VO_2 nanowires SEM image and I-V measurement graph.

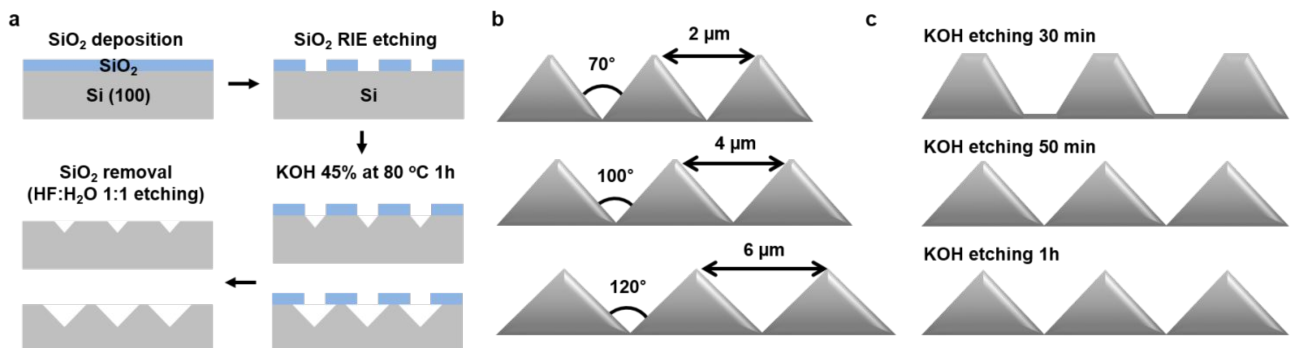


Figure S5. (a) Schematic fabrication process of V-groove templates and schematic diagrams of the V-groove templates with different pitch size (b) and KOH etching time (c).

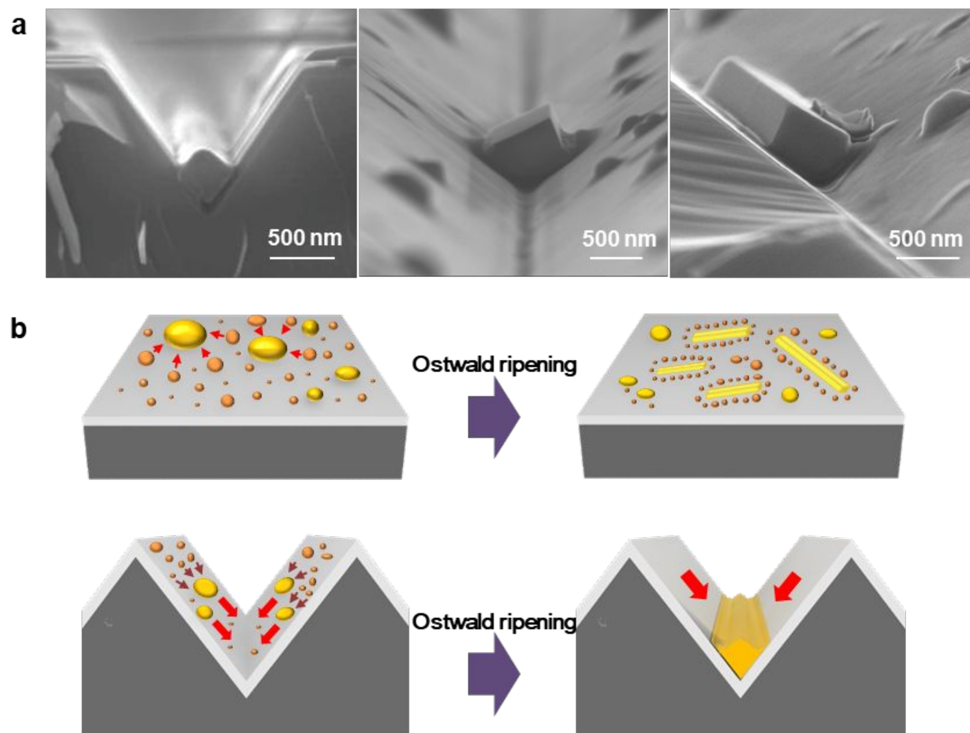


Figure S6. (a) The SEM image of VO_2 nanwire tail located on V groove substrate and (b) the schematic image of Ostwald ripening process on flat substrate and V groove substrate.

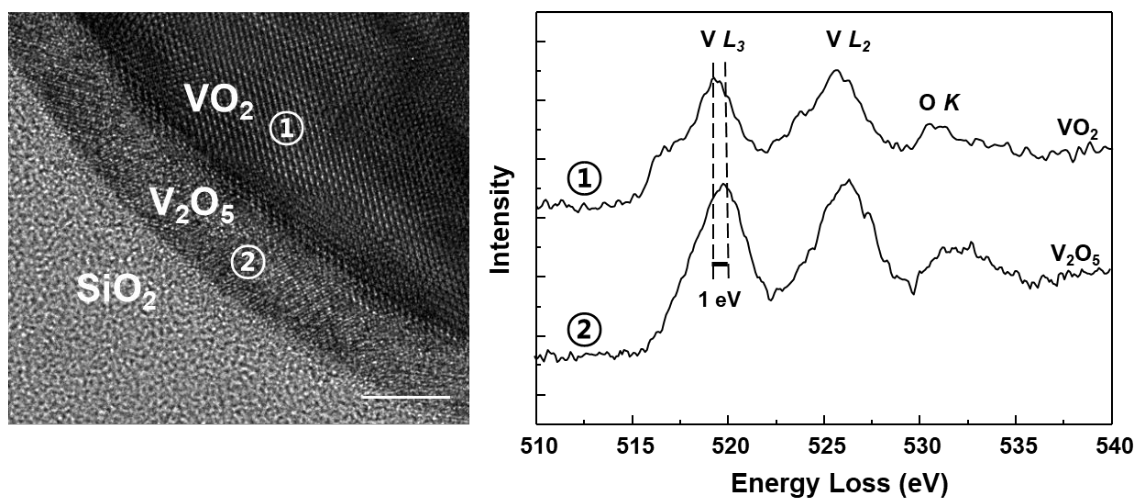


Figure S7. Electron energy loss spectroscopy (EELS) in V_2O_5 and VO_2 regions.

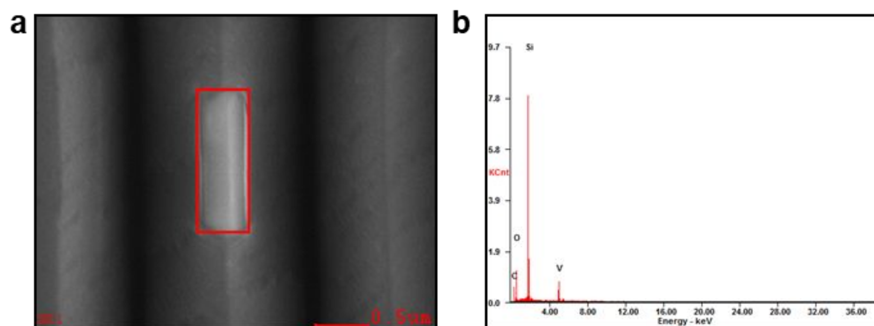
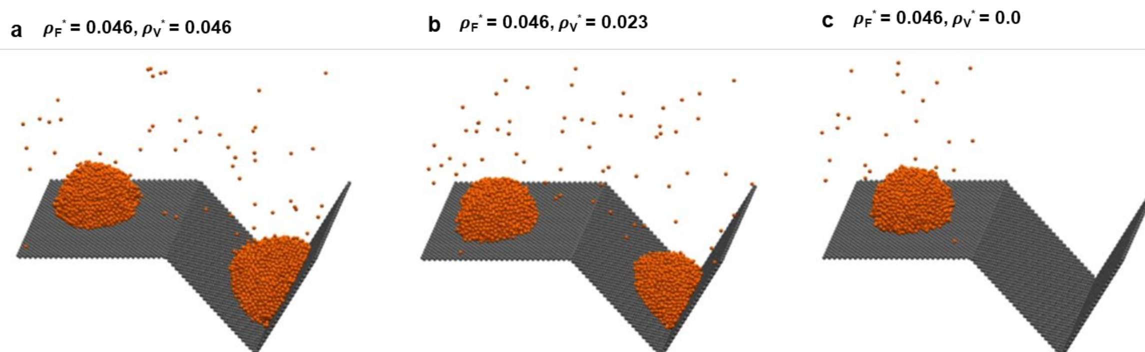


Figure S8. (a) SEM image and (b) EDXS result of the transferred VO_2 nanowire onto PDMS substrate.



Movie 1. Video showing the results of a real-time molecular dynamics (MD) simulation of directional Ostwald ripening.