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(71) Applicant: **APPLY CARD TECHNOLOGY LIMITED** [CN/CN]; 924A, Well Fung Industrial Centre, 68 Ta Chuen Ping Street, Kwai Chung, Hong Kong (CN).

(72) Inventor: **WU, Xiaoxing**; 924A, Well Fung Industrial Centre, 68 Ta Chuen Ping Street, Kwai Chung, Hong Kong (CN).

(74) Agent: **RUNPING&PARTNERS**; Suite 515, Yingu Mansion, No.9 Beisihuanxilu, Haidian District, Beijing 100190 (CN).

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(54) Title: METHODS OF MANUFACTURING IC CARD CIRCUIT BOARD SUBSTRATES AND IC CARDS

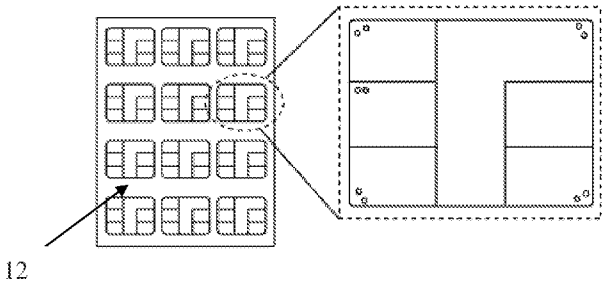

Fig. 5

(57) Abstract: A method of manufacturing an integrated circuit (IC) card circuit board substrate (18) is disclosed as including steps (a) providing a substrate (12) with two opposite major surfaces (13) both covered by a layer of copper, (b) forming at least two holes (14) through the substrate, each said hole being of a diameter of no more than 0.50 mm, (c) depositing a layer of copper on an interior surface (16) of each of the two holes, the layer of copper covering at least part of each of the major surfaces of the substrate, (d) forming an electric circuit on at least one of the major surfaces of the substrate, and (e) depositing at least a layer of nickel (15) and a layer of gold (17) on the layer of copper

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Methods of Manufacturing IC Card Circuit Board Substrates and IC Cards

[0001] This invention relates to methods of manufacturing integrated circuit (IC) card circuit board substrates and manufacturing IC cards (or so called "smart cards") and in particular such methods suitable for, but not limited to, manufacturing contact IC card circuit board substrates and contact IC cards.

Background of the Invention

[0002] Contact IC cards were devised in the 1990's and have since been undergoing development. For contact IC cards, at least a major surface of an IC module of the IC card with a read/write interface is exposed to the outside environment. Contact IC card does not carry power source. When in use, the read/write interface of the contact IC card is in direct physical contact with a read/write head of a computer terminal or processor, whereby data may be written into or read from the IC module in the contact IC card. The signals transmitted by the read/write head consist of two parts, namely a first part being an electric power signal which provides the electric power for the IC module, and a second part being combined data signals directing the IC module to carry out changing and storing of data, and to provide feedback to the read/write head.

[0003] With the development of communications technology, contact IC cards have been used as finance IC cards, SIM (which stands for "subscriber identity module" or "subscriber identification module") cards, in GSM and CDMA mobile phone communications technology, and in such daily areas as access control, transport, social security, identity certification, and electronic wallets.

[0004] The existing methods of manufacturing contact IC card circuit board substrates are rather complicated. In addition, after manufacture of the substrates, it is still necessary to arrange for the holes provided on the contact IC card circuit board substrates to be electrically conducting by laser, or alternatively by adding solder. Such increases the production cost and adversely affects competitiveness in the market.

[0005] It is thus an object of the present invention to provide a method of manufacturing IC card circuit board substrates and a method of manufacturing IC cards in which the aforesaid shortcomings are mitigated or at least to provide a useful alternative to the trade and

public.

Summary of the Invention

[0006] According to a first aspect of the present invention, there is provided a method of manufacturing an integrated circuit (IC) card circuit board substrate, including (a) providing a substrate with two opposite major surfaces both covered by a layer of copper, (b) forming at least two holes through said substrate, each said hole being of a diameter of no more than 0.50 mm, (c) depositing a layer of copper on an interior surface of each of said two holes, said layer of copper covering at least part of each of said major surfaces of said substrate, (d) forming an electric circuit on at least one of said major surfaces of said substrate, and (e) depositing at least a layer of nickel and a layer of gold on said layer of copper.

[0007] According to a second aspect of the present invention, there is provided a method of forming an integrated circuit (IC) card, including steps (a) providing a substrate with two opposite major surfaces both covered by a layer of copper, (b) forming at least two holes through said substrate, each said hole being of a diameter of no more than 0.50 mm, (c) depositing a layer of copper on an interior surface of each of said two holes, said layer of copper covering at least part of each of said major surfaces of said substrate, (d) forming an electric circuit on at least one of said major surfaces of said substrate, and (e) depositing at least a layer of nickel and a layer of gold on said layer of copper, (l) fixedly securing an IC module with said substrate, and (m) electrically connecting said IC module with said electric circuit on said at least one of said major surfaces of said substrate.

Brief Description of the Drawings

[0008] Embodiments of the present invention will now be described, by way of examples only, with reference to the accompanying drawings, in which:

Figs. 1 to 6 show a method according to an embodiment of the present invention to manufacture an integrated circuit (IC) card circuit board substrate,

Fig. 7 shows a schematic diagram of an IC card formed by flip flop bonding on an IC card circuit board substrate manufactured according to an embodiment of the present invention;

Figs. 8 to 10 show a method of forming the IC card of Fig. 7;

Fig. 11 shows a schematic diagram of an IC card formed by wire bonding on an IC card circuit board substrate manufactured according to an embodiment of the present invention;

and

Figs. 12 to 16 show a method of forming the IC card of Fig. 11.

Detailed Description of the Embodiments

[0009] Fig. 1 shows an FR4 sheet 10 from which a substrate 12 (which is here also called "flexible circuit board" (FCB)) is cut out. Both opposite major surfaces 13 of the FR4 sheet 10 (and thus of the FCB 12) are covered by copper. As shown in Fig. 2, pairs of holes 14 are formed through the FCB 12, e.g. by drilling or punching. Fig. 3 shows that, after drilling or punching, the cylindrical interior surface 16 of the holes 14 is not covered by an electrically conductive material, e.g. copper, and thus the two opposite major surfaces 13 of the PCB 12 are not electrically connected with each other..

[0010] The FCB 12 is then placed in a treatment tank for electroplating an electrically conductive material, e.g. copper, onto the cylindrical interior surface 16 of the holes 14. The electroplating process is carried out at a temperature of 0 ^{o}C to 75 ^{o}C for 2 hours. The treatment tank contains sodium hydroxide at a concentration of 12 grams per litre, formaldehyde at a concentration of 5 grams per litre, copper ions at a concentration of 2 grams per litre, and plastic palladium at a concentration of 5 grams per litre. A layer of copper is then formed on the cylindrical interior surfaces 16 of the holes 14 and on each opposite major surface 13 of the FCB 12, as shown in Fig. 4. The two opposite major surfaces 13 of the PCB 12 are thus electrically connected with each other.

[0011] An electric circuit is then formed on the major surfaces 13 of the FCB 12. A circuit pattern is first formed on the major surfaces 13 of the FCB 12. In particular, by using film exposure principle, a photo-resist material is applied on the major surfaces 13 of the FCB 12 to form pre-determined circuit patterns. Copper is then electroplated on the major surface 13 of the FCB 12 by placing the FCB 12 in a treatment tank for electroplating. The treatment tank contains tin brightener at a concentration of 20 millilitres per litre, copper brightener at a concentration of 5 millilitres per litre, sulfuric acid at a concentration of 180 grams per litre, copper sulfate at a concentration of 70 grams per litre, chloride ions at a concentration of 50 parts per million (PPM), electroplating tin at a concentration of 30 grams per litre, and tin (II) sulfate at a concentration of 30 grams per litre, and electroplating is carried out at a temperature of 0 ^{o}C to 45 ^{o}C for 2 hours. Excessive copper is then removed

by an etching solution containing copper chloride and aqueous chloride, such that the remaining copper on the major surfaces 13 of the FCB 12 forms the electric circuit, as shown in Fig. 5.

[0012] As shown in Fig. 6, a layer of nickel (Ni) 15 is then deposited on the layer of copper on the upper and lower surfaces 13 and the interior surface 16 of the holes 14 of the FCB 12 and a layer of gold (Au) 17 is deposited on the layer of nickel 15 by treating the FCB 12 by electroless nickel immersion gold (ENIG) in a treatment tank containing a gold plating bath solution at a concentration of 100 millitres per litre, potassium gold cyanide at a concentration of 0.8 grams per litre, nickel ions at a concentration of 4.6 grams per litre and palladium ions at a concentration of 3 grams per litre for 2 hours and at a temperature of 0 ^{o}C to 95 ^{o}C, to form an integrated circuit (IC) card circuit board substrate 18. ENIG is a type of surface plating, and the layer of immersion gold protects the layer of nickel from oxidation. In the IC card circuit board substrate 18, the two opposite major surfaces are electrically connected with each other *via* the holes 14.

[0013] The method of manufacturing the integrated circuit (IC) card circuit board substrate 18 according to the present invention is relatively simple and does not require the use of solder or laser for causing the holes to be electrically conductive, thus lowering the production cost.

[0014] Fig. 7 shows a schematic diagram of an IC card 20 (such as a SIM card) formed by flip flop bonding on the IC card circuit board substrate (FCB) 18. Figs. 8 to 10 show a method of forming the IC card 20 by the flip flop bonding method. An integrated circuit (IC) module 22 (also called a "chip" or a "wafer") is picked up by a first pick tool 24. The first pick tool 24 then rotates and passes the IC module 22 to a second pick tool 26. The second pick 26 then rotates and places the IC module 22 on the substrate 18. An adhesive 28 is then applied on the IC module 22 and the substrate 18 to secure the IC module 22 to the substrate 18. Two electrically conductive wires (e.g. gold wires) are then bonded (e.g. by ultrasonic bonding) to the contact points on the IC module 22 and the contact points on the substrate 18 to electrically connect the IC module 22 with the electric circuit on the substrate 18. The IC card 20 is formed. UV plastic is then added and subsequently treated for encapsulating the IC module 22, for water-proof and dust-proof purposes.

[0015] Fig. 11 shows a schematic diagram of an IC card 30 (such as a SIM card) formed by wire bonding on the IC card circuit board substrate 18 manufactured according to an embodiment of the present invention. Figs. 12 to 16 show a method of forming the IC card 30 by the wire bonding method. An adhesive 32 is provided at the location on the substrate (FCB) 18 for subsequently fixedly receiving an IC module. A tool 34 picks up an integrated circuit (IC) module 22 (also called a "chip" or a "wafer") and places the IC module 22 on the adhesive 32 on the FCB 18. Two electrically conductive wires 36 (e.g. gold wires) are then bonded (e.g. by ultrasonic bonding) to the contact points on the IC module 22 and the contact points on the substrate 18 to electrically connect the IC module 22 with the electric circuit on the substrate 18. An electrically conductive adhesive 38 is then applied to further secure the connection between the electrically conductive wires 36 and the FCB 12. The IC card 30 is formed. UV plastic 40 is then added and subsequently treated for encapsulating the IC module 22, for water-proof and dust-proof purposes.

[0016] It should be understood that the above only illustrates examples whereby the present invention may be carried out, and that various modifications and/or alterations may be made thereto without departing from the spirit of the invention.

[0017] It should also be understood that certain features of the invention, which are, for clarity, described in the context of separate embodiments, may be provided in combination in a single embodiment. Conversely, various features of the invention which are, for brevity, described in the context of a single embodiment, may also be provided separately or in any appropriate sub-combinations.

Claims

1. A method of manufacturing an integrated circuit (IC) card circuit board substrate, including:
   (a) providing a substrate with two opposite major surfaces both covered by a layer of copper,
   (b) forming at least two holes through said substrate, each said hole being of a diameter of no more than 0.50 mm,
   (c) depositing a layer of copper on an interior surface of each of said two holes, said layer of copper covering at least part of each of said major surfaces of said substrate,
   (d) forming an electric circuit on at least one of said major surfaces of said substrate, and
   (e) depositing at least a layer of nickel and a layer of gold on said layer of copper.

2. A method according to any of Claim 1, wherein said at least two holes are formed by drilling and/or punching.

3. A method according to Claim 1 or 2, wherein said substrate is a flexible circuit board.

4. A method according to any of the preceding claims, wherein said step (c) is carried out at a temperature of 0 °C to 75 °C.

5. A method according to any of the preceding claims, wherein said step (c) is carried out for substantially 2 hours.

6. A method according to any of the preceding claims, wherein said step (c) is carried out in a first treatment tank containing at least sodium hydroxide, formaldehyde, copper ions and plastic palladium.

7. A method according to Claim 6, wherein said first treatment tank contains copper ions at a concentration of substantially 2 grams per litre.

8. A method according to Claim 6 or 7, wherein said first treatment tank contains sodium

hydroxide at a concentration of substantially 12 grams per litre.

9. A method according to any one of Claims 6 to 8, wherein first treatment tank contains formaldehyde at a concentration of substantially 5 grams per litre.

10. A method according to any one of Claims 6 to 9, wherein first treatment tank contains plastic palladium at a concentration of substantially 5 grams per litre.

11. A method according to any of the preceding claims, wherein said step (d) includes a step (f) of forming a circuit pattern on said at least one of said major surfaces of said substrate, and a step (g) of depositing copper on said circuit pattern to form said electric circuit.

12. A method according to Claim 11, wherein said step (g) includes a step (h) of electroplating copper on said at least one of said major surfaces of said substrate and a step (i) of removing unwanted copper from said at least one of said major surfaces of said substrate whereby the remaining copper on said at least one of said major surfaces of said substrate forms said electric circuit.

13. A method according to Claim 12, wherein said step (h) is carried out in a second treatment tank containing at least tin brightener, copper brightener, sulfuric acid, copper sulfate, chloride ions, electroplating tin, and tin (II) sulfate.

14. A method according to Claim 13, wherein said second treatment tank contains tin brightener at a concentration of substantially 20 millilitres per litre.

15. A method according to Claim 13 or 14, wherein said second treatment tank contains sulfuric acid at a concentration of substantially 180 grams per litre.

16. A method according to any one of Claims 13 to 15, wherein said second treatment tank contains copper brightener at a concentration of substantially 5 millilitres per litre.

17. A method according to any one of Claims 13 to 16, wherein said second treatment tank contains copper sulfate at a concentration of substantially 70 grams per litre.

18. A method according to any one of Claims 13 to 17, wherein said second treatment tank contains chloride ions at a concentration of substantially 50 parts per million (PPM).

19. A method according to any one of Claims 13 to 18, wherein said second treatment tank contains electroplating tin at a concentration of substantially 30 grams per litre.

20. A method according to any one of Claims 13 to 19, wherein said second treatment tank contains tin (II) sulfate at a concentration of substantially 30 grams per litre.

21. A method according to any one of Claims 12 to 20, wherein said step (g) is carried out at a temperature of 0 °C to 45 °C.

22. A method according to any one of Claims 12 to 21, wherein said step (i) is carried out by using an etching solution including at least copper chloride and aqueous ammonia.

23. A method according to any one of Claims 12 to 22, wherein said step (g) is carried out for substantially 2 hours.

24. A method according to any of the preceding claims, wherein said step (e) is carried out in a third treatment tank containing at least a gold plating bath solution, potassium gold cyanide, palladium ions and nickel ions.

25. A method according to Claim 24, wherein said third treatment tank contains gold plating bath solution at a concentration of substantially 100 millitres per litre.

26. A method according to Claim 24 or 25, wherein said third treatment tank contains potassium gold cyanide at a concentration of substantially 0.8 grams per litre.

27. A method according to any one of Claims 24 to 26, wherein said third treatment tank contains palladium ions at a concentration of substantially 3 grams per litre.

28. A method according to any one of Claims 24 to 27, wherein said third treatment tank

contains nickel ions at a concentration of substantially 4.6 grams per litre.

29. A method according to any of the preceding claims, wherein said step (e) is carried out for substantially 2 hours.

30. A method according to any of the preceding claims, wherein said step (e) is carried out at a temperature of 0 °C to 95 °C.

31. A method according to any of the preceding claims, wherein, in said step (e), said layer of nickel is deposited on said layer of copper and said layer of gold is deposited on said layer of nickel.

32. A method according to any of the preceding claims, wherein said step (e) is carried out by electroless nickel immersion gold.

33. A method of forming an integrated circuit (IC) card, including steps:

(k) manufacturing an integrated circuit (IC) card circuit board substrate according to Claim 1,

(l) fixedly securing an IC module with said substrate, and

(m) electrically connecting said IC module with said electric circuit on said at least one of said major surfaces of said substrate.

34. A method according to Claim 33, wherein said step (l) is carried out by flip flop bonding.

35. A method according to Claim 33, wherein said step (l) is carried out by wire bonding.

36. A method according to any one of Claims 33 to 35 wherein said IC card is a SIM card.

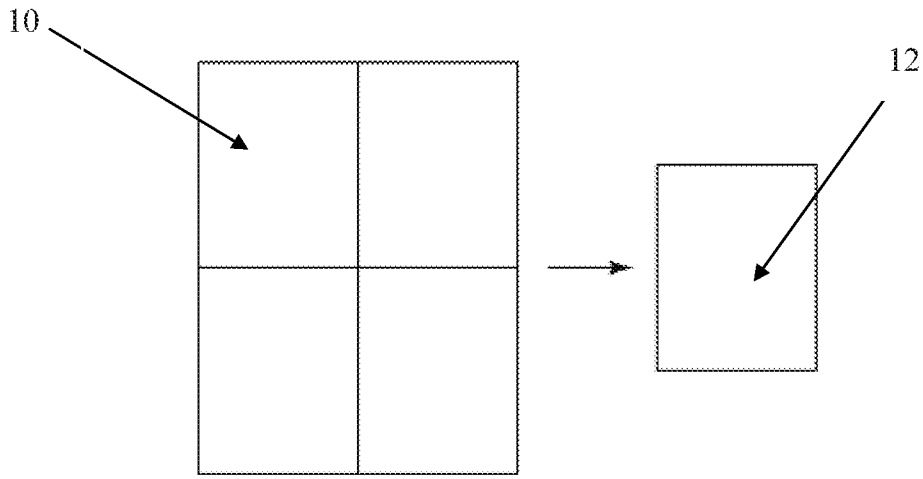

Fig. 1

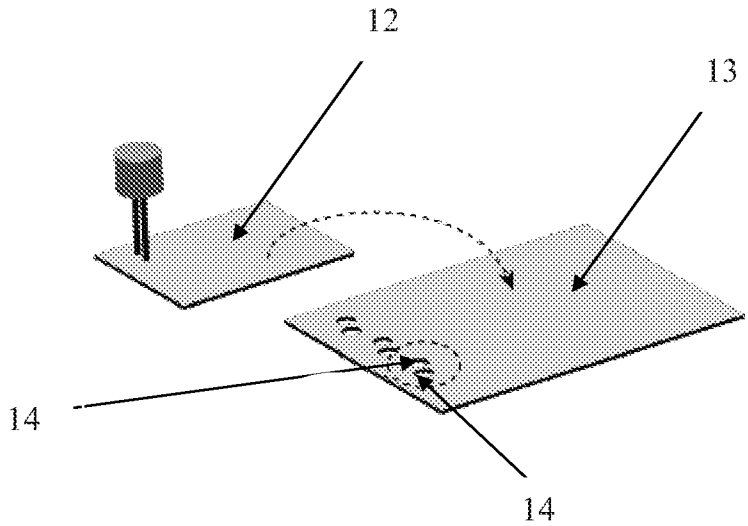

Fig. 2

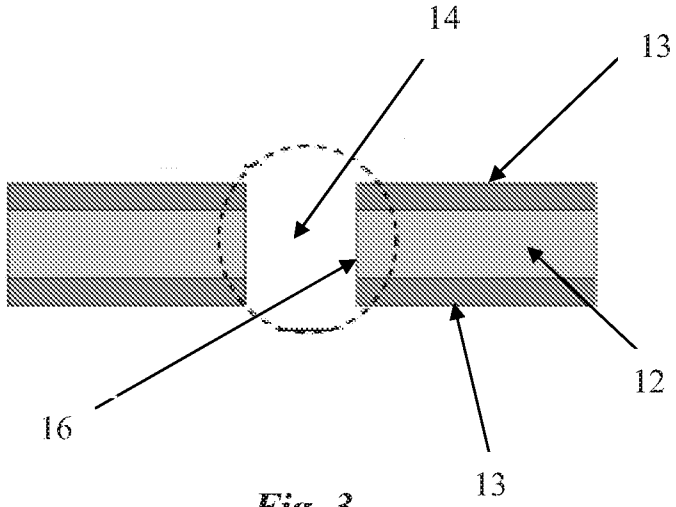

Fig. 3

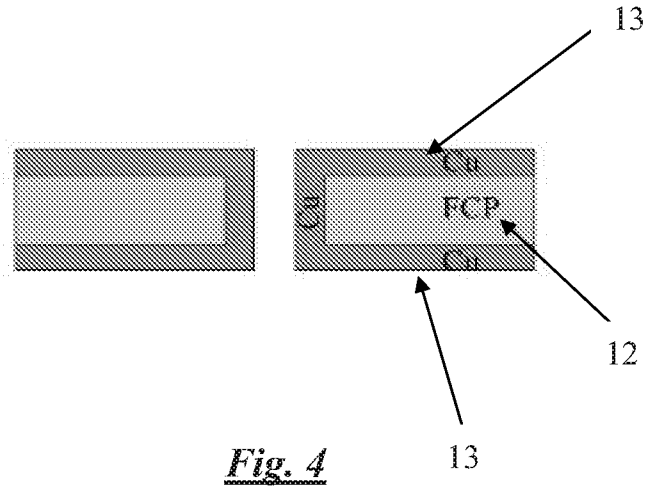

Fig. 4

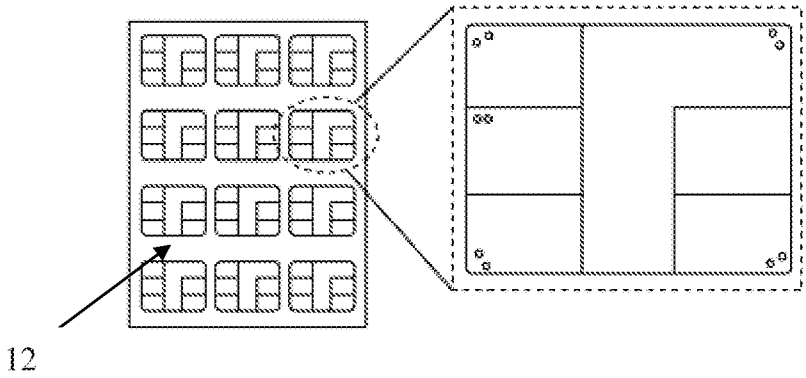

Fig. 5

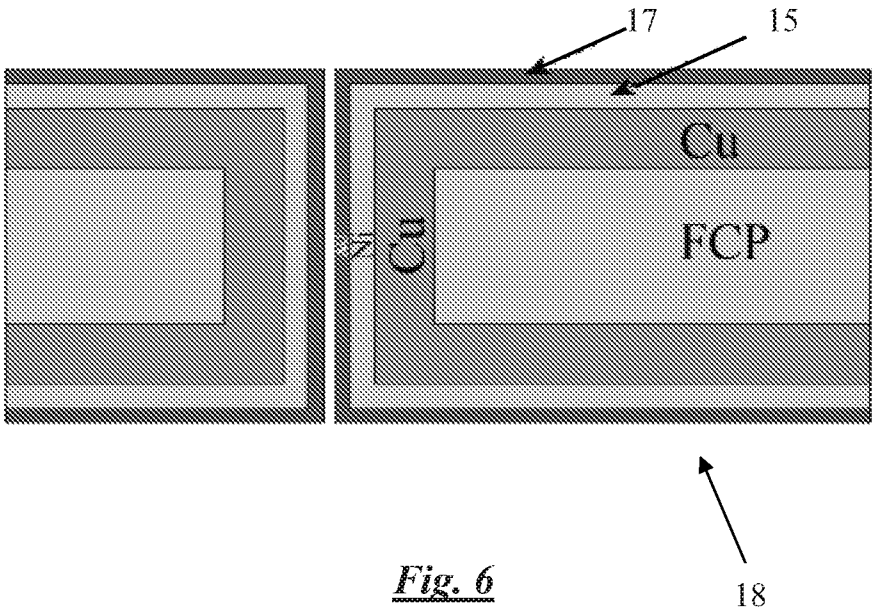

Fig. 6

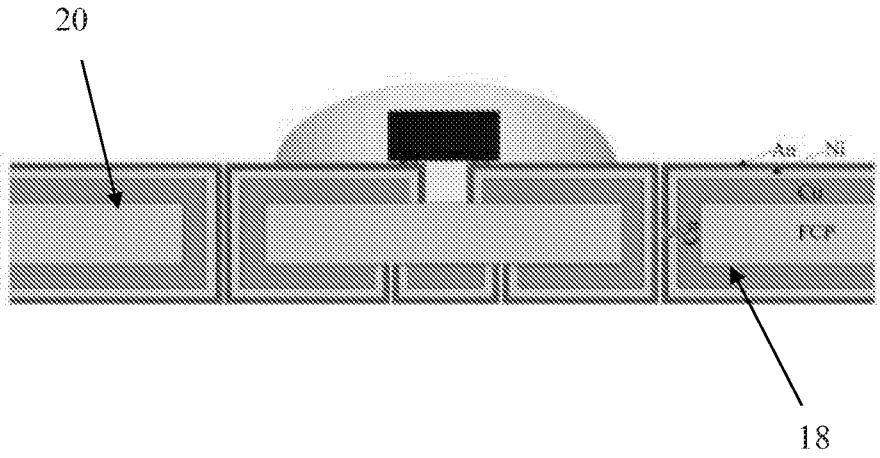

Fig. 7

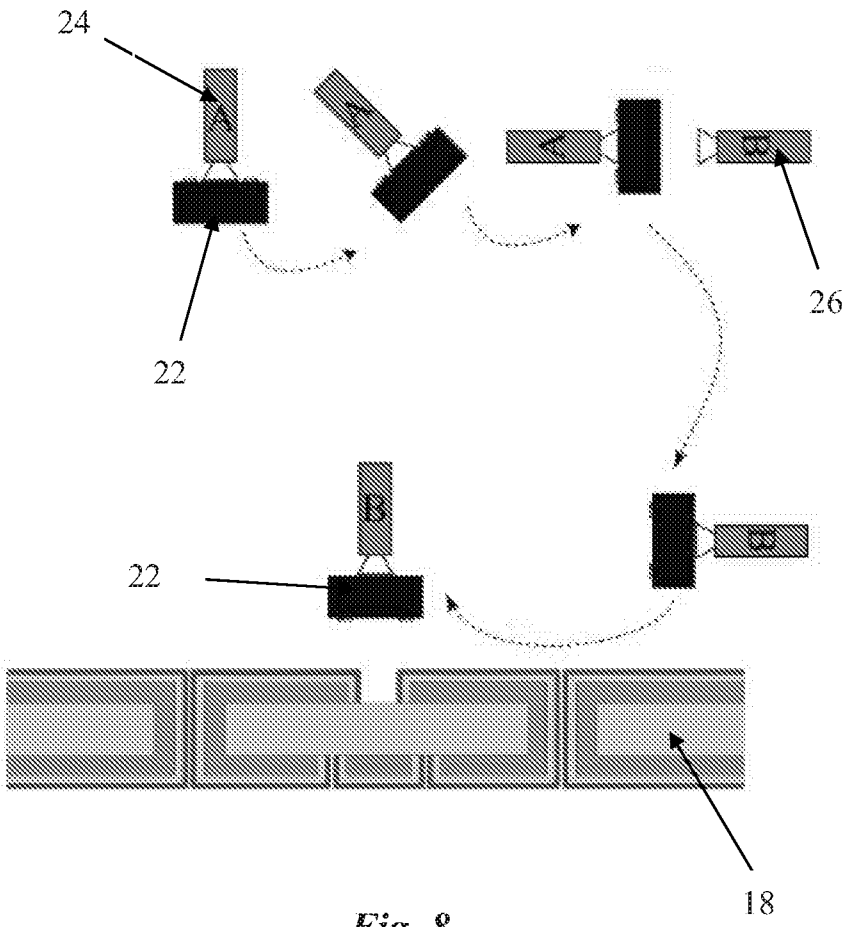

Fig. 8

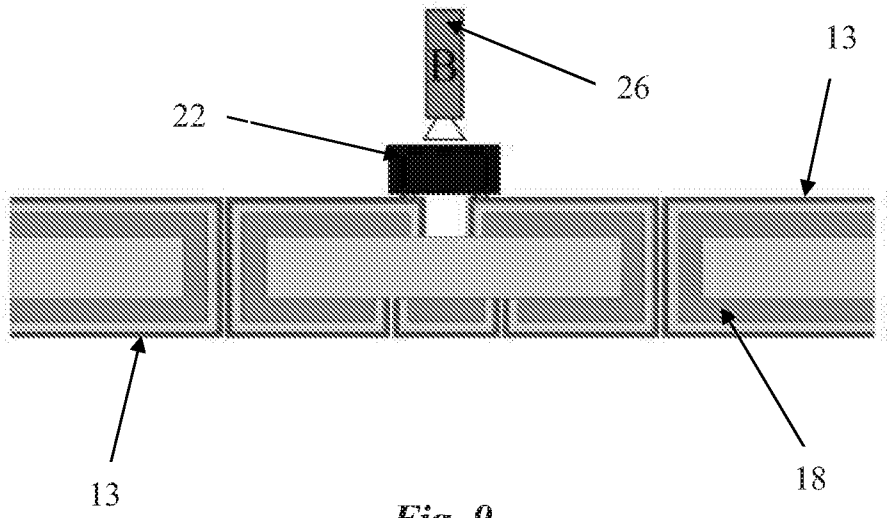

Fig. 9

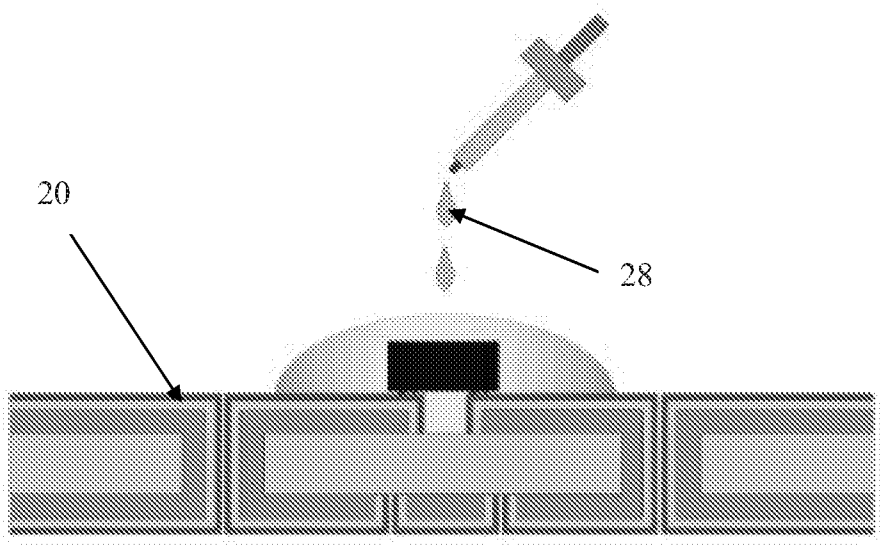

Fig. 10

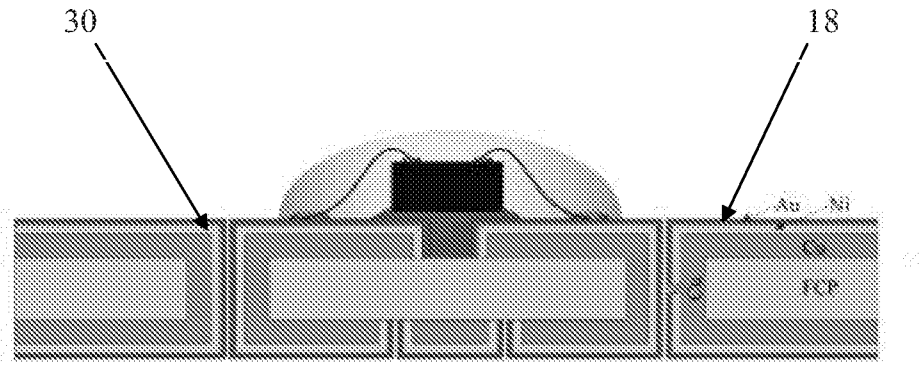

Fig. 11

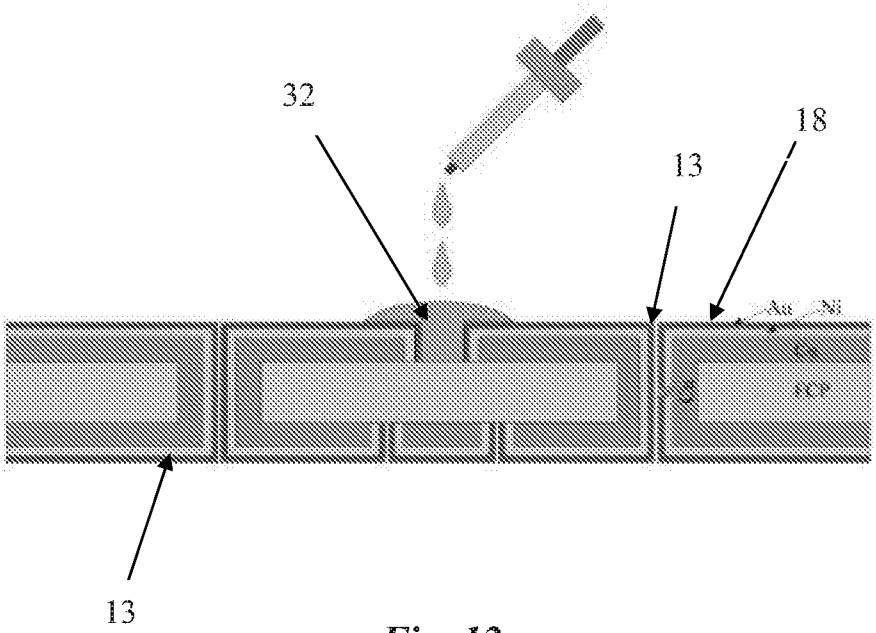

Fig. 12

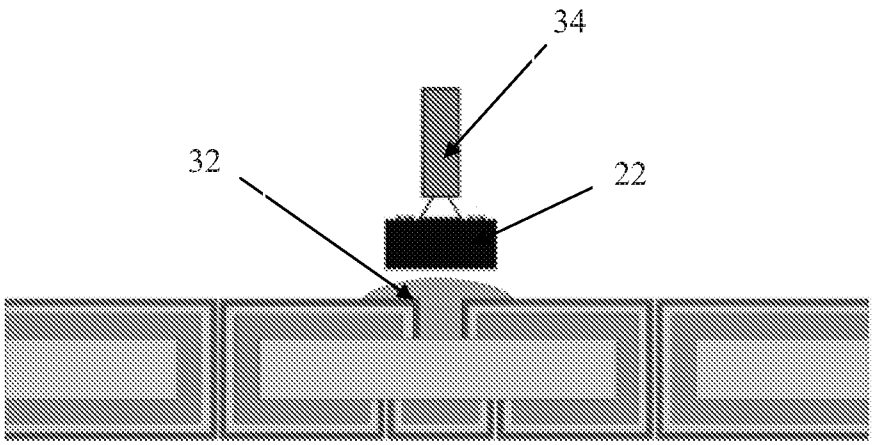

Fig. 13

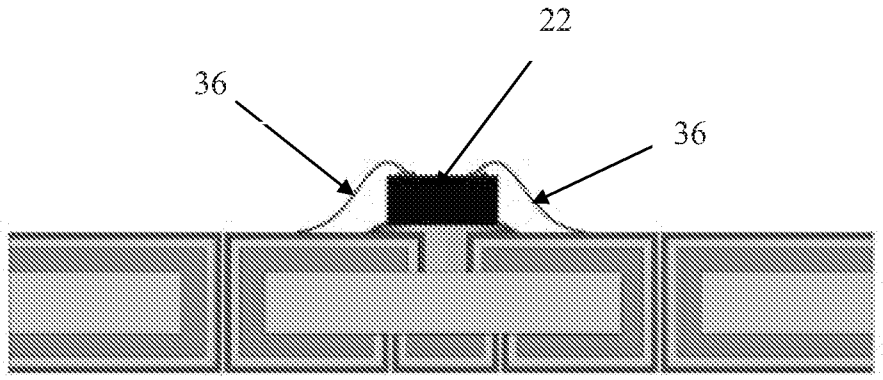

Fig. 14

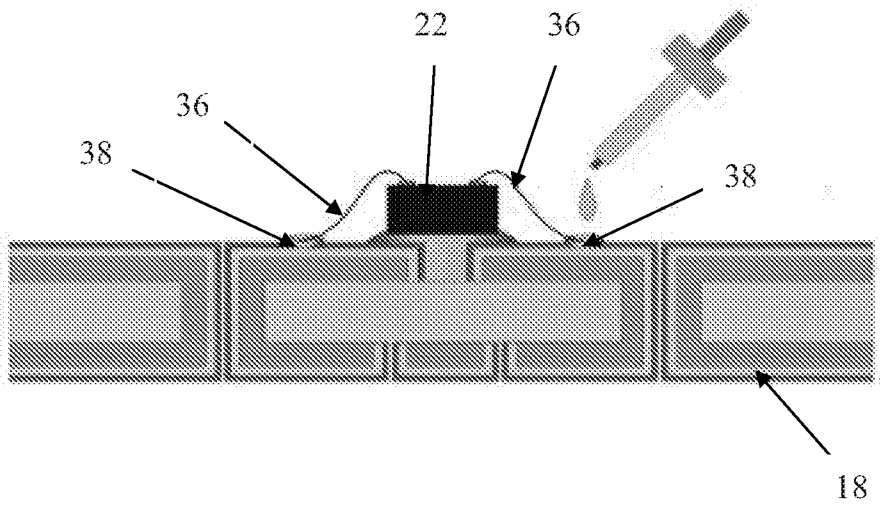

Fig. 15

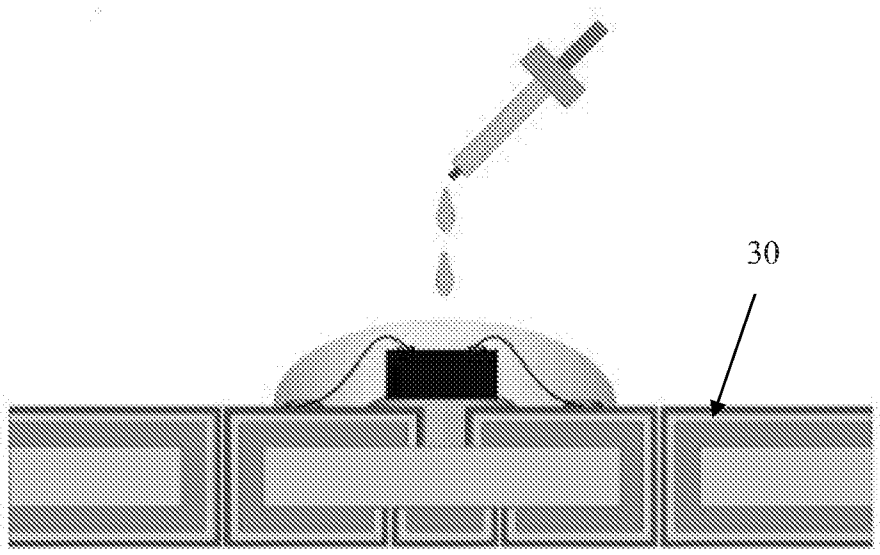

Fig. 16

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2017/101735

A. CLASSIFICATION OF SUBJECT MATTER

H05K 3/42(2006.01)i; H05K 1/18(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H05K; H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, WPI, EPODOC, CNKI, IEEE: through hole?, via?, card, IC, integrated circuit, module, mount+, secur+, sodium hydroxide, NaOH, formaldehyde, Pd, palladium, brightener, Cu, copper, tin, Sn, chloride, sulfate, sulfuric

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007045826 A1 (MICRON TECHNOLOGY, INC.) 01 March 2007 (2007-03-01) description, paragraphs [0013]-[0028] and figures 1-5	1-36
Y	US 5252383 A (JAPAN GORE-TEX, INC.) 12 October 1993 (1993-10-12) description, column 14, lines 3-22	1-36
Y	US 7993510 B2 (IBIDEN CO., LTD.) 09 August 2011 (2011-08-09) claim 1	13-23
Y	CN 103531485 A (XUDE TECHNOLOGY CO., LTD.) 22 January 2014 (2014-01-22) description, paragraphs [0031]-[0036] and figures 1A-1E	1-36
Y	US 2009107711 A1 (IBIDEN CO., LTD.) 30 April 2009 (2009-04-30) description, paragraphs [0070]-[0071]	13-23
A	EP 1249787 A1 (TOSHIBA K.K.) 16 October 2002 (2002-10-16) the whole document	1-36
A	JP 2002123809 A (DAINIPPON PRINTING CO., LTD.) 26 April 2002 (2002-04-26) the whole document	1-36

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
02 June 2018	**15 June 2018**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**HAN,Bing**
Facsimile No. **(86-10)62019451**	Telephone No. **86-(10)-53961217**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2007045826 A1	01 March 2007	US 2010052183 A1	04 March 2010
		US 7622377 B2	24 November 2009
		WO 2007027968 A2	08 March 2007
		SG 130075 A1	20 March 2007
US 5252383 A	12 October 1993	JP H0513951 A	22 January 1993
		EP 0521483 A2	07 January 1993
		JP 3218542 B2	15 October 2001
		EP 0521483 A3	05 January 1994
		DE 69223692 T2	23 July 1998
		EP 0521483 B1	29 December 1997
		DE 69223692 D1	05 February 1998
US 7993510 B2	09 August 2011	EP 1207730 B1	16 September 2009
		DE 60045566 D1	03 March 2011
		US 2004226745 A1	18 November 2004
		US 7514637 B1	07 April 2009
		DE 60042976 D1	29 October 2009
		US 7446263 B2	04 November 2008
		WO 0111932 A1	15 February 2001
		EP 2111087 B1	19 January 2011
		US 2005211561 A1	29 September 2005
		EP 1207730 A1	22 May 2002
		EP 1207730 A4	02 August 2006
		US 2008230263 A1	25 September 2008
		EP 2111087 A3	31 March 2010
		EP 2111087 A2	21 October 2009
		US 7812262 B2	12 October 2010
		PH 1200101296 B1	05 November 2009
		PH 1200700070 B1	19 November 2010
		JP 2002050868 A	15 February 2002
		JP 4480236 B2	16 June 2010
		JP 2002047594 A	15 February 2002
CN 103531485 A	22 January 2014	TW I442852 B	21 June 2014
		TW 201404264 A	16 January 2014
		CN 103531485 B	21 December 2016
		US 2014000109 A1	02 January 2014
		US 8973258 B2	10 March 2015
US 2009107711 A1	30 April 2009	US 2012005888 A1	12 January 2012
		US 8383956 B2	26 February 2013
		JP WO2006033315 A1	15 May 2008
		TW 200619437 A	16 June 2006
		US 2009107847 A1	30 April 2009
		US 7897027 B2	01 March 2011
		TW I391539 B	01 April 2013
		US 8197659 B2	12 June 2012
		CN 101027431 A	29 August 2007
		JP 4992428 B2	08 August 2012
		CN 101027431 B	13 April 2011
		US 7481909 B2	27 January 2009
		US 2006065534 A1	30 March 2006

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2017/101735

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
		WO 2006033315 A1	30 March 2006
		KR 100907841 B1	14 July 2009
		KR 20070045349 A	02 May 2007
EP 1249787 A1	16 October 2002	JP 2002312746 A	25 October 2002
JP 2002123809 A	26 April 2002	None	