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**EUROPEAN PATENT APPLICATION**

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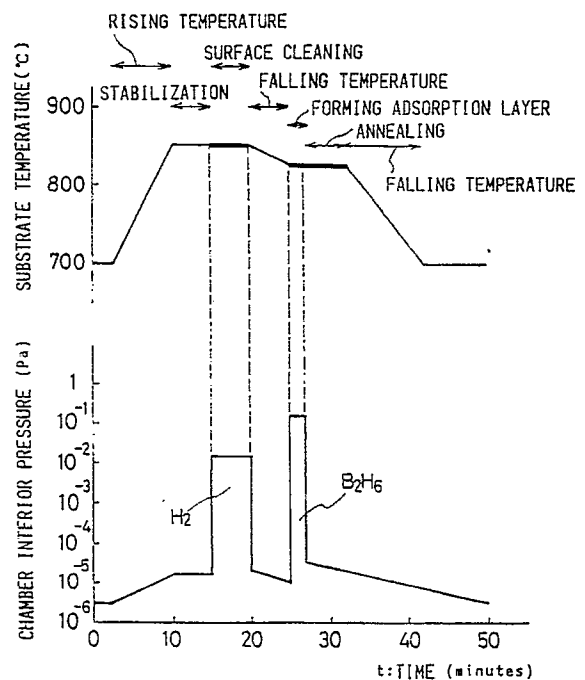
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**Method of producing semiconductor device.**

An impurity adsorption layer is formed on a substrate surface and solid-phase thermal diffusion is carried out to form source and drain regions of the metal-insulator-semiconductor field-effect-transistor having lightly doped drain structure or double doped drain structure. The thus formed impurity-doped region is ultrashallow, thereby producing fast and micro semiconductor devices.

**FIG. 2**



**EP 0 417 456 A3**



DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP-A-0 322 921 (FUJITSU LTD) * Figure 7; page 5, line 55 - page 6, line 24 *	1,2,4	H 01 L 21/225 H 01 L 21/336
A	---	7	
A	JOURNAL OF APPLIED PHYSICS, vol. 65, no. 11, 1st June 1989, pages 4435-4437, American Institute of Physics, New York, US; S.F. GONG et al.: "A metal-oxide-silicon field-effect transistor made by means of solid-phase doping" * Page 4435 *	1,3,5-7,9-11	
A	EXTENDED ABSTRACTS/SPRING MEETING, vol. 88-1, 15th - 20th May 1988, pages 301-302, abstract no. 193, Princeton, NY, US; T. MAKINO et al.: "A stacked-source-drain-MOSFET using selective epitaxy" * Whole document *	1,5	
A	NIKKEI HIGH TECH REPORT, vol. 4, no. 7, 13th February 1989, page 10, Tokyo, JP; "UV epitaxy applied to make transistor" * Whole document *	1,5-7,9,10	H 01 L
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
Place of search	Date of completion of the search	Examiner	
THE HAGUE	27-03-1991	GELEBART J. F. M.	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ..... & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

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### CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.
- Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid,  
namely claims:
- No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

### X LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions,  
namely:

See sheet -B-

- All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid,  
namely claims:
- None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims,  
namely claims:



**LACK OF UNITY OF INVENTION**

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1,2,4: A method of manufacturing a semiconductor device where first, the lightly doped regions are formed by diffusion from an adsorbed dopant layer and then, the highly doped regions are formed by ion implantation.
2. Claim 3: A method of manufacturing a semiconductor device where first, the lightly doped regions are formed by diffusion from an adsorbed dopant layer and then, the highly doped regions are formed by diffusion from another adsorbed dopant layer.
3. Claim 5: A method of manufacturing a semiconductor device where the lightly doped regions are formed by diffusion from an in-situ doped deposited semiconductor layer.
4. Claim 6: A method of manufacturing a semiconductor device where the lightly doped regions are formed by diffusion from alternated layers of adsorbed dopant and epitaxial semiconductor material.
5. Claims 7-12: A method of manufacturing a semiconductor device where first, the lightly doped regions are formed by ion implantation and then, highly doped regions are formed by diffusion.

CAVEAT: A further lack of unity a posteriori could be raised when searching the fifth invention (claims 7-12).