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(54) Title: LOW-POWER STATIC RANDOM ACCESS MEMORY

FIG. 2a

(57) Abstract: A low-power static random access memory (SRAM) is set forth which includes a cache memory function without requiring a special bit cell, and which realizes robust read and write operation without any write assist circuit at 16nm or below FinFET technology. The SRAM comprises a half-Vdd precharge 6T SRAM cell array for robust operation at low supply voltage at 16nm or below, and with cacheable dynamic flip-flop based differential amplifier referred to as a main amplifier (MA). Prior art 6T SRAM cell arrays use Vdd or Vdd-Vth precharge schemes, and have separate read and write amplifiers. The SRAM set forth uses one main amplifier only, which is connected to the bit line (BL) through a transmission gate. The main amplifiers functions as a read amplifier, write amplifier, and a cache memory.

WO 2022/269492 A1

LOW-POWER STATIC RANDOM ACCESS MEMORY

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application is related to and claims priority to United States Patent Application 63/213393, filed June 22, 2021, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention is directed to static random access memory (hereinafter SRAM), and more particularly to SRAM operable in multiple different voltage domains.

2. Description of the Related Art

[0003] There has been an ever-increasing need to reduce power dissipation in traditional SRAMs (e.g. Vdd supply voltage of 0.5 V or less), wherein a plurality of memory cells (hereinafter MCs) along a selected word-line (hereinafter WL) are simultaneously read or written, while the rest, referred to as half-select MCs, are virtually read or written. Recently, this need has become more pressing with the introduction of emerging SRAMs used in AI-chips, wherein all of the MCs are simultaneously read or written for massively parallel operations between processor element blocks and the SRAMs.

[0004] Indeed, semiconductor foundries provide 0.5V as the core voltage for 16nm FinFET technology. However, the SRAM operation voltage is higher than the core voltage, (e.g. 0.8V for 16nm FinFET technology) giving rise to the use of write assist circuitry (see Y.H. Chen et al., "A 16 nm 128 Mb SRAM in High- Metal-Gate FinFET Technology With Write-Assist Circuitry for Low-VMIN Applications," IEEE Journal Of Solid-State Circuits,Vol.50, No.1, January 2015).

[0005] Additional prior art relevant to this disclosure includes: K. Ishibashi and K. Osada editors, "Low Power and Reliable SRAM Memory Cell and Array Design," Springer Series in Advanced Microelectronics 3, April 2011, and GeeksforGeeks; Cache Memory in Computer Organization.

SUMMARY OF THE INVENTION

[0006] According to aspects of this specification, a method and apparatus are set forth for operating SRAM under two different voltage domains, such as 0.5V and 0.8V for 16nm FinFET technology, without any requirement for special circuitry such as write assist circuitry, which requires a negative voltage for a zero data write.

[0007] It is an aspect of the present invention to provide a static random-access memory comprising at least one six-transistor memory cell arranged between a first bitline, a second bitline and a word line; a bitline precharge circuit for precharging the first bitline and second bitline to a voltage of Vdd/2 prior to the at least one six-transistor memory cell receiving a word line signal; a main amplifier for receiving signals on data lines din and /din in a first voltage domain via a gate WEi; and a main amplifier precharge circuit for precharging the main amplifier in response to a signal /PEMA such that the main amplifier amplifies signals in the first voltage domain to a second domain.

[0008] The above aspects can be attained by a circuit for generating a half Vdd voltage from a main on-chip supply voltage Vdd/Vss comprising series connected transistors M1 and M2 in parallel with series connected transistors M3 and M4, connected between Vdd and Vss, with the half Vdd voltage output from a node connecting transistors M1, M2, M3 and M4, wherein transistors M1 and M3 function as a self-biased inverter and transistors M2 and M4 function as current sensing transistors.

[0009] These together with other aspects and advantages which will be subsequently apparent, reside in the details of construction and operation as more fully hereinafter described and claimed, reference being had to the accompanying drawings forming a part hereof, wherein like numerals refer to like parts throughout.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Fig. 1a shows a SRAM cell array according to the prior art.

[0011] Fig. 1b shows column precharge multiplexer and sense/write amplifiers of the prior art SRAM cell array depicted in Fig. 1a.

[0012] Figs. 2a and 2b show embodiments of circuits for writing to an MC without a level shifter.

[0013] Fig. 2c shows an exemplary precharge circuit for the circuits of Figs. 2a and 2b.

[0014] Fig. 2d is a timing diagram for the signals for the circuits in Figs.2a, 2b and 2c.

[0015] Fig. 3 is a simplified block diagram of a prior art memory system having a primary memory and cache memory.

[0016] Fig. 4 illustrates use of the circuits of Figs. 2a and 2b for the cache memory of Fig. 3 connected to a deep learning processing element (DPE) of an AI system.

[0017] Fig. 5 shows signals for performing a write mask, according to an embodiment.

[0018] Fig. 6a illustrates an 8b-DPE having 32 columns, and Fig. 6b shows a detail of Fig. 6a, according to an embodiment.

[0019] Fig. 7 shows circuitry applied to four main amplifiers (MAs) in Fig. 6b for performing a write mask.

[0020] Fig. 8 shows circuitry for performing a data inversion utilizing charge shared level comparison with half Vdd when the 32 column 8b-DPE of Fig. 6a is operating as a read cache.

[0021] Fig 9a. shows an alternate circuit for generating the half Vdd voltage, Fig. 9b is an equivalent circuit thereof and Fig. 9c is a resistance circuit thereof be simplified using small signal analysis.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022] A conventional SRAM cell array is shown in Fig. 1a, comprising a plurality of SRAM cells $MC_{1,1}$...$MC_{1,m}$...$MC_{n,1}$...$MC_{n,m}$, to which binary data (dout, din) is read/written on BLs BT<0>/BB<0> ... BT<m-1>/BB<m-1> via column precharge, multiplexers (column mux), and sense/write amplifiers ((S.A.) and W.A., respectively), in response to read/write signals on word lines WL<0>...WL<n-1>. The structures of the conventional column precharge multiplexer, column multiplexer and sense/write amplifiers are depicted in Fig. 1b.

[0023] In Figs. 1a and 1b, only one voltage domain is used for the column precharge multiplexer and sense/write amplifiers, namely Vdd. However, in the event the logic that

generates din and receives dout operates in a different voltage domain (e.g. if the logic operates at 0.4V and the SRAM operates at 0.8V for 16nm FinFET technology), a level shifter is required to convert the voltage from 0.4V to 0.8V before din is input to the W.A., because W.A. operates at 0.8V. A disadvantage of using such a level shifter is that it consumes considerable power and surface layout area.

[0024] According to exemplary embodiments, circuits for writing to an MC without a level shifter are shown in Figs. 2a and 2b. In Fig. 2a, din and /din are received from external logic in a first voltage domain (e.g. din = 0.4V and /din = 0 V) and are applied to a main amplifier (MA) via a gate WEi. After WEi turns off, MA amplifies the 0.4V and 0V signals in the first voltage domain to 0.8V and 0V, respectively, as shown in Fig. 2d. GBL and /GBL are connected to BL and /BL, respectively, through transmission switches controlled by YL and /YL gate signals. A bitline precharge circuit is enabled by signal $/PE_{BL}$, and a main amplifier precharge circuit is enabled by signal $/PE_{MA}$. The MA in Figs. 2a and 2b therefore functions as a write amplifier that includes level shifting functionality.

[0025] In the embodiment of Fig. 2b, only din is received from the external logic. The complementary signal (/din) is generated by an inverter that is operated at 0.4V. After /din is generated, din and /din are amplified by MA and sent to BL and /BL, in the same way as the embodiment of Fig. 2a.

[0026] An embodiment of the precharge circuit in Figs. 2a and 2b, is shown in Fig. 2c.

[0027] In the case of a data read, the read data passes from the MC to MA through the transmission gates upon application of gate control signals YL and /YL, and is amplified by MA for output as dout, which is level shifted to the 0.4V domain via an output inverter, as shown in Figs. 2a and 2b.

[0028] In the simplified prior art memory system shown in the block diagram of Fig. 3, a CPU communicates with cache memory and a primary memory, where the cache memory stores a portion of the data of the primary memory, and is commonly referred to as the cache line. In a single die (i.e. one chip), each of the cache memory and primary memory are SRAM. In Fig. 3, the CPU communicates with the cache memory and

primary memory over different bit line (BL) and global bit line (GBL) busses. The bus configuration and control in such a memory system can become complicated and consume layout area.

[0029] Therefore, as shown in Fig. 4, the MA of Figs. 2a and 2b can be used for the cache memory of Fig. 3 (i.e. MA_{00}...MA_{17}), where each bitline BLi and complementary bitline /BLi are connected to a respective SRAM MC (Figs. 2a and 2b) and accessed via a WL that corresponds to the cache line in the memory system of Fig. 3. As discussed above, in emerging memories such as AI systems, all the MCs along a selected WL are simultaneously read or written (for example from/to a Deep-learning Processing Element (DPE)). Thus, when operating as a write cache, write data is latched into the MA through the WEi transmission gate. Before each write, MA is reset or precharged by $/PE_{MA}$ (see Fig. 2c) and then write data is input to MA through the WEi gate, and finally the write data is amplified by MA in response to enable signals MEi and /MEi. If the data needs to be written to the SRAM MC as well (i.e. a write-through cache), the write data amplified by MA is transferred to MC via the transmission gates upon receipt of the gate control signals YL and /YL and enabling the word line (WL). The MA cache retains the write data until it is next accessed.

[0030] When operating as a read cache, the read signal from the MC is applied to MA through transmission gates controlled by YL and /YL, and is amplified by MA as in conventional SRAM. Once MA amplifies the signal by application of the ME and /ME signals, it retains the data until the MA is next accessed. In order to keep MA active, the bit line precharge signal, $/PE_{BL}$ is separate from the MA precharge signal, $/PE_{MA}$, and the GBL and /GBL lines are separated from BL and /BL by the transmission gates controlled by YL and /YL.

[0031] Fig. 5 shows signals for performing a write mask, according to an embodiment, wherein MA_{02} and MA_{05} of Fig. 4 hold data (GBL_{02}, $/GBL_{02}$, GBL_{05}, $/GBL_{05}$) as a cache memory. Each DPE_0/DPE_1 shown in Fig. 4 writes/reads eight bits din and dout (8b-DPE) via eight MAs (MA_{00} ~ MA_{07}), although in embodiments din and dout of a DPE and the number of MAs per DPE need not be restricted in number to eight. In normal write

cache mode of operation, each MA must be written to. Before the MA is written to, the MA holds data as a cache memory. When the MA cache is renewed, GBL and /GBL are first reset by the $/PE_{MA}$ signal. Then, the write data (in the 0.4V voltage domain), is written into MA through the WE control transistor. After that, ME activates MA to amplify the write data to the 0.8V voltage domain. In the case of a write mask, some of the MAs are not renewed or not written in write cache mode. For example, if MA_{02} and MA_{05} are to be masked, then MA_{00}, MA_{01}, MA_{03}, MA_{04}, MA_{06} and MA_{07} are renewed or written with new data, while MA_{02} and MA_{05} retain the previous data. To realize the write mask, signals, WE, $/PE_{MA}$, ME, /ME, are divided into eight signals corresponding to each MA, that is WE_{00}~WE_{07}, $/PE_{MA00}$~$/PE_{MA07}$, ME_{00}~ME_{07}, and $/ME_{00}$~$/ME_{07}$. In the case where MA_{02} and MA_{05} are masked, WE_{02}, WE_{05}, $/PE_{MA02}$, $/PE_{MA05}$, ME_{02}, ME_{05}, $/ME_{02}$, and $/ME_{05}$ are not asserted so that MA_{02} and MA_{05} retain the previous data. The held data in MA_{02} and MA_{05} can then be re-written into the bit cell when the transmission gate controlled by YL and /YL is activated.

[0032] In some embodiments, for example in an AI chip, the layout area of the 8b-DPE can be widened to 32 columns width or 32 MAs width, as shown in Fig. 6a, where an 8b-DPE is connected to 8 MAs with one MA selected from every four MAs and eight MAs selected and connected to one 8b-DPE, for 32 MAs in total. However, as discussed above, embodiments are not restricted to 8b-DPE, but are applicable to Nb-DPE, where N can be 4, 8, 16, and so on. Fig. 6b shows a detail of Fig. 6a for four MAs (MA_0, MA_1, MA_2, MA_3), according to an embodiment.

[0033] Fig. 7 shows circuitry applied to the four MAs (MA_0, MA_1, MA_2, MA_3) of Fig. 6b for performing a write mask, where the write mask is applied to only one MA in each four-MA group. Two write data path are provided, that is, a regular din path which is input to the MA in normal mode where Write Mask Enable (WME) is not asserted, and a data path where WME is asserted. When WME is asserted (i.e. for write mask mode), the regular din path is closed, and data from the data latch is input into MA through the WME asserted transmission gate. The latched data is the read cache data held from the previous cycle. The latch holds data when ME turns off and the read cache is reset or the mask write cycle starts. The masked MA writes the previous data which has been

held in the MA cache, using the latch data, so that the masked MA retains the read cache data during write cache mode. In this circuit, mask flexibility is limited to only one MA, however, only one $/PE_{MA}$, four WE, four ME, and four /ME are needed, which is simpler compared to the circuit of Fig. 4 in which all eight WE, /PE, ME, /ME signals are needed for each.

[0034] As discussed above, when operating as a read cache, where the MA retains data until the MA is next accessed, the dout swing power can be reduced by inverting the dout data by utilizing a half Vdd voltage, as shown in the embodiment of Fig. 8, where each dout charges up capacitance C_0 according to the S0 signal timing, and then each capacitance is shorted according to the S1 signal timing. At this stage, if the majority of the data on the dout lines is high (i.e. Vdd level), the charge is shared, and the shorted voltage will be larger than half Vdd. The shorted voltage is compared with half Vdd by the MA, and the resulting dout of the MA is selectively inverted by application of signals, sel and /sel which control respective gates to select either normal data or inverted data. Conventionally, if a majority of five out of eight dout lines is high, a combination of 8C5 =57 logic gates is required, whereas the circuit of Fig. 8 using charge sharing and half Vdd comparison results in a much simplified circuit.

[0035] Fig 9a. shows an alternate circuit for generating the half Vdd voltage for the precharge circuit of Fig. 2c, from the main on-chip supply voltage and for tracking changes in the main voltage supply with a minimum number of transistors so that it occupies minimal space on the chip. In the circuit of Fig. 9a, devices M1 and M3 comprise a self-biased inverter and devices M2 and M4 are current sensing devices that are always turned on. An equivalent circuit of Fig. 9a is shown in Fig. 9b, which can be simplified using small signal analysis to a resistance circuit as shown in Fig. 9c. The equivalent resistance can be calculated as follows:

$$R_{e1} = \frac{r_2 r_3}{r_2 + r_3} \tag{1}$$

$$R_{e1} = \frac{1}{r_2} + \frac{1}{r_3} \tag{2}$$

$$\frac{1}{R_{e1}} = gm_2 + gds_3 \tag{3}$$

[0036] Therefore, Re1 is

$$R_{e1} = \frac{1}{gm_2 + gds_3} \tag{4}$$

[0037] Re2 can be calculated as

$$R_{e2} = \frac{r_1 r_4}{r_1 + r_4} \tag{5}$$

$$\frac{1}{R_{e2}} = \frac{1}{r_1} + \frac{1}{r_4} \tag{6}$$

$$\frac{1}{R_{e2}} = gds_1 + gm_4 \tag{7}$$

$$R_{e2} = \frac{1}{gds_1 + gm_4} \tag{8}$$

[0038] Therefore, Vout is

$$Vout = VDD\frac{gds_1 + gm_4}{gds_1 + gm_4 + gm_2 + gds_3} \tag{11}$$

[0039] The output impedance is therefore

$$Rout = (\frac{1}{gm_1})||(\frac{1}{gm_2})||(\frac{1}{gm_3})||(\frac{1}{gm_4}) \tag{12}$$

[0040] From the foregoing it will be noted that the circuit of Fig. 9a tracks the change in the main supply voltage and replicates the change at the output.

[0041] In terms of DC analysis, the sum of the currents through M2 and M3 = the sum of currents through M1 and M4. Therefore

$$I_2 + I_3 = I_1 + I_4 \quad (13)$$

$$I_n = (\frac{1}{2})\mu_n Cox(\frac{W}{L})(V_{gs} - V_{th})^2 \quad (14)$$

$$I_p = (\frac{1}{2})\mu_p Cox(\frac{W}{L})(V_{sg} - |V_{thp}|)^2 \quad (15)$$

[0042] For equal impedance seen through NMOS and PMOS

$$\mu_n Cox(\frac{W}{L})_{1,2} = \mu_p Cox(\frac{W}{L})_{3,4} \quad (16)$$

[0043] Therefore

$$(V_{DD} - V_O - V_{th2})^2 + (V_{DD} - V_O - |V_{thp3}|)^2 = (V_O - V_{th1})^2 + (V_O - |V_{thp4}|)^2 \quad (17)$$

[0044] If

$$V_{th2} = |V_{thp3}| = V_{th1} = |V_{thp4}| \quad (18)$$

[0045] Then neglecting body effect,

$$V_O = \frac{V_{DD}}{2} \quad (19)$$

[0046] The many features and advantages of the invention are apparent from the detailed specification and, thus, it is intended by the appended claims to cover all such features and advantages of the invention that fall within the true spirit and scope of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation illustrated and described, and accordingly all suitable modifications and equivalents may be resorted to, falling within the scope of the invention.

What is claimed is:

1. A static random-access memory comprising:

at least one six-transistor memory cell arranged between a first bitline, a second bitline and a word line;

a bitline precharge circuit for precharging the first bitline and second bitline to a voltage of Vdd/2 prior to the at least one six-transistor memory cell receiving a word line signal;

a main amplifier for receiving signals on data lines din and /din in a first voltage domain via a gate WEi; and

a main amplifier precharge circuit for precharging the main amplifier in response to a signal $/PE_{MA}$ such that the main amplifier amplifies signals in the first voltage domain to a second domain.

2. The static random-access memory of claim 1, wherein the first voltage domain is din = 0.4V and /din = 0 V and the second voltage domain is din = 0.8V and /din = 0 V.

3. The static random-access memory of claim 1, further comprising a pair of transmission gates for connecting the first bitline and second bitline to global bit line busses GBL and /GBL, respectively, in response to YL and /YL gate signals, respectively.

4. The static random-access memory of claim 3, wherein the main amplifier precharge circuit precharges the global bit line busses GBL and /GBL before the main amplifier receives signals on data lines din and /din and independently of the bitline precharge circuit precharging the first bitline and second bitline.

5. The static random-access memory of claim 1, wherein the main amplifier functions as a write amplifier for amplifying a ower voltage on din to higher write voltage for writing to the at least one six-transistor memory cell.

6. The static random-access memory of claim 4 wherein a plurality of six-transistor memory cells along a selected word line are simultaneously read or written, wherein the main amplifier also functions as a cache memory.

7. The static random-access memory of claim 6, wherein the main amplifier amplifies read data on data line dout from the at least one six-transistor memory cell when accessed, and retains the data until the main amplifier is subsequently accessed.

8. The static random-access memory of claim 6, wherein the main amplifier retains write data when accessed until the main amplifier is subsequently accessed again.

9. The static random-access memory of claim 4, wherein the main amplifier is controlled by a write signal sequence of main amplifier precharge triggered by signal $/PE_{MA}$, then writing data into the main amplifier triggered by enable signals ME and /ME, followed by the first bitline and second bitline being connected to the global bit line busses GBL and /GBL causing the main amplifier to operate as a write amplifier.

10. The static random-access memory of claim 6, wherein enable signals ME and /ME are asserted in either standby or active modes and signal $/PE_{MA}$ is asserted before the main amplifier starts reset, such that the main amplifier operates as a cache amplifier.

11. The static random-access memory of claim 8, for use in a N-bit deep learning processing element (DPE) of an AI system, wherein signals $/PE_{MA}$, WE, ME, and /ME are decoded by N and a plurality of which are asserted to turn on the main amplifier for write masked operation.

12. A cache memory connected to an 8-bit deep learning processing element (DPE) having 32 columns of main amplifiers each according to the main amplifier claim 6, wherein one main amplifier of four is selected.

13. A cache memory connected to a 4-bit deep learning processing element (DPE) having 16 columns of main amplifiers each according to the main amplifier claim 6, wherein one main amplifier of four is selected.

14. The cache memory of claim 12, wherein data written to the main amplifier is selected either from din or latched data depending on assertion of a write mask enable signal WME.

15. The cache memory of claim 14, wherein one latch is provided every four main amplifiers for latching read data of one of the four main amplifiers when an enable signal is de-asserted.

16. The static random-access memory of claim 6, having a plurality of groups of main amplifiers, wherein the read data on dout from each group of main amplifiers charges up a capacitance C_0 in response to an S0 timing signal which is then shorted to a plurality of shared capacitances equal in number to the plurality of said groups of main amplifiers in response to a S1 timing signal, and wherein a shorted voltage across the plurality of shared capacitances is compared with the Vdd/2 voltage. 15. The static random-access memory of claim 6, having a plurality of groups of main amplifiers, wherein the read data on dout from each group of main amplifiers charges up a capacitance C_0 in response to an S0 timing signal which is then shorted to a plurality of shared capacitances equal in number to the plurality of said groups of main amplifiers plus one in response to a S1 timing signal, and wherein a shorted voltage across the plurality of shared capacitances is compared with the Vdd/2 voltage.

17. A circuit for generating a half Vdd voltage from a main on-chip supply voltage Vdd/Vss comprising series connected transistors M1 and M2 in parallel with series connected transistors M3 and M4, connected between Vdd and Vss, with the half Vdd voltage output from a node connecting transistors M1, M2, M3 and M4, wherein transistors M1 and M3 function as a self-biased inverter and transistors M2 and M4

function as current sensing transistors.

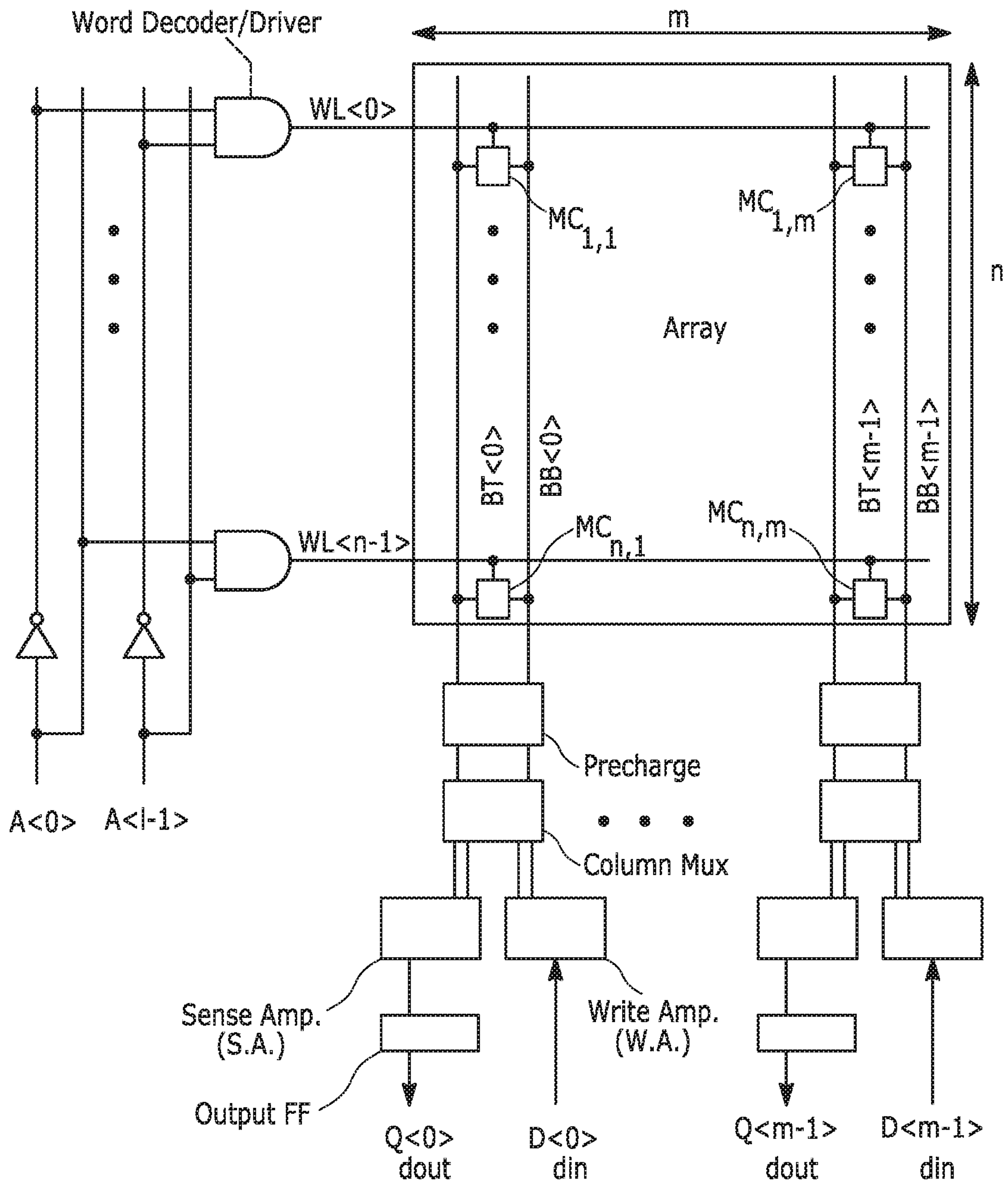
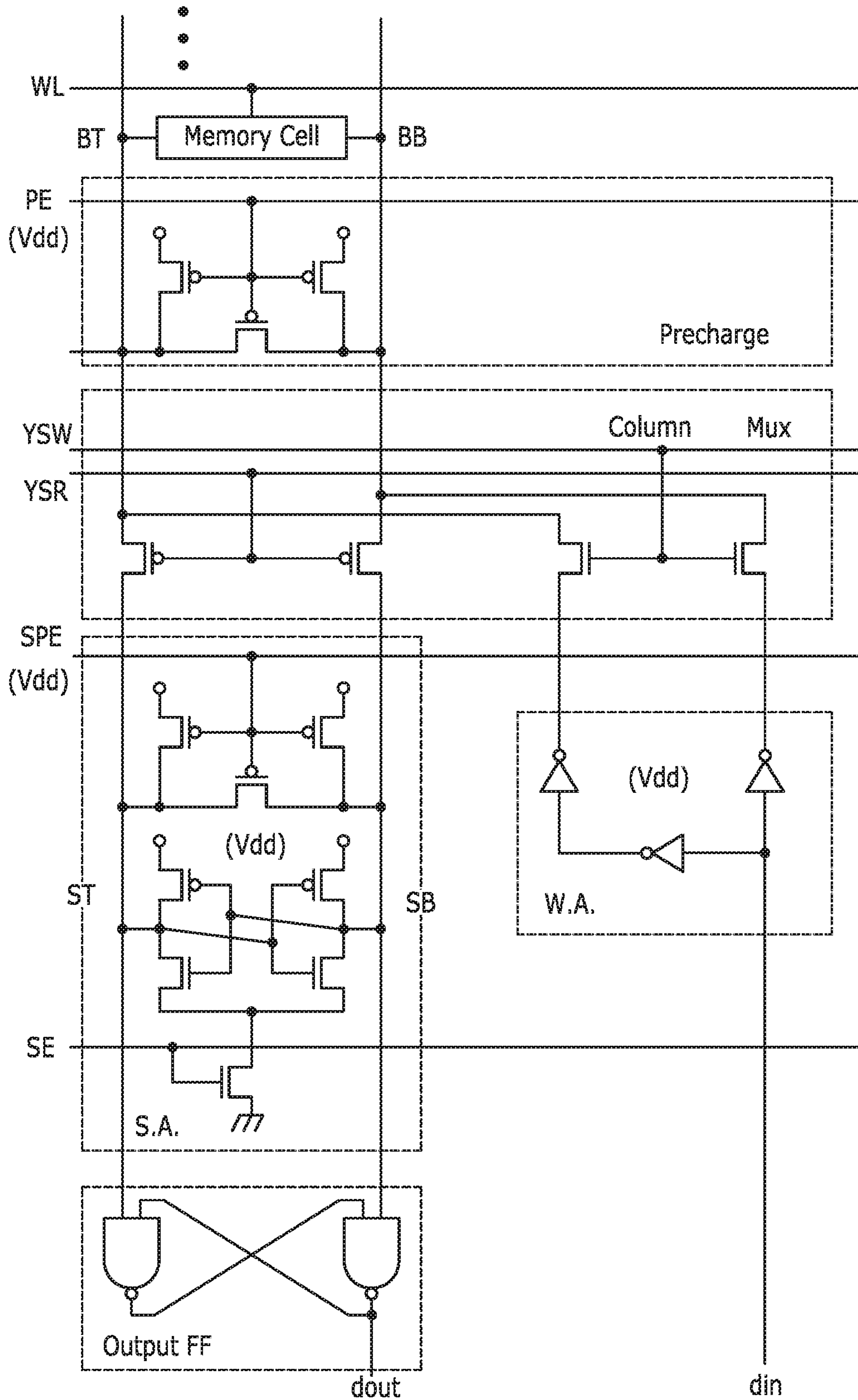


FIG. 1a



PRIOR ART

FIG. 1b

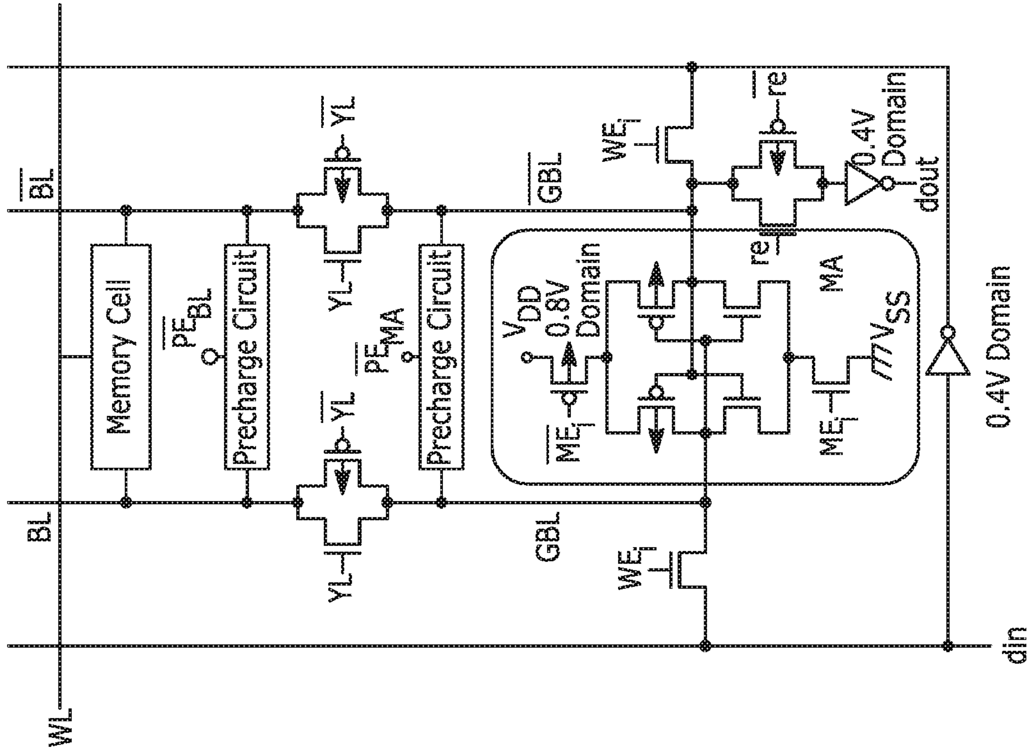


FIG. 2b

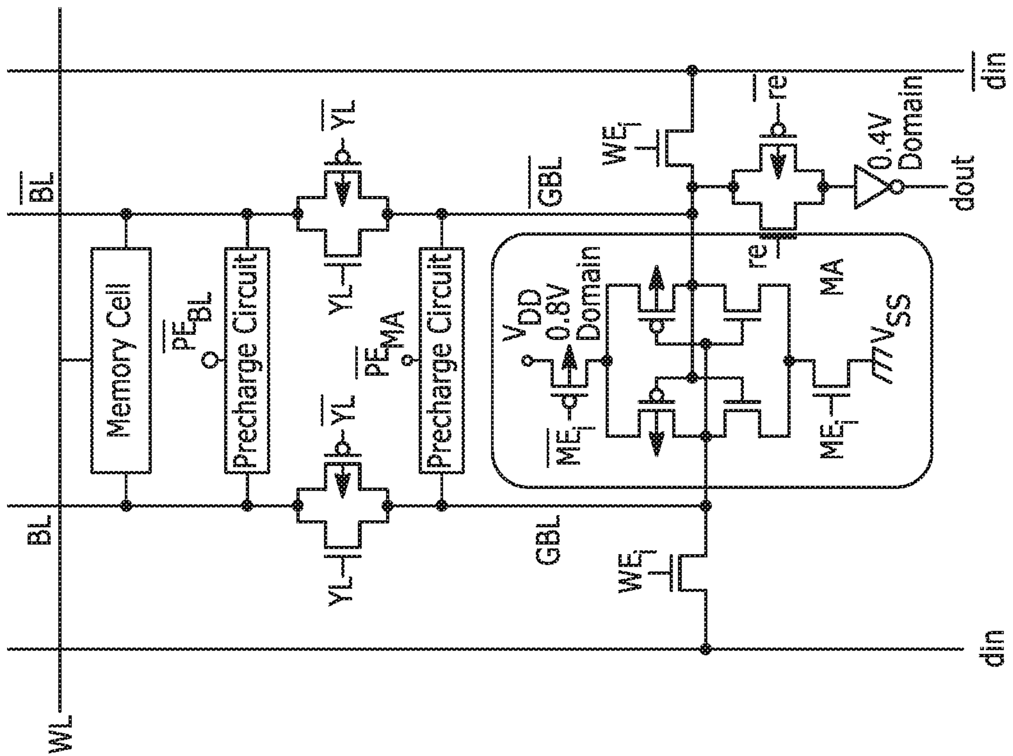


FIG. 2a

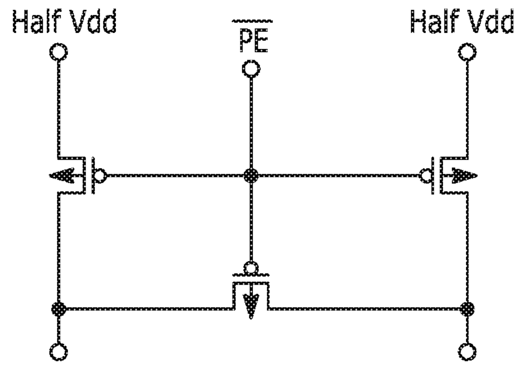


FIG. 2c

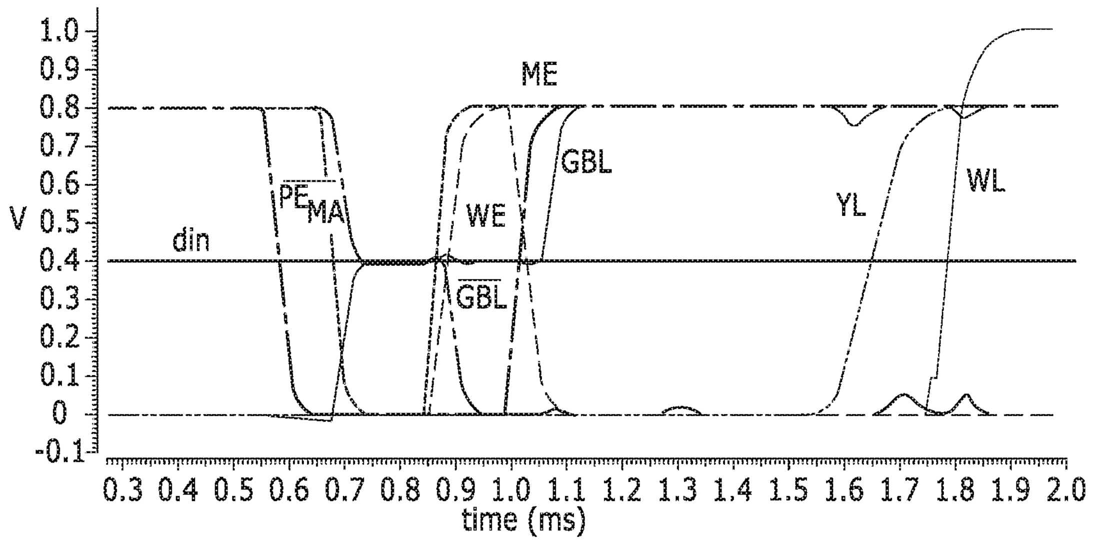
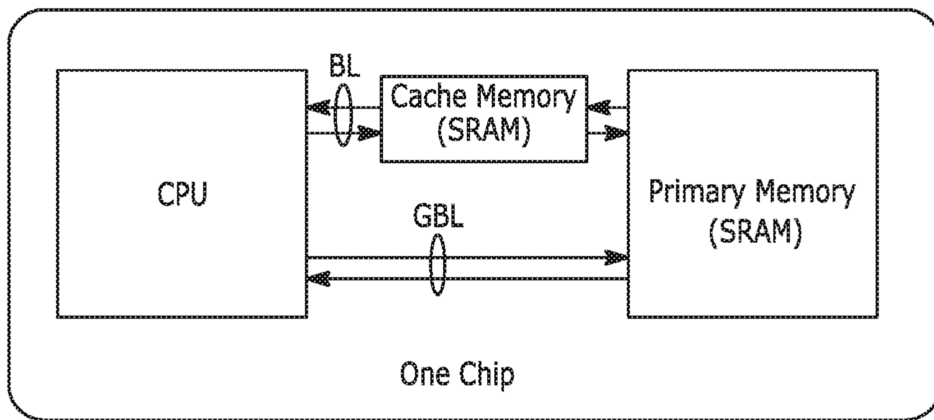


FIG. 2d



PRIOR ART

FIG. 3

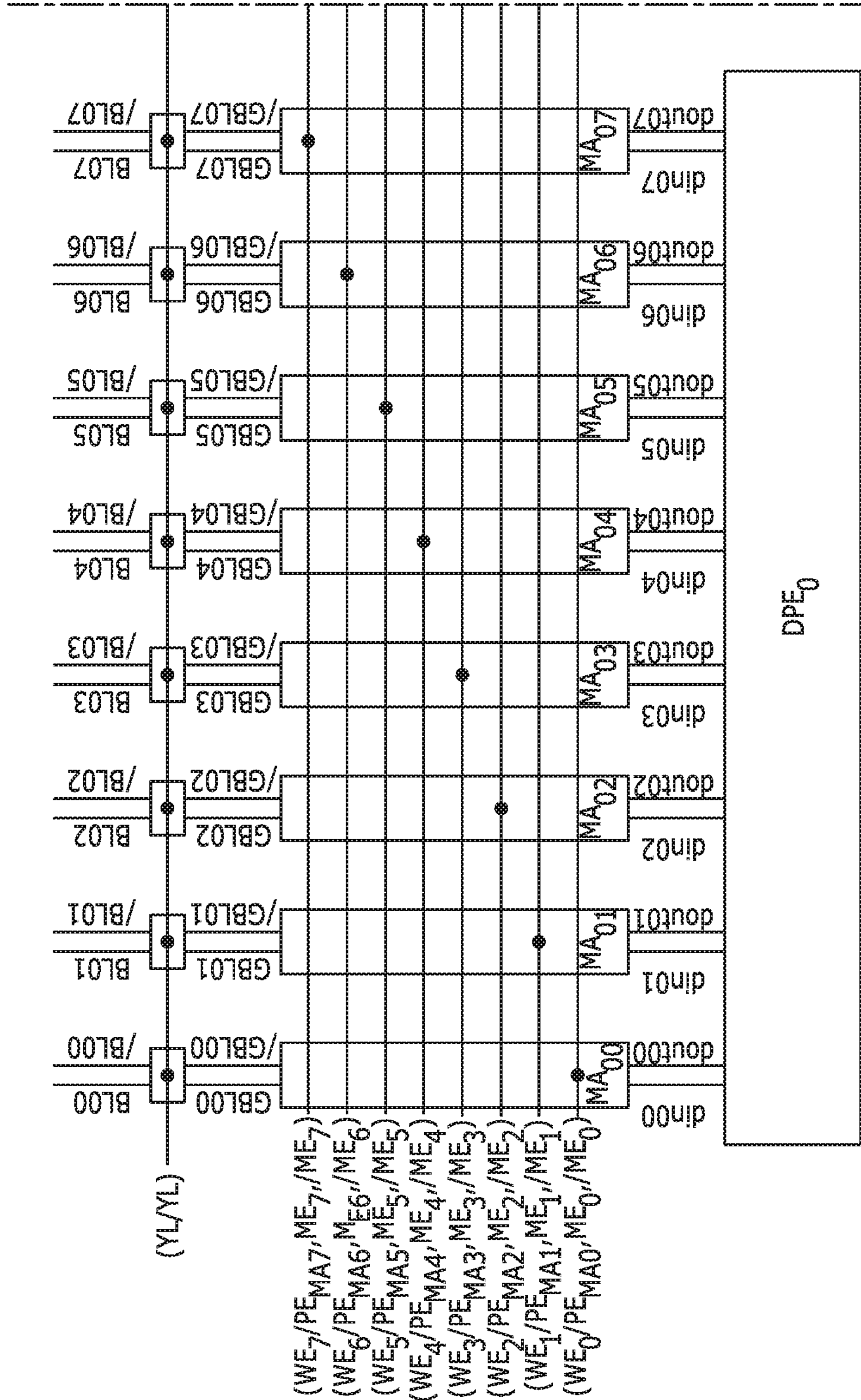


FIG. 4

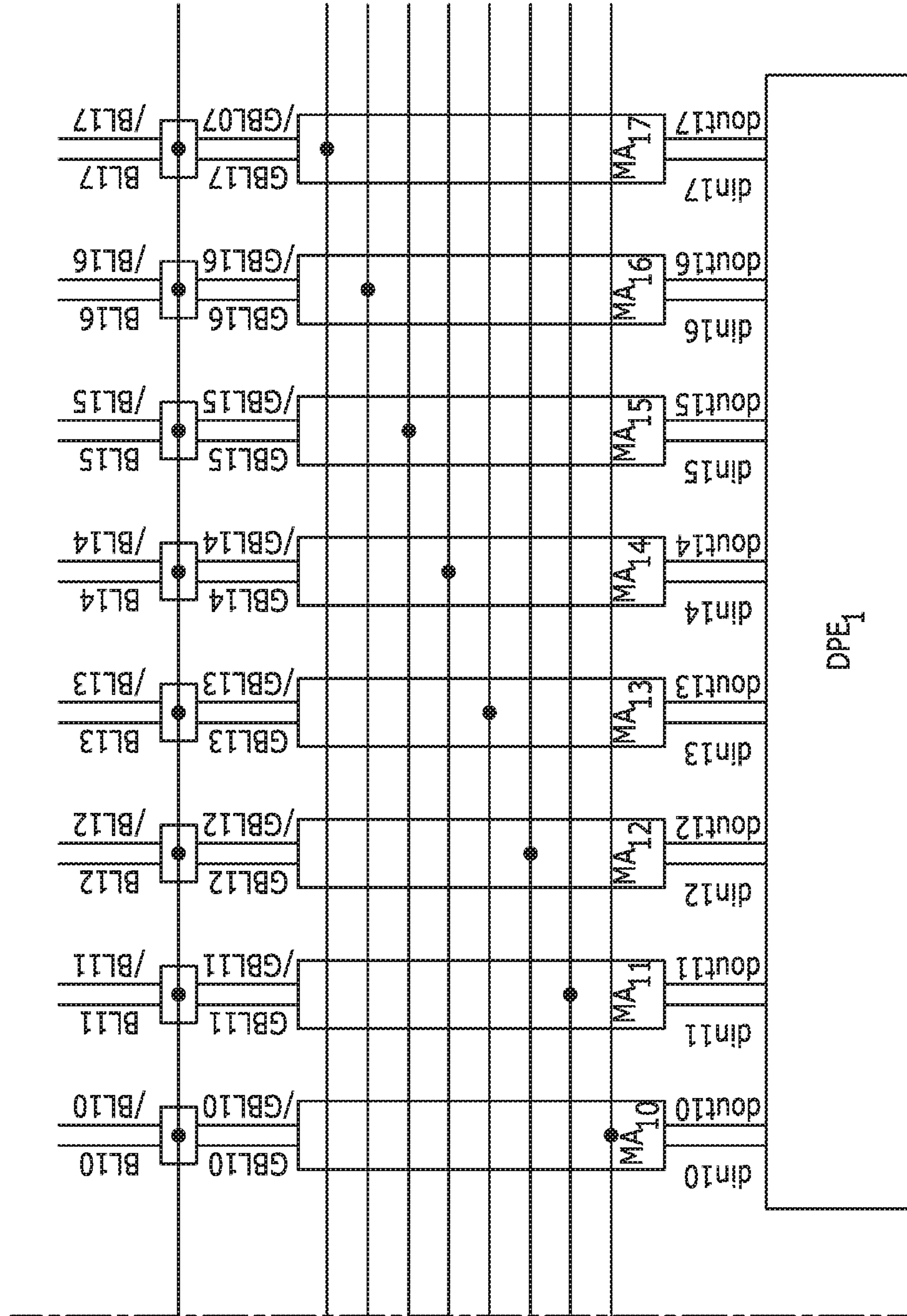


FIG. 4 (Continued)

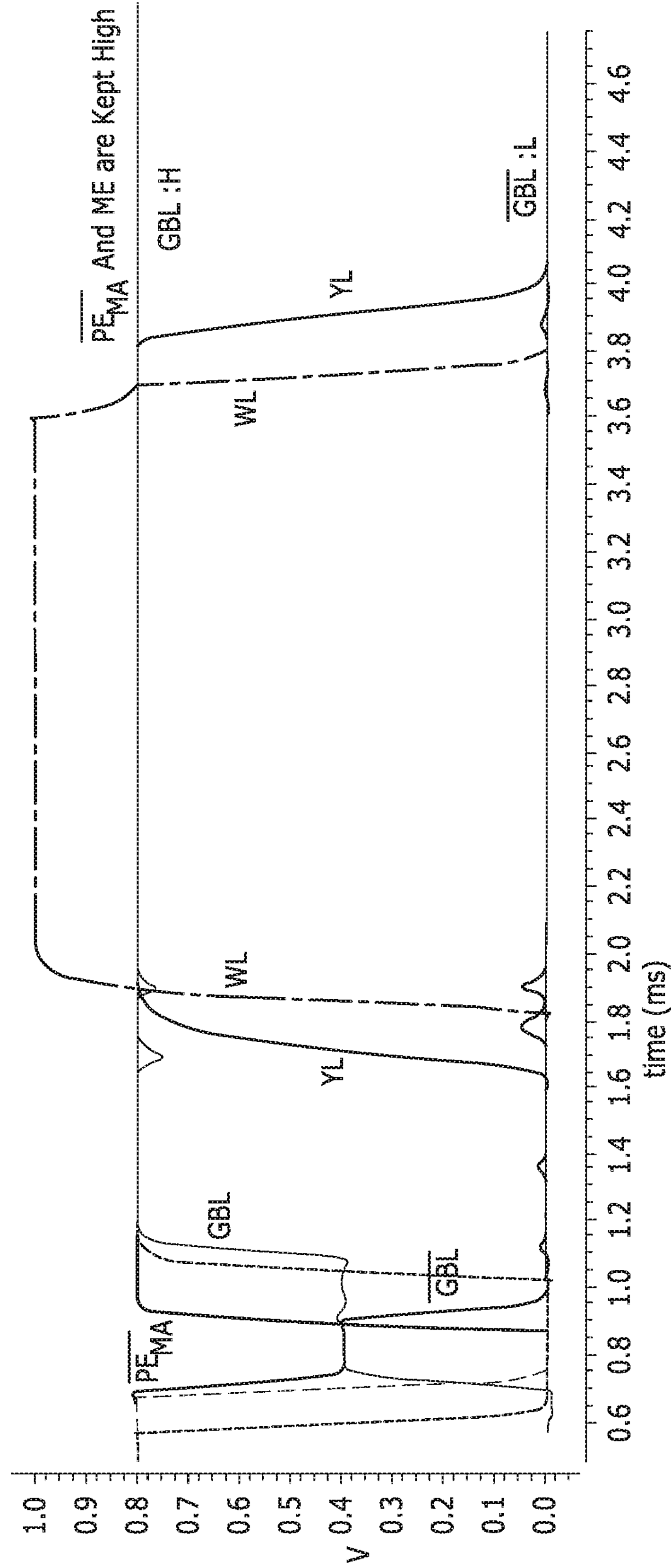


FIG. 5

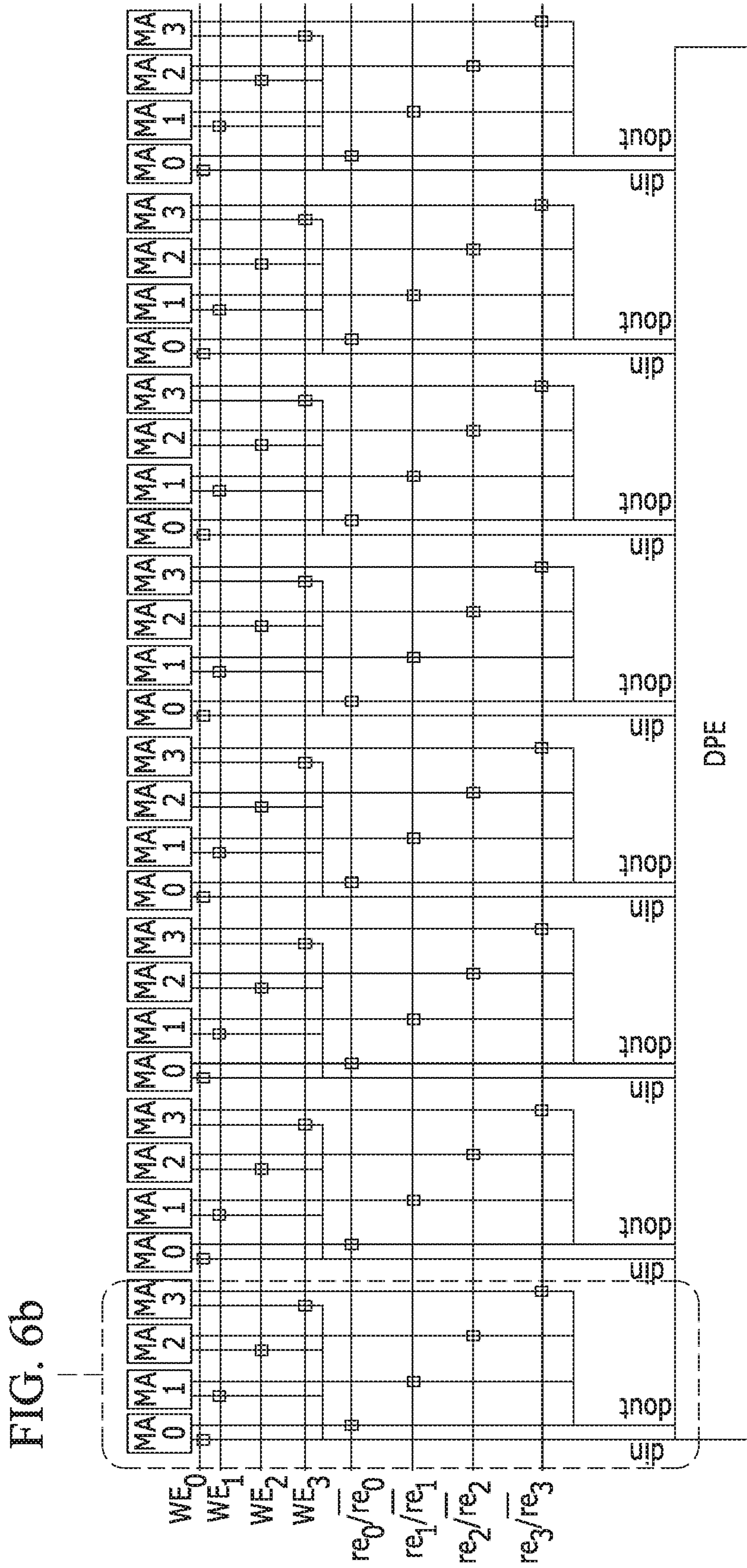


FIG. 6a

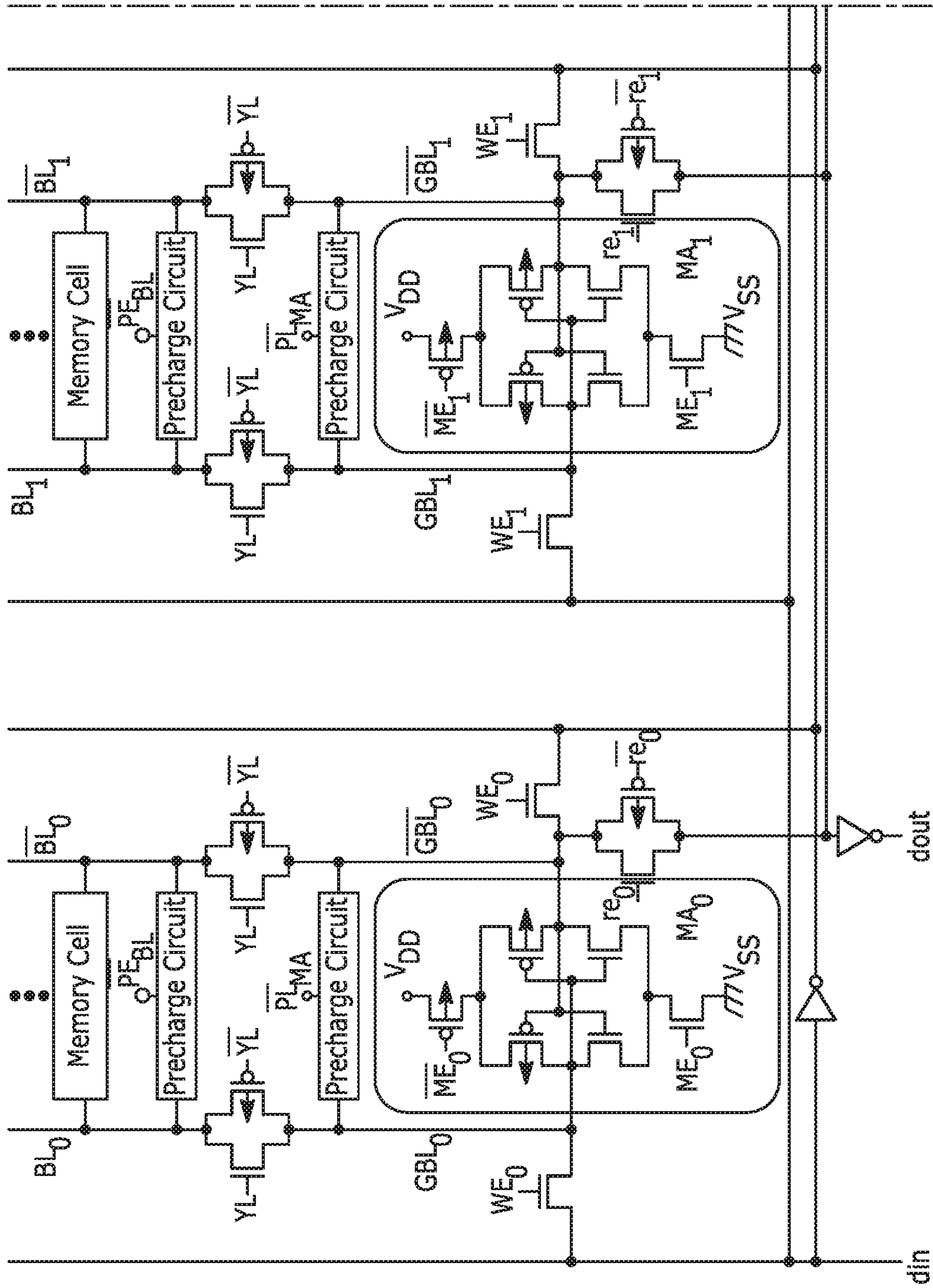


FIG. 6b

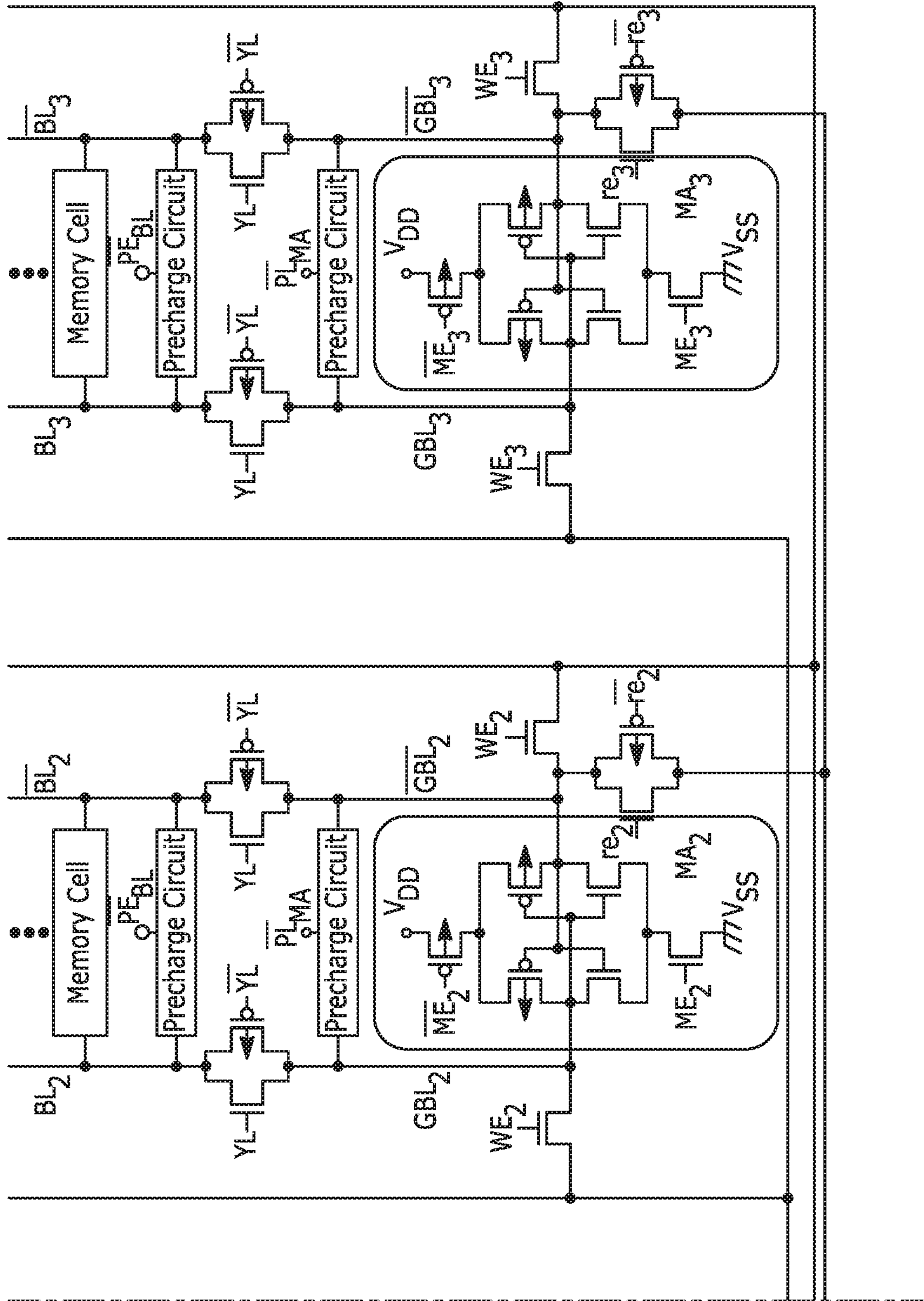


FIG. 6b (Continued)

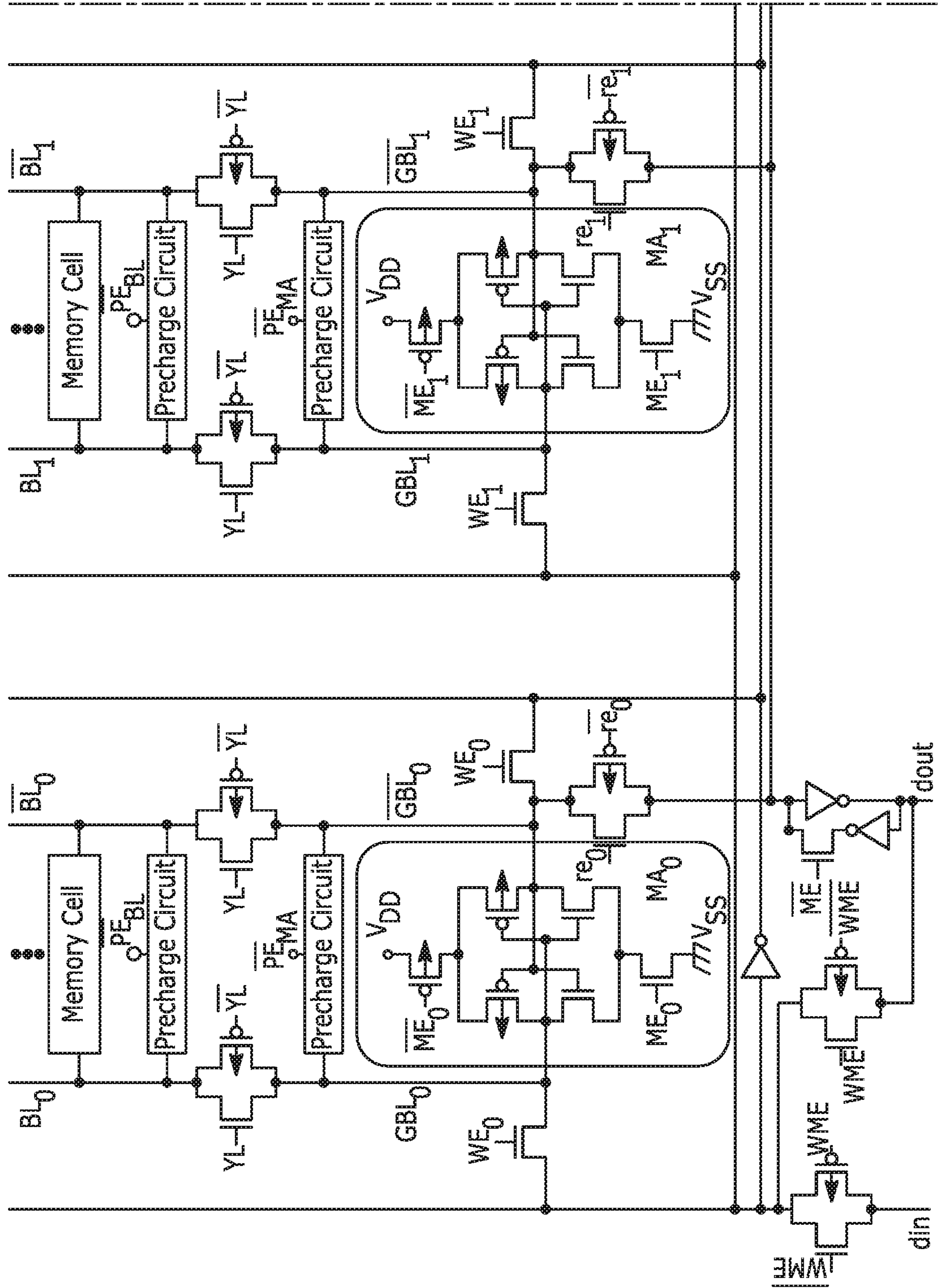


FIG. 7

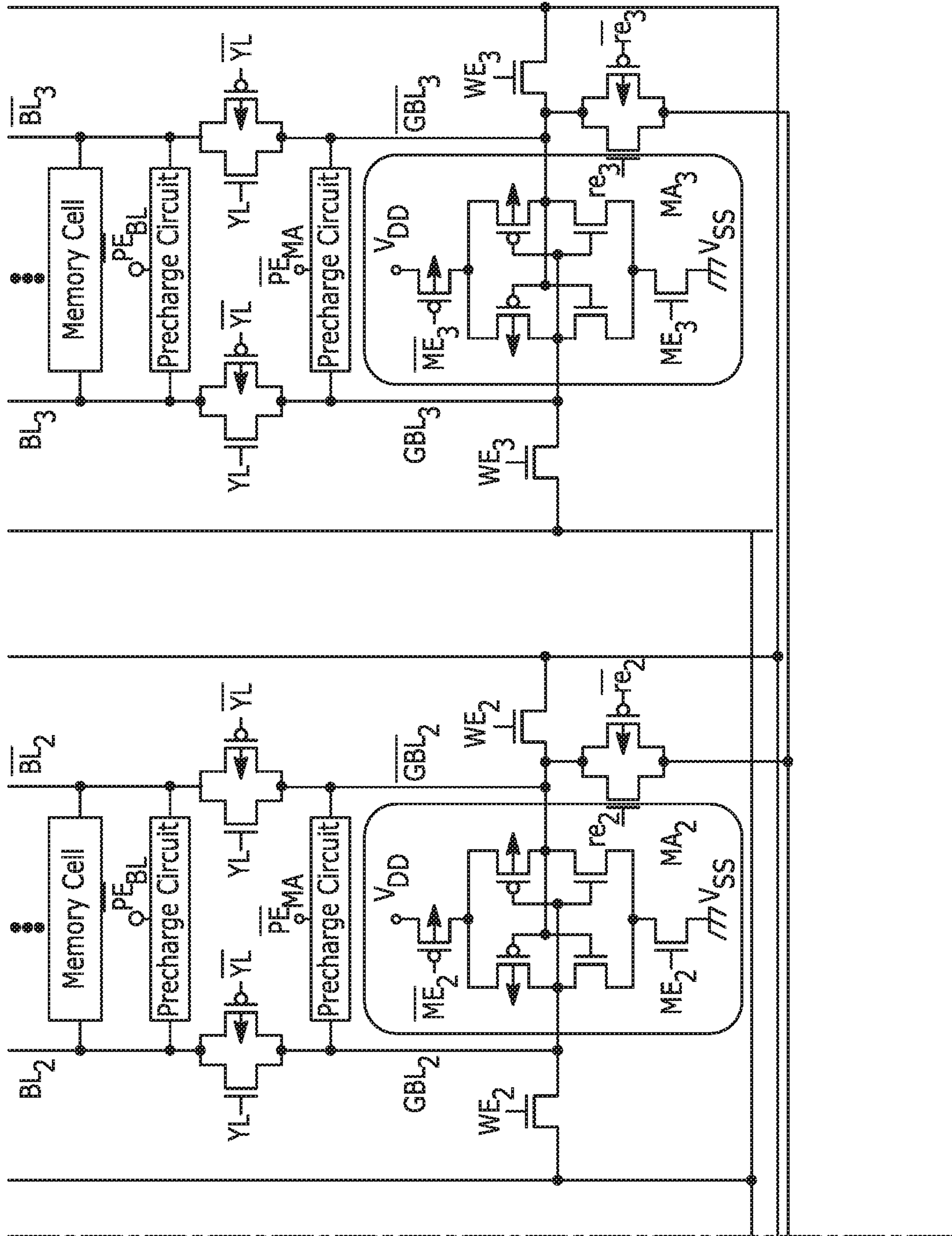


FIG. 7 (Continued)

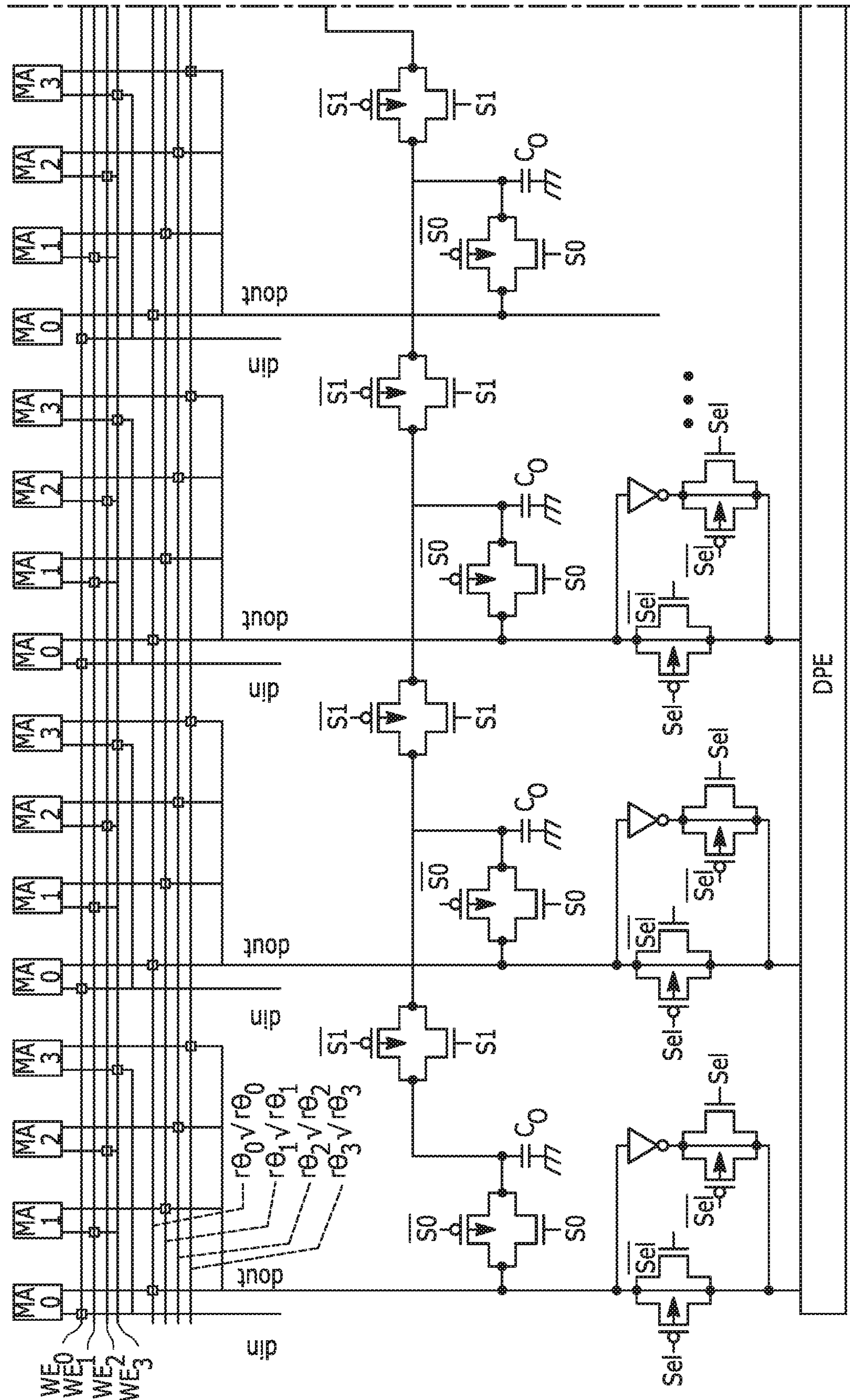


FIG. 8

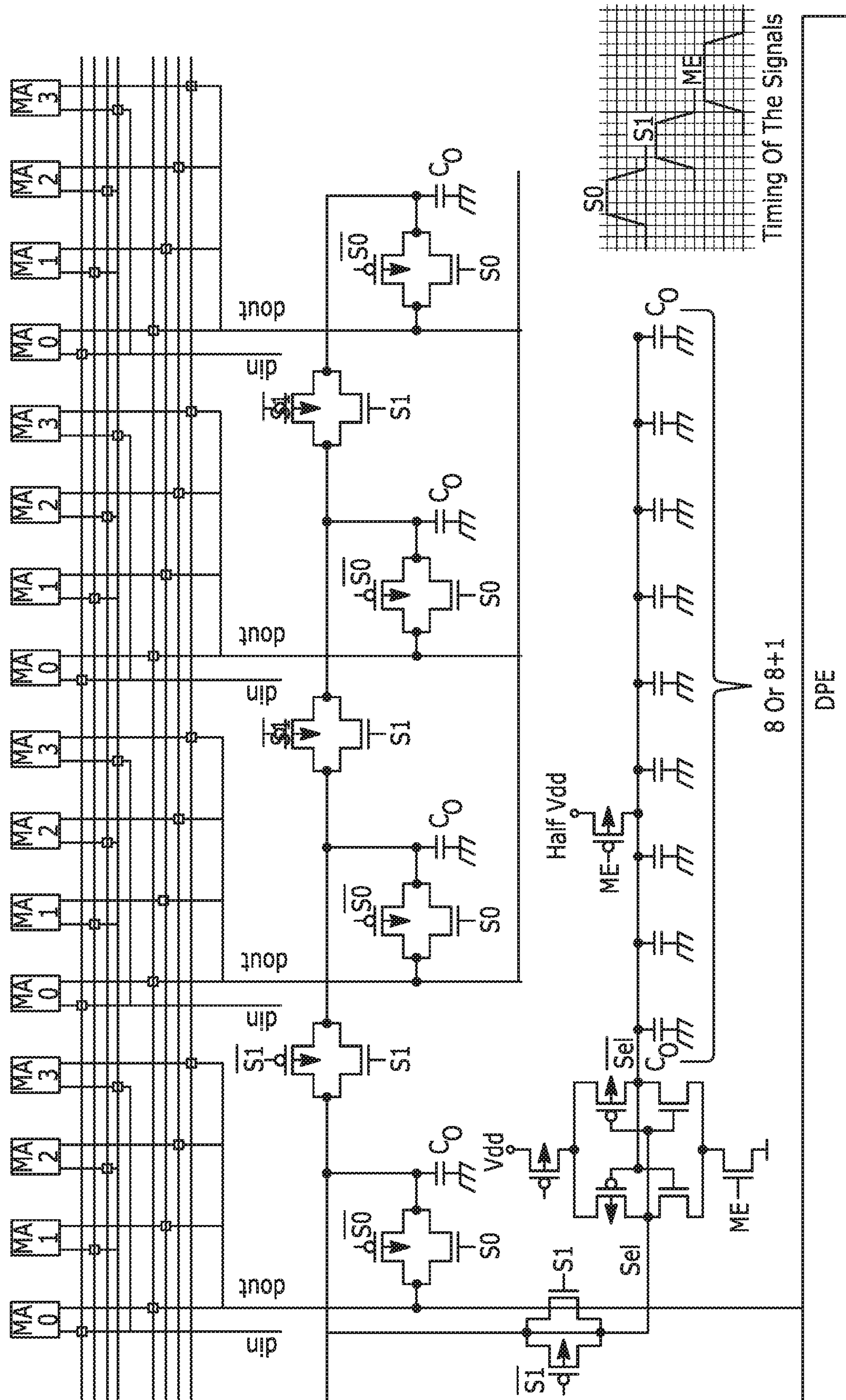


FIG. 8(Continued)

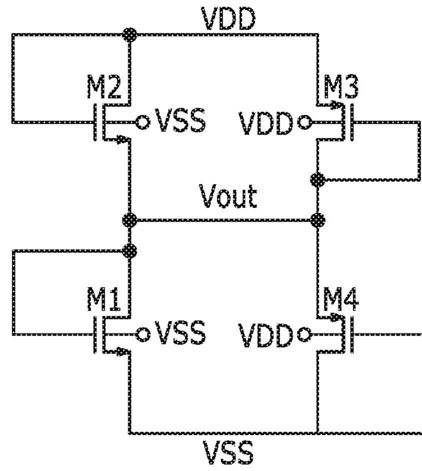


FIG. 9a

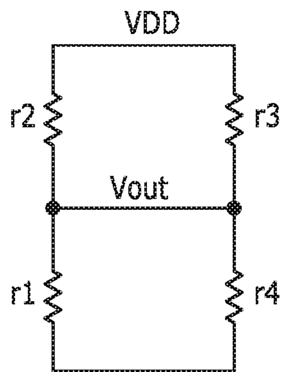


FIG. 9b

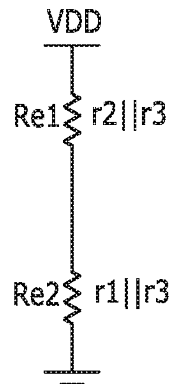


FIG. 9c

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2022/055759

A. CLASSIFICATION OF SUBJECT MATTER

IPC: ***G11C 11/419*** (2006.01) , ***G11C 5/14*** (2006.01) , ***G11C 7/12*** (2006.01) , ***G11C 8/08*** (2006.01)

CPC: **G11C 11/419** (2020.01) , G11C 5/147 (2021.02) , G11C 7/12 (2020.01) , G11C 8/08 (2020.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC (2006): G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
Database: Canadian Patent Database (Intellect), Questel Orbit, Google Patent
Keywords: static random access memory, SRAM, transistor cell, bitline, precharge, amplifier, response, deep learning, DPE, cache, select, memory cell

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2012/0014172 (JUNG et al.) 19 January 2012 (19-01-2012) * Paragraphs [0029]-[0031], [0037], [0038], [0055]-[0058], [0060] and [0067] *	1 and 5-10 --- 3, 4 and 11-16
Y	US 2012/0314468 (SIAU et al.) 13 December 2012 (13-12-2012) * Paragraphs [0007]-[0009], [0031], [0033], [0036], [0053], [0069] and [0071] *	3, 4 and 16
Y	US 2019/0340069 (KUMAR et al.) 07 November 2019 (07-11-2019) * Paragraphs [0009]-[0011], [0060], [0061], [0072], [0078] and [0084] *	11-15
A	US 2012/0014173 (DENG) 19 January 2012 (19-01-2012) * Whole document *	1-16

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

*	Special categories of cited documents:		
"A"	document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"D"	document cited by the applicant in the international application	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier application or patent but published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
26 September 2022 (26-09-2022)	03 October 2022 (03-10-2022)

Name and mailing address of the ISA/CA	Authorized officer
Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 819-953-2476	Alan Chan (819) 639-2473

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2016/0118091 (ASENOV et al.) 28 April 2016 (28-04-2016) * Whole document *	1-16
A	US 2017/0206949 (PICKERING) 20 July 2017 (20-07-2017) * Whole document *	1-16
A	US 2013/0148414 (SHU et al.) 13 June 2013 (13-06-2013) * Whole document *	1-16
A	US 2010/0265778 (YASUDA) 21 October 2010 (21-10-2010 * Whole document *	1-16
A	US 2021/0149763 (RANGANATHAN et al.) 20 May 2021 (20-05-2021) * Whole document *	1-16
A	Chen, Y. et al., "A 16nm 128Mb SRAM in High-κ Metal-Gate FinFET Technology with Write-Assist Circuitry for Low-V_{MIN} Applications", IEEE Journal of Solid-State Circuits, Vol 50, No. 1, January 2015, Pages 170-177. * Whole document *	1-16

Box No. II **Observations where certain claims were found unsearchable (Continuation of item 2 of the first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claim Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claim Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claim Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III **Observations where unity of invention is lacking (Continuation of item 3 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:
The claims are directed to a plurality of inventive concepts as follows:
Group A - Claims 1-16 and 15 (second instance; or claim 16, line 6-12) are directed to a static random-access memory; and
Group B – Claim 17 is directed to a circuit for generating a half Vdd voltage from a main on-chip supply voltage.
(Note that there are two identical instances of claim 15)

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claim Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim Nos.:

1-16

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/IB2022/055759

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
US2012014172A1	19 January 2012 (19-01-2012)	US2012014172A1	19 January 2012 (19-01-2012)
		US8995208B2	31 March 2015 (31-03-2015)
		KR20120008254A	30 January 2012 (30-01-2012)
		KR101781616B1	26 September 2017 (26-09-2017)
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		US10956263B2	23 March 2021 (23-03-2021)
		CN110444242A	12 November 2019 (12-11-2019)
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		KR20160047982A	03 May 2016 (03-05-2016)
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		TW201629956A	16 August 2016 (16-08-2016)
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		CN106463163A	22 February 2017 (22-02-2017)
		CN106463163B	01 November 2019 (01-11-2019)
		EP3140832A1	15 March 2017 (15-03-2017)
		EP3140832B1	04 July 2018 (04-07-2018)
		GB201408128D0	25 June 2014 (25-06-2014)
		GB2525904A	11 November 2015 (11-11-2015)
		GB2525904B	09 May 2018 (09-05-2018)
		KR20160149297A	27 December 2016 (27-12-2016)
		TW201606767A	16 February 2016 (16-02-2016)
		TWI664632B	01 July 2019 (01-07-2019)
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Continued in Supplemental Box

Continuation of patent family members

US2013148414A1	13 June 2013 (13-06-2013)	US2013148414A1	13 June 2013 (13-06-2013)
		US8593860B2	26 November 2013 (26-11-2013)
		CN104335281A	04 February 2015 (04-02-2015)
		CN104335281B	30 October 2018 (30-10-2018)
		EP2788986A1	15 October 2014 (15-10-2014)
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		EP2788986B1	20 September 2017 (20-09-2017)
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