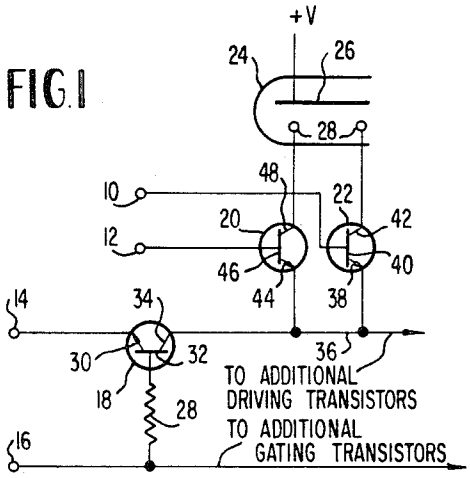
July 30, 1968 D. M. BARTON 3,395,268

BLANKING CIRCUIT FOR A PLURAL CATHODE DISPLAY TUBE

Filed June 10, 1965

FIG. 1



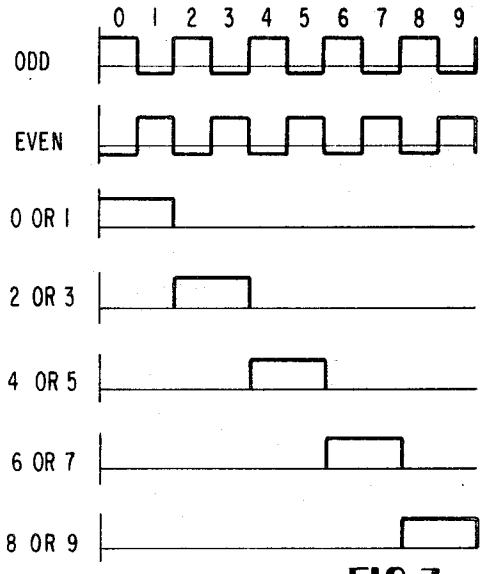
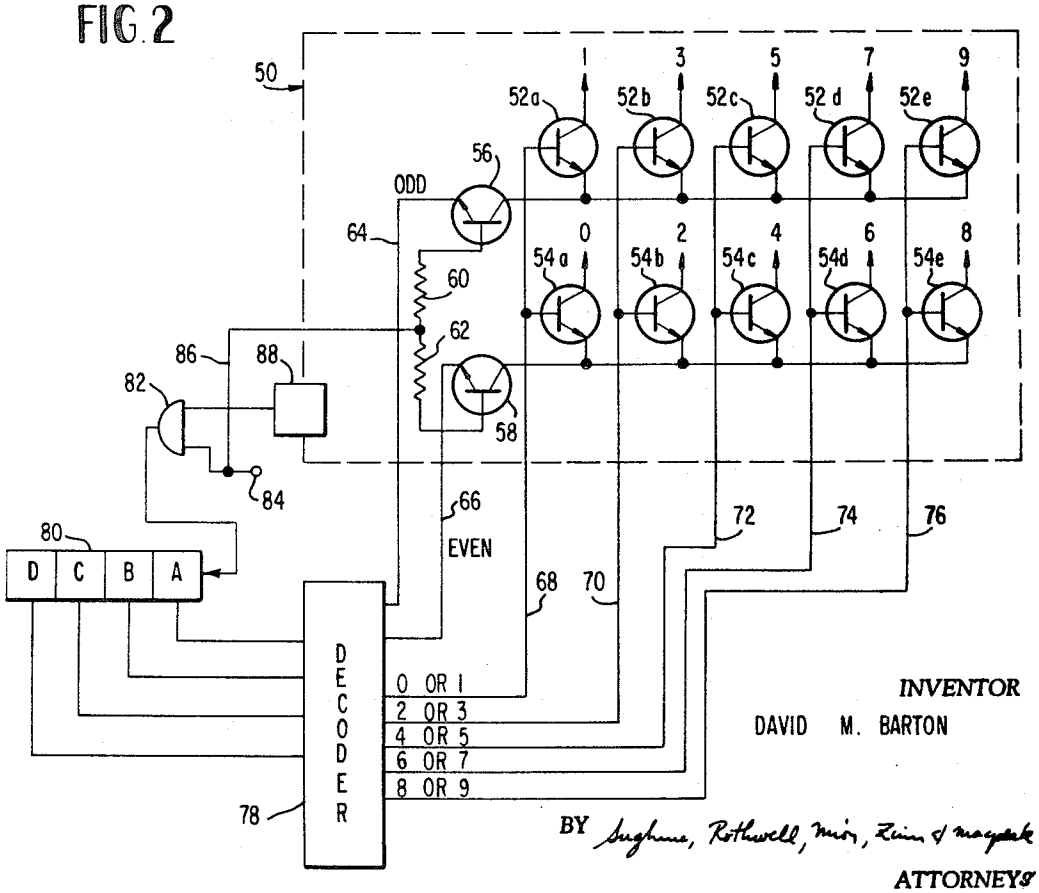


FIG. 3

FIG. 2



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3,395,268

BLANKING CIRCUIT FOR A PLURAL CATHODE DISPLAY TUBE

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1 Claim. (Cl. 235—92)

ABSTRACT OF THE DISCLOSURE

A transistorized circuit for connection between a counter and a numerical display tube to prevent the initiation of the display tube by the signals on the counter output leads while the counter is accumulating input actuation. A separate driving transistor for each indication on the display tube is energized only by the coincidence of unique conditioning signal and a common driving signal. The conditioning signals are applied to the bases respectively of the transistors. The driving signal is applied through a separate gating transistor to the emitters of a plurality of transistors. The driving and conditioning signals combine to select the particular transistor to be energized but a blanking pulse applied to the gating transistor prevents all transistors from being energized.

This invention relates to an electronic blanking circuit for blanking an illuminated read-out display during selected intervals.

The invention pertains to a circuit configuration for blanking or turning off a read-out device for a digital counter, such as a Burroughs Nixie numeric display tube. Such a tube is customarily operated from a counter by means of a coded arrangement of wires selectively conditioned in response to the state of the counter. The cathodes of the Nixie tube may be driven by individual transistors, each having its collector connected to the related cathode of the Nixie tube, its base connected to one of the coded wires from the counter and its emitter connected to another of the coded wires from the counter, the coding scheme requiring an input on the base and emitter to make the selected transistor conduct.

In digital measuring applications having display tube read-outs, e.g., digital voltmeter with read-out, a blur appears on the read-out tube between readings because an internal counter which is accumulating to form the answer is connected via a decoder circuit directly to the read-out device. The blur on the read-out device is annoying to the user. One scheme in the prior art for eliminating "blur" is to employ a storage means within the digital voltmeter. The storage means remembers the previous reading and stores it during the counting interval. At the end of the counting interval and on command of a given signal, the counter output is read by the storage means. Since the read-out display tube receives its information from the storage means and not from the counter, no blur occurs. Memories such as this are fairly expensive and thus there is an obstacle to their use in inexpensive measurement applications.

In accordance with the present invention, a simple, inexpensive electronic circuit is provided for connection between the display tube and the counter and decoder circuits for blanking the display tubes during the counting interval. Blanking transistors are inserted in series with the drive lines leading to the emitters of the driving transistors. By applying a blanking signal to the base of the series connected blanking transistors, the driving current to the emitters of the driving transistors can be blocked and the display tube will remain dark. It has been demonstrated that in an instrument in which the counting interval is short, there is little or no annoyance to the human eye if the read-out is simply blanked during this interval.

It is therefore an object of the present invention to provide a new and improved circuit for blanking a display tube during selected intervals.

A further object of the present invention is to provide a new, improved and inexpensive circuit for blanking a read-out tube during selected intervals.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings.

In the drawings:

FIGURE 1 is a schematic diagram of a preferred embodiment of the invention;

FIGURE 2 is a partially schematic and partially block diagram of an embodiment of the invention used in conjunction with a particular counter and decoding circuit;

FIGURE 3 is a series of time-waveforms helpful in explaining the operation of FIGURE 2.

Referring to FIGURE 1, there is shown a read-out display tube **24** which may be a Burroughs Nixie tube, having an anode **26** connected to a voltage source V, and cathodes **28**. Each cathode **28** corresponds to a particular character of the tube which is displayed when the corresponding cathode is energized. The display tube **24** is shown open ended to indicate that the tube may include additional cathodes not shown. Driving transistors **20** and **22** conduct current to the cathodes **28** of the display tube **24**, thus illuminating the corresponding characters. Terminals **10** and **12** are connected to bases **40** and **46** of transistors **22** and **20**, respectively. Collectors **42** and **48** of the driving transistors are connected to the cathodes **28** of the display tube, and emitters **38** and **44** are connected to a driving line **36** which supplies driving voltage to the driving transistors. A gating or blanking transistor **18**, having an emitter **30**, base **32** and collector **34** is connected via collector **34** to the emitter drive line **36**. It should be noted that emitter drive line **36** may be connected to the emitters of additional driving transistors not shown. Emitter **30** of transistor **18** is connected to a terminal **14** and base **32** is connected via a current limiting resistor **28** to the blanking input terminal **16**. Blanking input terminal **16** may also be connected to additional blanking or gating transistors, not shown in FIGURE 1. The number of driving transistors used and the number of blanking transistors necessary for a given number of driving transistors may vary and is dependent upon the particular coding scheme used in the display circuitry.

Transistor **18** is a blanking transistor which acts when turned off to blank all of the characters of the display tube which are driven by the driving transistors and which have their emitters connected to the collector of the blanking transistor. When terminal **16** is several volts positive, transistor **18** is in the "on" condition and control of the driving transistors is determined by the conditioning signals applied to their bases and emitters, respectively. For example, assuming transistor **18** is "on," driving transistor **20** is controlled by the conditioning signals applied to terminals **12** and **14**. A conditioning signal at terminal **12** is a slightly positive signal and a conditioning signal at terminal **14** is a grounded or slightly negative signal. With conditioning signals applied in coincidence at terminals **12** and **14**, and assuming transistor **18** is "on," driving transistor **20** will turn on thus causing a display character associated with driving transistor **20** to be illuminated. If a conditioning signal is present on only one of the input terminals, transistor **20** will not turn on and thus its associated character will not be illuminated.

In the illustration shown in FIGURE 1, if tube **24** is a Nixie tube having ten cathodes, corresponding to the decimal character 0 through 9, the presence of a conditioning signal at terminal **12** and a conditioning signal at terminal **14** will turn on driving transistor **20** and the Nixie tube will indicate a "0" reading. The presence of a conditioning signal at terminal **10** and a conditioning signal at terminal **14** will turn on driving transistor **22** resulting in the display of decimal character "1". The remainder of the driving transistors are not shown but it should be apparent that they would operate in the same manner as driving transistors **20** and **22** The input signals to the bases of the driving transistors may be the output leads from a decoding circuit which provides only one output at a time to any of the base terminals **10**, **12**, etc., in order to prevent conduction of more than one driving transistor at any one time. The decoding circuit may be connected to the output of an electronic counter which is used, for example, in a digital voltmeter. The particular decoding circuit and/or counter form no part of the present invention which consists of a novel blanking circuit that may be used with various types of counters and decoding schemes.

If the circuit is used with an electronic counter and decoding circuit as explained above, during the accumulation or counting period of the counter, the reading of the Nixie tube will be changing in accordance with the variation of the conditioning signals applied to base terminals of the driving transistors by the decoding circuit. The latter situation creates a visual blur on the Nixie read-out tube which is annoying to the user. In order to eliminate the blur it becomes necessary to prevent the read-out tube from responding to the decoder output during the accumulation or counting period. This may be done in the present invention by applying a blanking pulse to terminal **16**. The blanking pulse which in the embodiment shown is a grounded or slightly negative signal turns off blanking transistor **18** which in turn electrically disconnects terminal **14** from the emitter drive line **36**. All of the driving transistors are thus prevented from receiving a conditioning signal appearing at terminal **14** and thus remain in their non-conducting condition. When the counting period is over, the blanking signal is removed allowing the driving transistors to respond to the particular count of the counter and allowing the Nixie display tube to display the new count.

In FIGURE 2 there is shown a specific arrangement of the blanking circuit **50** for use with a particular coding arrangement. Terminal **84** may be the output connection of any measuring circuit, e.g., the output of an analog-to-time voltage converter. Input terminal **84** is connected as one input to AND gate **82**, the other input being supplied with pulses from a pulse source **88**. Terminal **84** is also connected to the blanking circuit **50** via lead **86** which connects particularly to the bases of blanking transistors **56** and **58** through current limiting resistors **60** and **62**, respectively. The output of AND gate **82** is supplied to a counter **80** having stages, A. B. C. and D. The outputs from counter **80** are applied in parallel as inputs to a decoder device **78**. The particular counter and decoder circuits form no part of the present invention, however, one such counter and decoder arrangement which provides a coded output arrangement similar to that shown in FIGURE 2 can be seen in U.S. patent application Ser. No. 440,830, filed Mar. 18, 1965, and assigned to assignee of the present invention. The output from decoder **78** is illustrated by the time-waveform graphs shown in FIGURE 3. It can be seen that for every odd count in the counter, lead **64** becomes slightly negative and lead **66** becomes positive, and for every even count in the counter, lead **66** becomes slightly negative and lead **64** becomes positive. Decoder output lead **68**, **70**, **72**, **74**, and **76** become selectively positive representing the counts of 0 or 1, 2 or 3, 4 or 5, 6 or 7 and 8 or 9, respectively. For example, if the counter **80** has received eight input pulses, it can be seen by reference to FIGURE 3 that decoder output lead **66** will be slightly negative and decoder output lead **76** will be positive.

The driving transistors **52A** through **52A** and **54A** through **54E** are arranged to provide driving signals to a ten-character Nixie tube display having characters 0 through 9. The numerals appearing above the collectors of the respective driving transistors represent the character of the Nixie tube responsive to the individual driving transistor. Odd character driving transistors **52A** through **52E** are connected to the collector of blanking transistor **56**, and even character driving transistors **54A** through **54E** have their emitters connected to the collector of blanking transistor **58**. The emitters of blanking transistors **56** and **58** are connected respectively to the odd lead **64** and the even lead **66** from decoder **78**.

The operation of FIGURE 2 is as follows: Assume the counter **80** has received six pulses from the source **88** through the AND gate **82** and that no further pulses are being received and accumulated bceause terminal **84** is high and the gate **82** is only conditioned by a low or negative voltage signal at terminal **84**. Having received the six input pulses, the stages of counter **80** will be particular stable states depending upon the type of counter used and the number of input pulses received. The output wires of the counter which are connected to the input of the decoder **78** are selectively energized in dependence upon the particular stable states of the stages of counter **80**. Under the conditions described, the decoder output line **66** will be low or negative indicating an "even" count and decoder output line **74** will be positive indicating a count of either 6 or 7. It can be seen by referring to FIGURE 3 that the decoder provides a negative output on the "even" line and a positive output on the "6" or "7" line when the counter has accumulated six pulses. The signal on lead **74** is applied to the bases of transistors **52D** and **54D**. However, a driving negative potential is applied only to the emitter of transistor **54D** via line **66** and the emitter-collector path of blanking transistor **58**, and no driving voltage is applied to the emitter of transistor **52D**. Thus, with conditioning signals applied to the base and emitter of transistor **54D**, that transistor becomes conductive causing the Nixie tube to display the digit 6. The display continues to indicate the digit 6 as long as neither a blanking signal is applied to blanking transistor **58** nor the count in counter **80** changes.

If, for example, terminal **84** is connected to an analog-to-time voltage converter, and it is desirable to take readings periodically, a second reading may be initiated in the counter by resetting the counter to 0 by means not shown, and providing the negative signal output of the analog-to-time converter to energize AND gate **82** and blank the display. The width of the negative pulse at terminal **84** will be proportional to the analog voltage being measured by the analog-to-time converter, and, consequently, the number of pulses passed through AND gate **82** from pulse source **88** will be proportional to the analog voltage being measured. Also, the negative voltage at terminal **84** is connected via lead **86** and current limiting resistors **60** and **62** to the bases of blanking transistors **56** and **58**. The blanking transistors **56** and **58** consequently become non-conducting during the accumulation period and prevent driving currents from being supplied to the emitters of the driving transistors **52A** through **52E** and **54A**. During the accumulation period the counter **80** will accumulate the pulses supplied thereto by the pulse source **88** and the output of the decoder **78** will be changing with each additional pulse input to the counter. However, since the display is blanked by the blanking transistors **56** and **58**, the outputs from the decoder **78** will not cause a blur on the Nixie tube display. The termination of the negative pulse at terminal **84** ends the accumulation period and at the same time removes the blanking signal from the bases of transistors **56** and **58**. The output of the decoder **78** which is now a coded indication of the number of pulses accumulated by the counter

energizes a particular driving transistor in the manner described above.

Although preferred embodiments of the invention have been described above, particularly FIGURE 2 which shows a specific arrangement of one blanking transistor per five driving transistors, it should be apparent that the number of driving transistors and blanking transistors may vary in dependence upon the code used and the number of Nixie display tubes used. The invention contemplates primarily the use of a blanking transistor for isolating one of the conditioning signals from a driving transistor which can become conductive only upon the application of two conditioning signals being applied thereto.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A blanking circuit for a display tube of the type having a plurality of cathodes each corresponding to a different character to be displayed, said display tube adapted to display a numerical indication of the count accumulated by a counter which receives pulses only during the presence of a gating pulse and whose output is applied to a decoder, said decoder having a first pair of outputs and a second plurality of outputs indicating the count in said counter, comprising

(a) a first and second group of driving transistors each having emitter, base and collector terminals, each having its collector terminal connected to a different cathode of said display tube and energized by a conditioning signal on their respective base terminals and a driving signal on their respective emitter terminals,

(b) a first emitter drive line connected to the emitter terminals of said first group of driving transistors,

(c) a second emitter drive line connected to the emitter terminals of said second group of driving transistors,

(d) a first blanking transistor having emitter, base and collector terminals connected to said first emitter drive line,

(e) a second blanking transistor having emitter, base and collector terminals connected to said second emitter drive line,

(f) means for applying conditioning signals selectively to the base terminals of said first and second group of driving transistors, said latter means comprising connections between said second plurality of outputs of said decoder and the base terminals of said driving transistors respectively,

(g) means for applying driving signals to said first and second emitter drive lines through the emitter-collector paths of said first and second blanking transistors respectively, said latter means comprising connections between said first pair of outputs of said decoder, indicating respectively odd and even counts in said counter, and the emitter terminals of said first and second blanking transistors, and

(h) means for applying blanking signals to the base terminals of said first and second blanking transistors for causing said first and second blanking transistors to become non-conductive.

References Cited

UNITED STATES PATENTS

2,766,444	10/1956	Sheftelman	340—318
2,933,644	4/1960	Hupp	315—84.5
3,008,067	11/1961	Somlyody	340—168 X
3,020,418	2/1962	Emile	307—88.5
3,304,548	2/1967	Klinikowski	235—92 XR

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UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,395,268 July 30, 1968

David M. Barton

It is certified that error appears in the above identified patent and that said Letters Patent are hereby corrected as shown below:

Column 1, line 28, "This" should read -- The --. Column 3, line 12, after "22" insert a period; line 57, "A.B.C." should read -- A,B,C, --; line 73, after "7" insert a comma. Column 4, line 3, "52A through 52A" should read -- 52A through 52E --; line 22, "will be particular" should read -- will be in particular --; line 63, after "54A" insert -- through 54E --.

Signed and sealed this 13th day of January 1970.

(SEAL)
Attest:

Edward M. Fletcher, Jr.
Attesting Officer

WILLIAM E. SCHUYLER, JR.
Commissioner of Patents