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Owens

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[54] **TEMPERATURE COMPENSATED VOLTAGE REGULATOR HAVING BETA COMPENSATING MEANS**

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[51] **Int. Cl.** **G05f 1/58**

[58] **Field of Search** ..... 323/4, 8, 9, 38, 323/68, 69, 72; 307/270, 296, 297, 299 B, 303, 313

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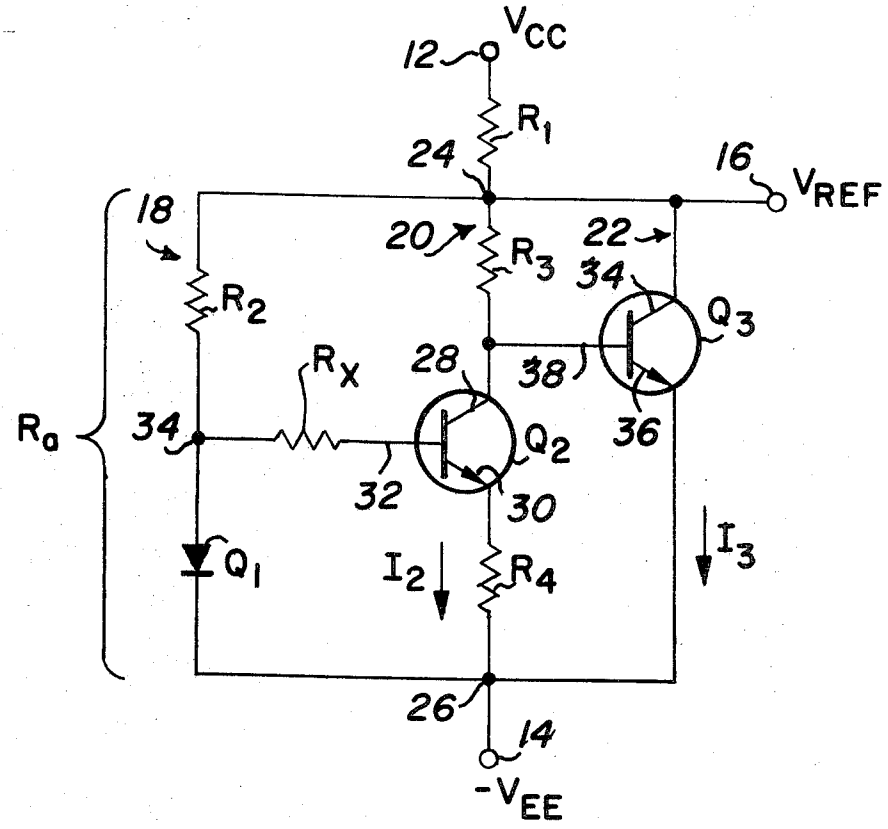
[57] **ABSTRACT**

A temperature compensated voltage regulator circuit having a resistive impedance of a particular value disposed in the base circuit of the first of two cascaded transistor elements to provide compensation for possible beta (β) variations incurred as a result of process variables.

6 Claims, 2 Drawing Figures



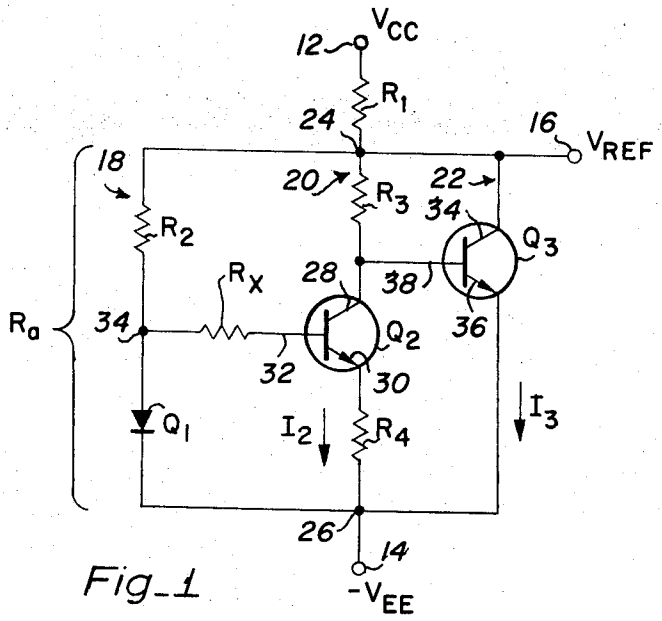

12
V_{CC}
R_1
24
16
V_{REF}
18
20
R_3
22
34
Q_3
R_2
R_X
28
38
R_a
34
Q_2
36
32
30
Q_1
I_2
R_4
I_3
26
14
$-V_{EE}$

Fig_1

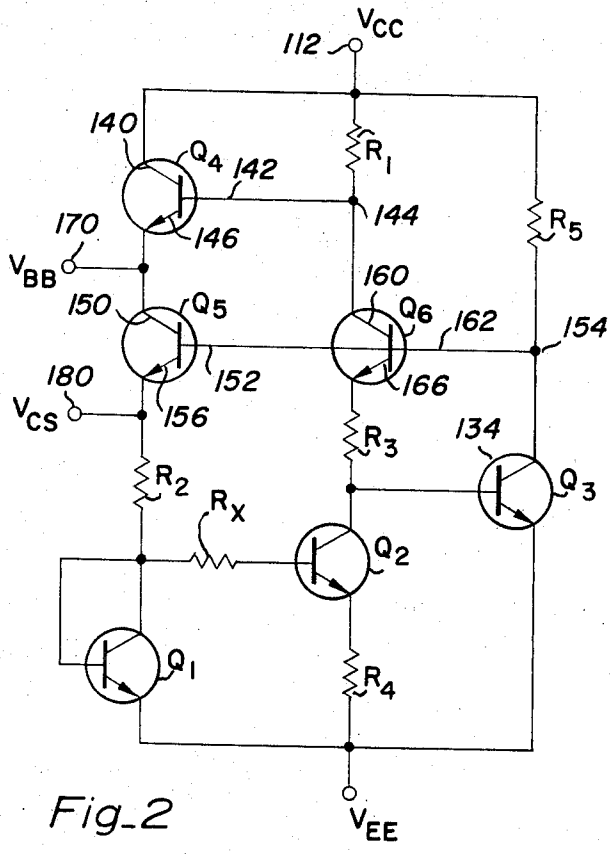

112
V_{CC}
140
Q_4
142
R_1
144
R_5
170
146
V_{BB}
160
150
Q_5
Q_6
162
154
180
152
166
V_{CS}
156
R_3
134
R_2
Q_3
R_X
Q_2
Q_1
R_4
V_{EE}

Fig_2

TEMPERATURE COMPENSATED VOLTAGE REGULATOR HAVING BETA COMPENSATING MEANS

BACKGROUND OF THE INVENTION

The present invention relates generally to reference voltage supply circuitry for integrated circuit applications and more particularly to voltage regulator circuitry for temperature and voltage compensated emitter coupled logic (TVECL) and the like, such circuitry including means for compensating for beta (β) variations incurred as a result of semiconductor process variables.

In electronic circuitry comprised of several discrete integrated circuits, it is important that the bias network be capable of providing a reference voltage that is predictable and constant under all adverse conditions, i.e., the output voltage should be invariant as a function of supply voltage, ambient temperature or semiconductor parameters. Although prior art temperature compensated voltage regulators have long been provided with means to compensate for temperature and voltage variations, no means has heretofore been provided to compensate for V_{BE} variations and base current (I_b) variations resulting from processing variables.

The temperature compensating principle utilized in TVECL drivers is based upon the fact that two transistors operating at different current densities have different base-to-emitter voltage (V_{BE}) temperature coefficients, i.e., the rate of change of base-to-emitter forward voltage versus temperature is different for the two devices, and by coupling the two devices together in a certain manner their differences can be utilized to cancel the temperature coefficient of a third device. Unfortunately however, the previous assumption that run-to-run variations in V_{BE} could be compensated for by the same circuit mechanisms that compensate for temperature variations is not true. For example, in a typical TVECL circuit the range of reference voltage variation ΔV_{REF} caused by process variations in V_{BE} can be expressed as

$$dV_{REF}/dV_{BE} = 1$$

or

$$\Delta V_{REF} = \Delta V_{BE},$$

and may run as high as ±20mV to ±40mV. This is a very significant variation when the reference voltage is used to drive an ECL gate, or the like, since the noise margin of typical ECL integrated circuits is in the range of only 100–150mV.

SUMMARY OF THE PRESENT INVENTION

It is therefore a principle object of the present invention to provide a TVECL voltage regulator circuit for developing a reference voltage that is independent of process variables.

Briefly, the circuit of the present invention includes a first terminal for receiving a first bias potential; a second terminal for receiving a second bias potential; an output terminal at which a reference potential is to be developed; a first resistor coupling the first terminal to the output terminal; a second resistor and a forward biased diode forming a first series circuit coupling the output terminal to the second terminal; a third resistor, a first transistor having a base, an emitter and a collector, and a fourth resistor forming a second series circuit coupling the output terminal to the second terminal; a fifth resistor coupling the base of the first transistor to the junction of the second resistor and the diode; and a second transistor having a base coupled to the collector of the first transistor, a collector coupled to the output terminal, and an emitter coupled to the second terminal.

A primary advantage of the present invention is that the circuit may be utilized to provide a reference voltage which is predictable even though manufacturing process variables cause the various component elements to have slightly varying electrical characteristics.

Other objects and advantages of the present invention will no doubt become apparent to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the several figures of the drawing.

IN THE DRAWING

FIG. 1 of the drawing schematically represents a simplified embodiment of a reference voltage supply circuit having beta (β) compensating means in accordance with the present invention.

FIG. 2 is a diagram schematically illustrating an alternative embodiment of a reference voltage supply circuit for developing a pair of reference voltages.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawing, there is shown In FIG. 1 a simplified schematic diagram representing an integrated circuit (IC) voltage regulator circuit in accordance with the present invention. Although the various elements are shown in the form of discrete classical electrical components, it will be appreciated that these elements are only representative of the electrical characteristics exhibited by various integrated circuit components.

The regulator circuit, sometimes referrzd to as a bias driver, is designated generally by the numeral **10**, and is provided with three external contact points including a first terminal **12** to which a positive supply voltage V_{cc} is applied, a second terminal **14** to which a negative supply voltage V_{ee} is applied, and an output terminal **16** from which the reference voltage V_{REF} may be taken. It will be appreciated that the circuit is basically a voltage dividing circuit including a passive resistance R_1 connected between terminals **12** and **16**, and in series with an active resistance means R_a connected between terminals **16** and **14**.

The active resistance portion of the circuit includes means forming what may generally be viewed as three series circuits **18, 20** and **22** connected in parallel across the circuit nodes **24** and **26**. The first circuit **18** includes a second resistive impedance element represented by the resistor R_2 and a uni-directional current conducting device such as the diode Q_1. The second circuit **20** includes a third resistive impedance element R_3, an NPN transistor Q_2 and a fourth resistive impedance element R_4. The collector **28** of transistor Q_2 is connected to circuit node **4** by resistor R_3, while its emitter **30** is connected to circuit node **26** by resistor R_4. The base **32** of transistor Q_2 is coupled to the junction of resistor R_2 and the anode of diode Q_1 represented by the node **34** by a resistive impedance element R_x having a particular value which will be discussed in detail below. The third circuit **22** is formed

by an NPN transistor Q_3 whose collector **34** is coupled to circuit node **24** and whose emitter **36** is coupled to circuit node **26.** The base **38** of transistor Q_3 is coupled to the collector **28** of transistor Q_2.

Assuming now for purposes of illustration that the base resistor R_x is not in the circuit and base **32** is connected directly to circuit node **34,** the reference voltage V_{REF} can be expressed as

$$V_{REF} = \alpha_2 I_2 R_3 + V_{BE3} + I_{b3} R_3 \quad (1)$$

where $I_2 = V_{BE1} - V_{BE2}/R_4$ (2)

β_2 is the ratio of the collector current I_{c2} to the emitter current I_{e2} of transistor Q_2,

I_{b3} is the base current of transistor Q_3, and

$V_{BE1}V_{BE2}$ and V_{BE3} are the base-to-emitter voltages of the transistors having like numbered subscripts. Substituting equation (2) into equation (1) gives

$$V_{REF} = \alpha_2 R_3 [(V_{BE1} - V_{BE2})/R_4] + V_{BE3} + I_{b3} R_3 \quad (3)$$

Differentiating equation (3) with respect to the first variable base-to-emitter voltage V_{BE}, it can be shown that

$$dV_{REF}/dV_{BE} = 1 \quad (4)$$

or

$$\Delta V_{REF} = \Delta V_{BE3} \quad (5)$$

This variation, of perhaps ±20mV to ±40mV in a typical circuit, is of course very significant when the reference voltage is used to drive an ECL gate since the noise margin of typical ECL integrated circuits is in the range of 100–150mV.

The second variable that causes the reference voltage to vary is the base current. This relationship can be expressed as

$$V_{REF} = (I_2 - I_{b2})\ R_3 + V_{BE3} + I_{b3} R_3 \quad (6)$$

and taking the partial derivative

$$\delta V_{REF} = -\delta I_{b2} R_3 + \delta I_{b3} R_3 \quad (7)$$

the reference voltage variation can be expressed as

$$\Delta V_{REF} \approx (\Delta I_{b3} - \Delta I_{b2})\ R_3. \quad (8)$$

In a typical circuit wherein

$I_3 = 4mA$ $R_3 = 600\Omega$

$I_2 = 2mA$ $\beta_{NOM} \approx 100$, $\beta_{min} = 60$

the ΔV_{REF} will be found to be about 8mV. Therefore, by adding the two components of variation it can be seen that the total variation in V_{REF} lies within the range of 28mV to 48mV.

Since ECL gates require two reference voltages, the above error must be multiplied by a factor of two. Thus, a typical ECL gate could experience a noise margin reduction of approximately 56mV to 96mV. Where the initial noise margin is 125mV, it is obvious that such a reduction in noise margin would be catastrophic.

Since it is known that a major portion of the ΔV_{BE} resulting from process variation is a function of beta (β), i.e.,

$$\Delta V_{BE} \approx K\Delta\beta \quad (9)$$

where K is a constant and since the fractiOn of ΔV_{BE} that is a function of ΔB is very large at the low current levels typically assigned to the transistor Q_3, most of the $\Delta V_{REF}/\Delta V_{BE3}$ can be eliminated by inserting a resistor R_x in the base of transistor Q_2. As a result of so doing, equation (**1**) can be rewritten as

$$V_{REF} = [(V_{BE1} - V_{BE2} - I_{b2}R_x/R_4) - I_{b2}]R_3 + V_{BE3} + I_{b3}R_3 \quad (10)$$

The change in V_{REF} as a function of V_{BE} and I_b is then

$$dV_{REF} = -R_x\ R_3/R_4\ dI_{b2} - R_3 dI_{b2} + dV_{BE3} + R_3 dI_{b3}. \quad (11)$$

If V_{REF} is invariant as a function of I_b and V_{BE}, then dV_{REF} may be set equal to zero and equation (11) may be solved for R_x to result in the expression

$$R_x \approx \Delta V_{BE3} + R_3\Delta I_{b3} - R_3\ \Delta I_{b2}/(R_3/R_4)\ \Delta I_{b2}$$

Thus, by chosing a value of R_x capable of satisfying the above equation, the reference voltage variations caused by ΔV_{BE} and ΔI_b can be eliminated. In examples such as the above, typical values for R_x lie within the range of 250Ω to 1,000Ω.

To illustrate application of the present invention in a typical circuit for developing a pair of reference voltages, reference is made to FIG. **2** of the drawing. In this embodiment, which is designed to provide the two bias voltages, V_{BB} and V_{CS}, three additional transistors Q_4, Q_5 and Q_6, and an additional resistor R_5 is added to the circuit of FIG. **1.** In this circuit, the collector **140** of transistor Q_4 is coupled to terminal **112** while its base **142** is coupled to the lower end of resistor R_1 at **144** and its emitter **146** is coupled to the collector **150** of transistor Q_5.

The base **152** of transistor Q_5 is coupled to the junction **154** of the lower end of resistor R_5 and the collector **134** of transistor Q_3. The emitter **156** of transistor Q_5 is coupled to the upper end of resistor R_2. The collector **160** of transistor Q_6 is also coupled to circuit point **144,** while its base **162** is coupled to circuit point **154,** and its emitter **166** is coupled to the upper end Of resistor R_3. The reference voltage V_{BB} is taken at terminal **170** and the reference voltage V_{CS} is taken at terminal **180.**

The remainder of the circuit elements are as illustrated in the previous embodiment. For purposes of illustration a diode connected transistor Q_1 is shown in place of the simple diode shown in FIG. **1.**

As in the previous embodiment, if the process variation is not compensated for, the ΔV_{BE3} will be reflected

into the V_{CS} reference and the ΔV_{BE4} will be reflected into the V_{BB} reference. Since process variations in V_{BE} are of the same sign on the same chip, the magnitudes of V_{CS} and V_{BB} will change approximately the same amount as the process variation ΔV_{BE}, therefore, the noise margin degradation vs. process variation ΔV_{BE} is approximately equal to $\Delta V_{BE3} + \Delta V_{BE4}$. At the usual current levels

$$\Delta V_{BE3} \approx \Delta V_{BE4} \approx 20\text{–}30\text{mV}. \quad (13)$$

By inserting the resistor R_x in the base of transistor Q_2, as described above, the process variations ΔV_{BE} as well as the voltage variations across resistors R_1 and R_3 caused by variations in the base currents of transistors Q_3 and Q_4 will be substantially reduced. Accordingly, the resulting improvement in noise margin will be between 30mV and 70mV depending upon whether the bias driver is used in an SSI or an MSI integrated circuit.

Using the ratio explained above, it can be shown that

$$R_x = \Delta V_{BE3}/\alpha\Delta I_{b_2}\ (R_3/R_4)\ . \quad (14)$$

The change in voltage across R_x caused by $\Delta\beta$ changes current through R_4, i.e.,

$$I_{(R4)} = V_{BE1} - V_{BE2} - V_{R_x}/R_4 \quad (15)$$

and

$$\Delta I_{R4} = -1/R_4\Delta V_{R_x} \quad (16)$$

The change in voltage across R_3 caused by the change in voltage across R_x is $\Delta V_{R3} = \Delta I_{R4}\ \alpha R_3$ or

$$\Delta V_{R3} = -\alpha(R_3/R_4)\Delta V_{R_x} \quad (18)$$

If

$$\Delta V_{R_3} = -\Delta V_{BE3} \quad (19)$$

the effects of the process variation ΔV_{BE} are cancelled. Therefore, the following equation may be written:

$$\Delta V_{R_x}\alpha(R_3/R_4) = \Delta V_{BE3} \quad (20)$$

By choosing a value of R_x from equation (14), equation (20) can be realized.

With the ill effects of ΔV_{BE3} eliminated, the R_x can be further tailored to cancel the base current loading effects on R_3 or R_1. If the emitter currents of Q_3 and Q_4 are equal and much greater than I_{E2} and if R_3 equals R_1, then $\Delta I_{b3}R_3$ will be totally eliminated, and $\Delta I_{b4}R_1$ will be reduced by 50 percent.

Letting

$$\Delta I_{R_4}\alpha R_3 = -\Delta I_{b3}R_3 \quad (21)$$

and substituting

$$\Delta I_{R_4} = -\Delta I_{b2}(R_x/R_4) \quad (22)$$

then

$$\alpha(\Delta I_{b2}\ R_x/R_4) = \Delta I_{b3} \quad (23)$$

or

$$R_x = R_4\Delta I_{b3}/\alpha\Delta I_{\ b2} \quad (24)$$

Thus, the total value of R_x necessary to compensate for the process variables $\Delta V_{BE3} + \Delta V_{BE4} + \Delta I_{b3}R_3 + \Delta I_{b3}R_1\alpha$ is, from equations (14) and (24)

$$[R_x = [\Delta V_{BE3}/\Delta I_{b2}\alpha(R_3/R_4)] + [R_4\Delta I_{b3}/\alpha\Delta I_{b2}]$$

The first term in the above equation is general, however the second term depends upon the emitter currents in transistors Q_3 and Q_4 and the relative compensation desired at V_{BB} and V_{CS}. If I_{E3} is not equal to I_{E4}, then $\Delta I_{b3}R_3$ is not equal to $\Delta I_{b4}R_1$ and $\Delta I_{b4}R_1$ is not reduced by 50 percent. Thus, either $\Delta I_{b3}R_3$ or $\Delta I_{b4}R_1$ can be compensated for totally, but not both terms. In most applications, it should be more desirable to partially undercompensate one term or partially overcompensate for the other.

In summary it may be emphasized that the principle features and advantages of the present invention is the elimination of the effects of V_{BE} process variations (ΔV_{BE3} and ΔV_{BE4}) and the significant reduction of ΔI_bR effects.

What is claimed is:

1. A temperature compensated voltage regulator circuit including beta compensating means, comprising:

a first terminal for receiving a first bias potential;

a second terminal for receiving a second bias potential;

an output terminal at which a reference potential is developed;

first resistive impedance means coupling said first terminal to said output terminal;

a second resistive impedance means and a forward biased diode means forming a first series circuit coupling said output terminal to said second terminal;

a third resistive impedance means, a first transistor device having a base, an emitter and a collector, and a fourth resistive impedance means forming a second series circuit coupling said output terminal to said second terminal;

a fifth resistive impedance means coupling the base of said first transistor device to the junction of said second resistive impedance means and said diode means; and

a second transistor device having a base coupled to the collector of said first transistor device, a collector coupled to said output terminal and an emitter coupled to said second terminal.

2. A temperature compensated voltage regulator circuit as recited in claim **1** wherein said fifth resistive impedance means has a resistive impedance R_x selected to satisfy the equation

$$R_x = \Delta V_{BE3} + R_3 \Delta I_{b3} - R_3 \Delta I_{b2}/(R_3/R_4) \Delta I_{b2}$$

where

R_3 is the resistive impedance of said third impedance means;

R_4 is the resistive impedance of said fourth impedance means;

ΔV_{BE3} is the base-emitter forward voltage variation of said second transistor device;

ΔI_{b2} is the base current variation of said first transistor device; and

ΔI_{b3} is the base current variation of said second transistor device.

3. A temperature compensated voltage regulator circuit including beta compensating means comprising:

a first terminal for receiving a first bias potential;

a second terminal for receiving a second bias potential;

an output terminal at which a reference potential is to be developed;

a first resistive impedance means coupling said first terminal to said output terminal;

a second resistive impedance means and a forward biased diode means forming a series circuit coupling said output terminal to said second terminal;

a third resistive impedance means;

a fourth and a fifth resistive impedance means;

a first transistor device having a first base coupled to the junction of said second resistive impedance means and said diode means by said third resistive impedance means, a first collector coupled to said output terminal by said fourth resistive impedance means, and a first emitter coupled to said second terminal by said fifth resistive impedance means; and

a second transistor device having a second base coupled to said first collector, a second collector coupled to said output terminal, and a second emitter coupled to said second terminal.

4. A temperature compensated voltage regulator circuit as recited in claim **3** wherein said fifth resistive impedance means has a resistive impedance R_x selected to satisfy the equation

$$R_x = \Delta V_{BE3} + R_3 \Delta I_{b3} - R_3 \Delta I_{b2}/(R_3/R_4) \Delta I_{b2}$$

where

R_3 is the resistive impedance of said fourth impedance means;

R_4 is the resistive impedance of said fifth impedance means;

ΔV_{BE3} is the base emitter forward voltage variation of said second transistor device;

ΔI_{b2} is the base current variation of said first transistor device; and

ΔI_{b3} is the base current variation of said second transistor device.

5. A temperature compensated voltage regulator circuit including beta compensating means, comprising:

a first terminal for receiving a first bias potential;

a second terminal for receiving a second bias terminal;

a third terminal at which a first reference potential is to be developed;

a fourth terminal at which a second reference potential is to be developed;

a first resistive impedance means;

a first transistor device having a first base coupled to said first terminal by said first resistive impedance means, a first collector coupled to said first terminal and a first emitter coupled to said third terminal;

a second resistive impedance means;

a second transistor device having a second base coupled to said first terminal by said second resistive impedance means, a second collector coupled to said third terminal and a second emitter coupled to said fourth terminal;

a third resistive impedance means and a forward biased diode means forming a series circuit coupling said fourth terminal to said second terminal;

a third transistor device having a third base coupled to said second base, a third collector coupled to said first base and a third emitter;

a fourth resistive impedance means;

a fifth resistive impedance means;

a sixth resistive impedance means;

a fourth transistor device having a fourth base coupled to the junction of said third impedance means and said diode means by said fifth impedance means, a fourth collector coupled to said third emitter by said fourth impedance means and a fourth emitter coupled to said second terminal by said sixth impedance means; and

a fifth transitor device having a fifth base coupled to said fourth collector, a fifth collector coupled to said first terminal through said second resistive impedance means and a fifth emitter coupled to said second terminal.

6. A temperature compensated voltage regulator circuit as recited in claim **5** wherein said fifth resistive impedance means has a resistive impedance R_x selected to satisfy the equation

$$R_x = \Delta V_{BE3} + R_3 \Delta I_{b3} - R_3 \Delta I_{b2}/(R_3/R_4) \Delta I_{b2}$$

where

R_3 is the resistive impedance of said fourth impedance means;

R_4 is the resistive impedance of said sixth impedance means;

ΔV_{BE3} is the base-emitter forward voltage variation of said fifth transistor device;

ΔI_{b2} is the base current variation of said fourth transistor device; and

ΔI_{b3} is the base current variation of said fifth transistor device.

* * * * *