(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 December 2015 (30.12.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/196492 A1

(51) International Patent Classification:
G06F 9/48 (2006.01) *H04W 52/02* (2009.01)
G06F 9/305 (2006.01)

(21) International Application Number:
PCT/CN2014/081068

(22) International Filing Date:
28 June 2014 (28.06.2014)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: VIRTUAL SENSOR HUB FOR ELECTRONIC DEVICES RELATED APPLICATIONS

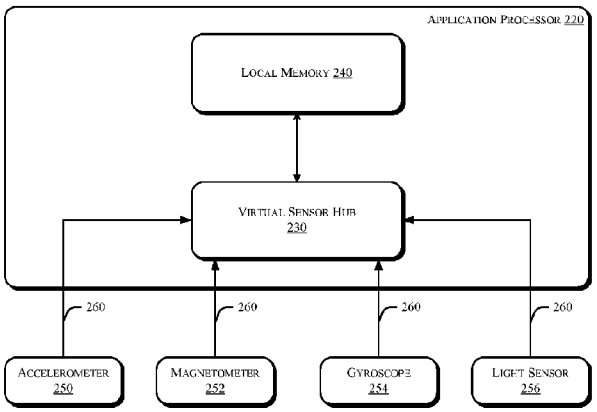

FIG. 2

(57) Abstract: An application processor (220) comprises a memory (240) and a virtual sensor hub (230) which is coupled to the memory (240). Said hub (230) comprises: a plurality of sensor drivers, and a sensor fusion driver communicatively coupled to the plurality of sensor drivers, wherein the sensor fusion driver receives inputs from the plurality of sensor drivers and processes the data to generate sensor data. Due to this design of said hub (230), the electronic device can achieve the effect of low power consumption.

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VIRTUAL SENSOR HUB FOR ELECTRONIC DEVICES

RELATED APPLICATIONS

[0001] None.

BACKGROUND

[0002] The subject matter described herein relates generally to the field of electronic devices and more particularly to a virtual sensor hub for electronic devices.

[0003] Electronic devices such as laptop computers, tablet computing devices, electronic readers, mobile phones, and the like may include location sensors such as global positioning sensors that can determine a location of the electronic device. Further such electronic devices may include sensors, e.g., accelerometers, gyroscopes, etc., for positioning, orientation, motion detection, and detection of other environmental characteristics. Existing electronic device architectures incorporate a microcontroller to act as a sensor hub. Techniques which enable an electronic device to process inputs from such sensors in an application processor on the electronic device may find utility.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The detailed description is described with reference to the accompanying figures.

[0005] Fig. 1 is a schematic illustration of an electronic device which may be adapted to implement a virtual sensor hub in accordance with some examples.

[0006] Fig. 2 is a high-level schematic illustration of an exemplary architecture to implement a virtual sensor hub in accordance with some examples.

[0007] Fig. 3 is a schematic illustration of logic components of a virtual sensor hub in accordance with some examples.

[0008] Figs. 4-5 are flowcharts illustrating operations in a method to implement a virtual sensor hub in accordance with some examples.

[0009] Figs. 6-10 are schematic illustrations of electronic devices which may be adapted to implement smart frame toggling in accordance with some examples.

DETAILED DESCRIPTION

[0010] Described herein are exemplary systems and methods to implement a virtual sensor hub in electronic devices. In the following description, numerous specific details are set forth to provide a thorough understanding of various examples. However, it will be understood by those skilled in the art that the various examples may be practiced without the specific details. In other instances, well-known methods, procedures, components, and circuits have not been illustrated or described in detail so as not to obscure the particular examples.

[0011] As described above, it may be useful to provide electronic devices with a virtual sensor hub which may be implemented in a application processor, rather than in a separate controller. The subject matter described herein addresses these and other issues by providing a virtual sensor hub which may be implemented in logic in an application processor of the electronic device. In some examples, the virtual sensor hub receives inputs from one or more sensors coupled to the virtual sensor hub by a communication bus and processes the inputs to generate sensor data.

[0012] Additional features and operating characteristics of the virtual sensor hub and of electronic devices are described below with reference to Figs. 1-10.

[0013] Fig. 1 is a schematic illustration of an electronic device 100 which may be adapted to implement a virtual sensor hub in accordance with some examples. In

various examples, electronic device 100 may include or be coupled to one or more accompanying input/output devices including a display, one or more speakers, a keyboard, one or more other I/O device(s), a mouse, a camera, or the like. Other exemplary I/O device(s) may include a touch screen, a voice-activated input device, a track ball, a geolocation device, an accelerometer/gyroscope, biometric feature input devices, and any other device that allows the electronic device 100 to receive input from a user.

[0014] The electronic device 100 includes system hardware 120 and memory 140, which may be implemented as random access memory and/or read-only memory. A file store may be communicatively coupled to electronic device 100. The file store may be internal to electronic device 100 such as, *e.g.*, eMMC, SSD, one or more hard drives, or other types of storage devices. Alternatively, the file store may also be external to electronic device 100 such as, *e.g.*, one or more external hard drives, network attached storage, or a separate storage network.

[0015] System hardware 120 may include one or more processors 122, graphics processors 124, network interfaces 126, and bus structures 128. In one embodiment, processor 122 may be embodied as an Intel® Atom™ processors, Intel® Atom™ based System-on-a-Chip (SOC) or Intel ® Core2 Duo® or i3/i5/i7 series processor available from Intel Corporation, Santa Clara, California, USA. As used herein, the term "processor" means any type of computational element, such as

but not limited to, a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, or any other type of processor or processing circuit.

[0016] Graphics processor(s) 124 may function as adjunct processor that manages graphics and/or video operations. Graphics processor(s) 124 may be integrated onto the motherboard of electronic device 100 or may be coupled via an expansion slot on the motherboard or may be located on the same die or same package as the Processing Unit.

[0017] In one embodiment, network interface 126 could be a wired interface such as an Ethernet interface (see, e.g., Institute of Electrical and Electronics Engineers/IEEE 802.3-2002) or a wireless interface such as an IEEE 802.11a, b or g-compliant interface (see, e.g., IEEE Standard for IT-Telecommunications and information exchange between systems LAN/MAN--Part II: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications Amendment 4: Further Higher Data Rate Extension in the 2.4 GHz Band, 802.11G-2003). Another example of a wireless interface would be a general packet radio service (GPRS) interface (see, e.g., Guidelines on GPRS Handset Requirements, Global System for Mobile Communications/GSM Association, Ver. 3.0.1, December 2002).

[0018] Bus structures 128 connect various components of system hardware 128. In one embodiment, bus structures 128 may be one or more of several types of bus structure(s) including a memory bus, a peripheral bus or external bus, and/or a local bus using any variety of available bus architectures including, but not limited to, 11-bit bus, Industrial Standard Architecture (ISA), Micro-Channel Architecture (MSA), Extended ISA (EISA), Intelligent Drive Electronics (IDE), VESA Local Bus (VLB), Peripheral Component Interconnect (PCI), Universal Serial Bus (USB), Advanced Graphics Port (AGP), Personal Computer Memory Card International Association bus (PCMCIA), and Small Computer Systems Interface (SCSI), a High Speed Synchronous Serial Interface (HSI), a Serial Low-power Inter-chip Media Bus (SLIMbus®), or the like.

[0019] Electronic device 100 may include an RF transceiver 130 to transceive RF signals, a Near Field Communication (NFC) radio 134, and a signal processing module 132 to process signals received by RF transceiver 130. RF transceiver may implement a local wireless connection via a protocol such as, e.g., Bluetooth or 802.11X. IEEE 802.11a, b or g-compliant interface (see, e.g., IEEE Standard for IT-Telecommunications and information exchange between systems LAN/MAN--Part II: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications Amendment 4: Further Higher Data Rate Extension in the 2.4 GHz Band, 802.11G-2003). Another example of a wireless interface would be a

WCDMA, LTE, general packet radio service (GPRS) interface (see, e.g., Guidelines on GPRS Handset Requirements, Global System for Mobile Communications/GSM Association, Ver. 3.0.1, December 2002).

[0020] Electronic device 100 may further include one or more input/output interfaces such as, e.g., a keypad 136 and a display 138. In some examples electronic device 100 may not have a keypad and use the touch panel for input.

[0021] Memory 140 may include an operating system 142 for managing operations of electronic device 100. In one embodiment, operating system 142 includes a hardware interface module 154 that provides an interface to system hardware 120. In addition, operating system 140 may include a file system 150 that manages files used in the operation of electronic device 100 and a process control subsystem 152 that manages processes executing on electronic device 100.

[0022] Operating system 142 may include (or manage) one or more communication interfaces 146 that may operate in conjunction with system hardware 120 to transceive data packets and/or data streams from a remote source. Operating system 142 may further include a system call interface module 144 that provides an interface between the operating system 142 and one or more application modules resident in memory 130. Operating system 142 may be embodied as a UNIX operating system or any derivative thereof (*e.g.*, Linux, Android, *etc.*) or as a Windows® brand operating system, or other operating systems.

[0023] Fig. 2 is a high-level schematic illustration of an exemplary architecture to implement a virtual sensor hub 230 in electronic devices. Referring to Fig. 2, an application processor 220 may be embodied as general purpose processor 122 or as a low-power controller. Application processor 220 may comprise a virtual sensor hub 230 to receive inputs from one or more sensors via a communication bus 260, which in some examples may be implemented as an inter-integrated circuit (I2C) bus. As described above, in some examples the a virtual sensor hub 230 may be implemented as logic instructions executable on application processor 220, e.g., as software or firmware. Local memory 240 may be implemented using volatile and/or non-volatile memory.

[0024] Virtual sensor hub 230 may be communicatively coupled to one or more sensors which provide signals that indicate whether an electronic device is in motion or other environmental conditions. For example, the sensors may include an accelerometer 250, a magnetometer 252, a gyroscope 254, and a light sensor 256.

[0025] Fig. 3 is a schematic illustration of logic components of a virtual sensor hub in accordance with some examples. Referring to Fig. 3, in some examples the virtual sensor hub 220 includes a plurality of drivers including an accelerometer driver 350 to manage communication with the accelerometer 250, a magnetometer driver 352 to manage communication with the magnetometer 252, a

gyroscope driver 354 to manage communication with the gyroscope 254 and a light sensor driver to manage communication with the light sensor 256.

[0026] Data outputs from the respective drivers 350, 352, 354, 356 are input to a sensor fusion driver, which processes the data to generate sensor data. The sensor data may be passed to a human interface driver (HID) 340, which manages communication with one or more human interface devices, e.g., a display, microphone, vibrator, or the like.

[0027] Having described various structures of a system to implement a virtual sensor hub in electronic devices, operating aspects of a system will be explained with reference to Figs. 4-5, which are flowcharts illustrating operations in a method to implement a virtual sensor hub in accordance with some examples. The operations depicted in the flowcharts of Figs. 4-5 may be implemented by the virtual sensor hub 220, alone or in combination with other component of electronic device 100.

[0028] Referring to Fig. 4, at operation 410 the various sensors generate sensor outputs. For example, the accelerometer 250 may generate accelerometer data in response to detecting motion in the electronic device. Similarly, the magnetometer 252 and gyroscope 254 may generate magnetometer data in response to a change in position or orientation of the electronic device 100. At operation 415 data from the various sensors are placed on the communication bus 260 that is coupled directly to

the virtual sensor hub 230. Referring to Fig. 5, at operation 510 the virtual sensor hub 220 receives data from the various sensors. For example the virtual sensor hub 220 receives data from at least one of the accelerometer 250, magnetometer 252, gyroscope, and light sensor 256. At operation 515 the virtual sensor hub 220 processes the data received to generate sensor data, and at operation 520 at least some of the sensor data is output to a human interface device (HID) driver 340 for presentation on a human interface device, e.g., a display, , speaker, or the like.

[0029] As described above, in some examples the electronic device may be embodied as a computer system. Fig. 6 illustrates a block diagram of a computing system 600 in accordance with an example. The computing system 600 may include one or more central processing unit(s) 602 or processors that communicate via an interconnection network (or bus) 604. The processors 602 may include a general purpose processor, a network processor (that processes data communicated over a computer network 603), or other types of a processor (including a reduced instruction set computer (RISC) processor or a complex instruction set computer (CISC)). Moreover, the processors 602 may have a single or multiple core design. The processors 602 with a multiple core design may integrate different types of processor cores on the same integrated circuit (IC) die. Also, the processors 602 with a multiple core design may be implemented as symmetrical or asymmetrical multiprocessors. In an example, one or more of the processors 602 may be the same

or similar to the processors 102 of Fig. 1. For example, one or more of the processors 602 may include the control unit 120 discussed with reference to Figs. 1-3. Also, the operations discussed with reference to Figs. 3-5 may be performed by one or more components of the system 600.

[0030] A chipset 606 may also communicate with the interconnection network 604. The chipset 606 may include a memory control hub (MCH) 608. The MCH 608 may include a memory controller 610 that communicates with a memory 612 (which may be the same or similar to the memory 130 of Fig. 1). The memory 412 may store data, including sequences of instructions, that may be executed by the processor 602, or any other device included in the computing system 600. In one example, the memory 612 may include one or more volatile storage (or memory) devices such as random access memory (RAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), static RAM (SRAM), or other types of storage devices. Nonvolatile memory may also be utilized such as a hard disk. Additional devices may communicate via the interconnection network 604, such as multiple processor(s) and/or multiple system memories.

[0031] The MCH 608 may also include a graphics interface 614 that communicates with a display device 616. In one example, the graphics interface 614 may communicate with the display device 616 via an accelerated graphics port (AGP). In an example, the display 616 (such as a flat panel display) may

communicate with the graphics interface 614 through, for example, a signal converter that translates a digital representation of an image stored in a storage device such as video memory or system memory into display signals that are interpreted and displayed by the display 616. The display signals produced by the display device may pass through various control devices before being interpreted by and subsequently displayed on the display 616.

[0032] A hub interface 618 may allow the MCH 608 and an input/output control hub (ICH) 620 to communicate. The ICH 620 may provide an interface to I/O device(s) that communicate with the computing system 600. The ICH 620 may communicate with a bus 622 through a peripheral bridge (or controller) 624, such as a peripheral component interconnect (PCI) bridge, a universal serial bus (USB) controller, or other types of peripheral bridges or controllers. The bridge 624 may provide a data path between the processor 602 and peripheral devices. Other types of topologies may be utilized. Also, multiple buses may communicate with the ICH 620, e.g., through multiple bridges or controllers. Moreover, other peripherals in communication with the ICH 620 may include, in various examples, integrated drive electronics (IDE) or small computer system interface (SCSI) hard drive(s), USB port(s), a keyboard, a mouse, parallel port(s), serial port(s), floppy disk drive(s), digital output support (e.g., digital video interface (DVI)), or other devices.

[0033] The bus 622 may communicate with an audio device 626, one or more disk drive(s) 628, and a network interface device 630 (which is in communication with the computer network 603). Other devices may communicate via the bus 622. Also, various components (such as the network interface device 630) may communicate with the MCH 608 in some examples. In addition, the processor 602 and one or more other components discussed herein may be combined to form a single chip (e.g., to provide a System on Chip (SOC)). Furthermore, the graphics accelerator 616 may be included within the MCH 608 in other examples.

[0034] Furthermore, the computing system 600 may include volatile and/or nonvolatile memory (or storage). For example, nonvolatile memory may include one or more of the following: read-only memory (ROM), programmable ROM (PROM), erasable PROM (EPROM), electrically EPROM (EEPROM), a disk drive (e.g., 628), a floppy disk, a compact disk ROM (CD-ROM), a digital versatile disk (DVD), flash memory, a magneto-optical disk, or other types of nonvolatile machine-readable media that are capable of storing electronic data (e.g., including instructions).

[0035] Fig. 7 illustrates a block diagram of a computing system 700, according to an example. The system 700 may include one or more processors 702-1 through 702-N (generally referred to herein as "processors 702" or "processor 702"). The processors 702 may communicate via an interconnection network or bus 704. Each processor may include various components some of which are only discussed

with reference to processor 702-1 for clarity. Accordingly, each of the remaining processors 702-2 through 702-N may include the same or similar components discussed with reference to the processor 702-1.

[0036] In an example, the processor 702-1 may include one or more processor cores 706-1 through 706-M (referred to herein as "cores 706" or more generally as "core 706"), a shared cache 708, a router 710, and/or a processor control logic or unit 720. The processor cores 706 may be implemented on a single integrated circuit (IC) chip. Moreover, the chip may include one or more shared and/or private caches (such as cache 708), buses or interconnections (such as a bus or interconnection network 712), memory controllers, or other components.

[0037] In one example, the router 710 may be used to communicate between various components of the processor 702-1 and/or system 700. Moreover, the processor 702-1 may include more than one router 710. Furthermore, the multitude of routers 710 may be in communication to enable data routing between various components inside or outside of the processor 702-1.

[0038] The shared cache 708 may store data (e.g., including instructions) that are utilized by one or more components of the processor 702-1, such as the cores 706. For example, the shared cache 708 may locally cache data stored in a memory 714 for faster access by components of the processor 702. In an example, the cache 708 may include a mid-level cache (such as a level 2 (L2), a level 3 (L3), a level 4

(L4), or other levels of cache), a last level cache (LLC), and/or combinations thereof. Moreover, various components of the processor 702-1 may communicate with the shared cache 708 directly, through a bus (e.g., the bus 712), and/or a memory controller or hub. As shown in Fig. 7, in some examples, one or more of the cores 706 may include a level 1 (L1) cache 716-1 (generally referred to herein as "L1 cache 716"). In one example, the control unit 720 may include logic to implement the operations described above with reference to the memory controller 122 in Fig. 2.

[0039] Fig. 8 illustrates a block diagram of portions of a processor core 706 and other components of a computing system, according to an example. In one example, the arrows shown in Fig. 8 illustrate the flow direction of instructions through the core 706. One or more processor cores (such as the processor core 706) may be implemented on a single integrated circuit chip (or die) such as discussed with reference to Fig. 7. Moreover, the chip may include one or more shared and/or private caches (e.g., cache 708 of Fig. 7), interconnections (e.g., interconnections 704 and/or 112 of Fig. 7), control units, memory controllers, or other components.

[0040] As illustrated in Fig. 8, the processor core 706 may include a fetch unit 802 to fetch instructions (including instructions with conditional branches) for execution by the core 706. The instructions may be fetched from any storage devices such as the memory 714. The core 706 may also include a decode unit 804 to decode

the fetched instruction. For instance, the decode unit 804 may decode the fetched instruction into a plurality of uops (micro-operations).

[0041] Additionally, the core 706 may include a schedule unit 806. The schedule unit 806 may perform various operations associated with storing decoded instructions (e.g., received from the decode unit 804) until the instructions are ready for dispatch, e.g., until all source values of a decoded instruction become available. In one example, the schedule unit 806 may schedule and/or issue (or dispatch) decoded instructions to an execution unit 808 for execution. The execution unit 808 may execute the dispatched instructions after they are decoded (e.g., by the decode unit 804) and dispatched (e.g., by the schedule unit 806). In an example, the execution unit 808 may include more than one execution unit. The execution unit 808 may also perform various arithmetic operations such as addition, subtraction, multiplication, and/or division, and may include one or more an arithmetic logic units (ALUs). In an example, a co-processor (not shown) may perform various arithmetic operations in conjunction with the execution unit 808.

[0042] Further, the execution unit 808 may execute instructions out-of-order. Hence, the processor core 706 may be an out-of-order processor core in one example. The core 706 may also include a retirement unit 810. The retirement unit 810 may retire executed instructions after they are committed. In an example, retirement of the executed instructions may result in processor state being committed from the

execution of the instructions, physical registers used by the instructions being de-allocated, etc.

[0043] The core 706 may also include a bus unit 714 to enable communication between components of the processor core 706 and other components (such as the components discussed with reference to Fig. 8) via one or more buses (e.g., buses 804 and/or 812). The core 706 may also include one or more registers 816 to store data accessed by various components of the core 706 (such as values related to power consumption state settings).

[0044] Furthermore, even though Fig. 7 illustrates the control unit 720 to be coupled to the core 706 via interconnect 812, in various examples the control unit 720 may be located elsewhere such as inside the core 706, coupled to the core via bus 704, etc.

[0045] In some examples, one or more of the components discussed herein can be embodied as a System On Chip (SOC) device. Fig. 9 illustrates a block diagram of an SOC package in accordance with an example. As illustrated in Fig. 9, SOC 902 includes one or more processor cores 920, one or more graphics processor cores 930, an Input/Output (I/O) interface 940, and a memory controller 942. Various components of the SOC package 902 may be coupled to an interconnect or bus such as discussed herein with reference to the other figures. Also, the SOC package 902 may include more or less components, such as those discussed herein

with reference to the other figures. Further, each component of the SOC package 902 may include one or more other components, e.g., as discussed with reference to the other figures herein. In one example, SOC package 902 (and its components) is provided on one or more Integrated Circuit (IC) die, e.g., which are packaged into a single semiconductor device.

[0046] As illustrated in Fig. 9, SOC package 902 is coupled to a memory 960 (which may be similar to or the same as memory discussed herein with reference to the other figures) via the memory controller 942. In an example, the memory 960 (or a portion of it) can be integrated on the SOC package 902.

[0047] The I/O interface 940 may be coupled to one or more I/O devices 970, e.g., via an interconnect and/or bus such as discussed herein with reference to other figures. I/O device(s) 970 may include one or more of a keyboard, a mouse, a touchpad, a display, an image/video capture device (such as a camera or camcorder/video recorder), a touch surface, a speaker, or the like.

[0048] Fig. 10 illustrates a computing system 1000 that is arranged in a point-to-point (PtP) configuration, according to an example. In particular, Fig. 10 shows a system where processors, memory, and input/output devices are interconnected by a number of point-to-point interfaces. The operations discussed with reference to Fig. 2 may be performed by one or more components of the system 1000.

[0049] As illustrated in Fig. 10, the system 1000 may include several processors, of which only two, processors 1002 and 1004 are shown for clarity. The processors 1002 and 1004 may each include a local memory controller hub (MCH) 1006 and 1008 to enable communication with memories 1010 and 1012. MCH 1006 and 1008 may include the memory controller 120 and/or logic 125 of Fig. 1 in some examples.

[0050] In an example, the processors 1002 and 1004 may be one of the processors 702 discussed with reference to Fig. 7. The processors 1002 and 1004 may exchange data via a point-to-point (PtP) interface 1014 using PtP interface circuits 1016 and 1018, respectively. Also, the processors 1002 and 1004 may each exchange data with a chipset 1020 via individual PtP interfaces 1022 and 1024 using point-to-point interface circuits 1026, 1028, 1030, and 1032. The chipset 1020 may further exchange data with a high-performance graphics circuit 1034 via a high-performance graphics interface 1036, e.g., using a PtP interface circuit 1037.

[0051] As shown in Fig. 10, one or more of the cores 106 and/or cache 108 of Fig. 1 may be located within the processors 1004. Other examples, however, may exist in other circuits, logic units, or devices within the system 1000 of Fig. 10. Furthermore, other examples may be distributed throughout several circuits, logic units, or devices illustrated in Fig. 10.

[0052] The chipset 1020 may communicate with a bus 1040 using a PtP interface circuit 1041. The bus 1040 may have one or more devices that communicate with it, such as a bus bridge 1042 and I/O devices 1043. Via a bus 1044, the bus bridge 1043 may communicate with other devices such as a keyboard/mouse 1045, communication devices 1046 (such as modems, network interface devices, or other communication devices that may communicate with the computer network 1003), audio I/O device, and/or a data storage device 1048. The data storage device 1048 (which may be a hard disk drive or a NAND flash based solid state drive) may store code 1049 that may be executed by the processors 1004.

[0053] The following examples pertain to further examples.

[0054] Example 1 is a virtual sensor hub comprising a plurality of sensor drivers and a sensor fusion driver communicatively coupled to the plurality of sensor drivers, wherein the sensor fusion driver receives inputs from the plurality of sensor drivers and processes the data to generate sensor data.

[0055] In Example 2, the subject matter of Example 1 can optionally include an arrangement in which the plurality of sensor drivers includes an accelerometer driver.

[0056] In Example 3, the subject matter of any one of Examples 1–2 can optionally include an arrangement in which the plurality of sensor drivers includes a magnetometer driver.

[0057] In Example 4, the subject matter of any one of Examples 1–3 can optionally include an arrangement in which the plurality of sensor drivers includes a gyroscope driver.

[0058] In Example 5, the subject matter of any one of Examples 1–4 can optionally include an arrangement in which the plurality of sensor drivers includes a light sensor driver .

[0059] In Example 6, the subject matter of any one of Examples 1–5 can optionally include an arrangement in which the sensor fusion driver is communicatively coupled to a human interface device driver.

[0060] Example 7 is an application processor comprising a memory and a virtual sensor hub coupled to the memory and comprising a plurality of sensor drivers, and a sensor fusion driver communicatively coupled to the plurality of sensor drivers, wherein the sensor fusion driver receives inputs from the plurality of sensor drivers and processes the data to generate sensor data.

[0061] In Example 8, the subject matter of Example 7 can optionally include an arrangement in which the plurality of sensor drivers includes an accelerometer driver.

[0062] In Example 9, the subject matter of any one of Examples 7-8 can include an arrangement in which the accelerometer driver is communicatively coupled to at least one accelerometer.

[0063] In Example 10, the subject matter of any one of Examples 7-9 can include an arrangement in which the plurality of sensor drivers includes a magnetometer driver.

[0064] In Example 11, the subject matter of any one of Examples 7-10 can include an arrangement in which the magnetometer driver is communicatively coupled to at least one magnetometer.

[0065] In Example 12, the subject matter of any one of Examples 7-11 can include an arrangement in which the plurality of sensor drivers includes a gyroscope driver.

[0066] In Example 13, the subject matter of any one of Examples 7-12 can include an arrangement in which the gyroscope driver is communicatively coupled to at least one gyroscope.

[0067] In Example 14, the subject matter of any one of Examples 7-13 can include an arrangement in which the plurality of sensor drivers includes a light sensor driver.

[0068] In Example 15, the subject matter of any one of Examples 7-14 can include an arrangement in which the light sensor driver is communicatively coupled to at least one light sensor.

[0069] In Example 16, the subject matter of any one of Examples 7-15 can include an arrangement in which the sensor fusion driver is communicatively coupled to a human interface device driver.

[0070] In Example 17, the subject matter of any one of Examples 7-16 can include an arrangement in which the human interface driver is communicatively coupled to at least one human interface.

[0071] Example 18 is an electronic device comprising at least one application processor, a memory, and a virtual sensor hub coupled to the memory and comprising a plurality of sensor drivers and a sensor fusion driver communicatively coupled to the plurality of sensor drivers, wherein the sensor fusion driver receives inputs from the plurality of sensor drivers and processes the data to generate sensor data.

[0072] In Example 19 the subject matter of Examples 18 can include an arrangement in which the plurality of sensor drivers includes an accelerometer driver.

[0073] In Example 20, the subject matter of any one of Examples 18-19 can include an arrangement in which the accelerometer driver is communicatively coupled to at least one accelerometer.

[0074] In Example 21, the subject matter of any one of Examples 18-20 can include an arrangement in which the plurality of sensor drivers includes a magnetometer driver.

[0075] In Example 22, the subject matter of any one of Examples 18-21 can include an arrangement in which the magnetometer driver is communicatively coupled to at least one magnetometer.

[0076] In Example 23, the subject matter of any one of Examples 18-22 can include an arrangement in which the plurality of sensor drivers includes a gyroscope driver.

[0077] In Example 24, the subject matter of any one of Examples 18-23 can include an arrangement in which the gyroscope driver is communicatively coupled to at least one gyroscope.

[0078] In Example 25, the subject matter of any one of Examples 18-24 can include an arrangement in which the plurality of sensor drivers includes a light sensor driver.

[0079] The terms “logic instructions” as referred to herein relates to expressions which may be understood by one or more machines for performing one or more logical operations. For example, logic instructions may comprise instructions which are interpretable by a processor compiler for executing one or more operations on one or more data objects. However, this is merely an example of machine-readable instructions and examples are not limited in this respect.

[0080] The terms "computer readable medium" as referred to herein relates to media capable of maintaining expressions which are perceivable by one or more machines. For example, a computer readable medium may comprise one or more storage devices for storing computer readable instructions or data. Such storage devices may comprise storage media such as, for example, optical, magnetic or semiconductor storage media. However, this is merely an example of a computer readable medium and examples are not limited in this respect.

[0081] The term “logic” as referred to herein relates to structure for performing one or more logical operations. For example, logic may comprise circuitry which provides one or more output signals based upon one or more input signals. Such circuitry may comprise a finite state machine which receives a digital

input and provides a digital output, or circuitry which provides one or more analog output signals in response to one or more analog input signals. Such circuitry may be provided in an application specific integrated circuit (ASIC) or field programmable gate array (FPGA). Also, logic may comprise machine-readable instructions stored in a memory in combination with processing circuitry to execute such machine-readable instructions. However, these are merely examples of structures which may provide logic and examples are not limited in this respect.

[0082] Some of the methods described herein may be embodied as logic instructions on a computer-readable medium. When executed on a processor, the logic instructions cause a processor to be programmed as a special-purpose machine that implements the described methods. The processor, when configured by the logic instructions to execute the methods described herein, constitutes structure for performing the described methods. Alternatively, the methods described herein may be reduced to logic on, e.g., a field programmable gate array (FPGA), an application specific integrated circuit (ASIC) or the like.

[0083] In the description and claims, the terms coupled and connected, along with their derivatives, may be used. In particular examples, connected may be used to indicate that two or more elements are in direct physical or electrical contact with each other. Coupled may mean that two or more elements are in direct physical or electrical contact. However, coupled may also mean that two or more elements may

not be in direct contact with each other, but yet may still cooperate or interact with each other.

[0084] Reference in the specification to "one example" or "some examples" means that a particular feature, structure, or characteristic described in connection with the example is included in at least an implementation. The appearances of the phrase "in one example" in various places in the specification may or may not be all referring to the same example.

[0085] Although examples have been described in language specific to structural features and/or methodological acts, it is to be understood that claimed subject matter may not be limited to the specific features or acts described. Rather, the specific features and acts are disclosed as sample forms of implementing the claimed subject matter.

CLAIMS

What is claimed is:

1. A virtual sensor hub, comprising:

a plurality of sensor drivers; and

a sensor fusion driver communicatively coupled to the plurality of sensor drivers, wherein the sensor fusion driver receives inputs from the plurality of sensor drivers and processes the data to generate sensor data.

2. The virtual sensor hub of claim 1, wherein the plurality of sensor drivers includes an accelerometer driver.

3. The virtual sensor hub of claim 1, wherein the plurality of sensor drivers includes a magnetometer driver.

4. The virtual sensor hub of claim 1, wherein the plurality of sensor drivers includes a gyroscope driver.

5. The virtual sensor hub of claim 1, wherein the plurality of sensor drivers includes a light sensor driver.

6. The virtual sensor hub of claim 1, wherein the sensor fusion driver is communicatively coupled to a human interface device driver.

7. An application processor, comprising:

a memory; and

a virtual sensor hub coupled to the memory and comprising:

a plurality of sensor drivers; and

a sensor fusion driver communicatively coupled to the plurality of sensor drivers, wherein the sensor fusion driver receives inputs from the plurality of sensor drivers and processes the data to generate sensor data.

8. The application processor of claim 7, wherein the plurality of sensor drivers includes an accelerometer driver.

9. The application processor of claim 8, wherein the accelerometer driver is communicatively coupled to at least one accelerometer.

10. The application processor of claim 7, wherein the plurality of sensor drivers includes a magnetometer driver.

11. The application processor of claim 10, wherein the magnetometer driver is communicatively coupled to at least one magnetometer.

12. The application processor of claim 7, wherein the plurality of sensor drivers includes a gyroscope driver.

13. The application processor of claim 12, wherein the gyroscope driver is communicatively coupled to at least one gyroscope.

14. The application processor of claim 7, wherein the plurality of sensor drivers includes a light sensor driver.

15. The application processor of claim 14, wherein the light sensor driver is communicatively coupled to at least one light sensor.

16. The application processor of claim 7, wherein the sensor fusion driver is communicatively coupled to a human interface device driver.

17. The application processor of claim 15, wherein the human interface driver is communicatively coupled to at least one human interface.

18. An electronic device, comprising:

at least one application processor;

a memory; and

a virtual sensor hub coupled to the memory and comprising:

a plurality of sensor drivers; and

a sensor fusion driver communicatively coupled to the plurality of sensor drivers, wherein the sensor fusion driver receives inputs from the plurality of sensor drivers and processes the data to generate sensor data.

19. The electronic device of claim 18, wherein the plurality of sensor drivers includes an accelerometer driver.

20. The electronic device of claim 19, wherein the accelerometer driver is communicatively coupled to at least one accelerometer.

21. The electronic device of claim 20, wherein the plurality of sensor drivers includes a magnetometer driver.

22. The electronic device of claim 21, wherein the magnetometer driver is communicatively coupled to at least one magnetometer.

23. The electronic device of claim 18, wherein the plurality of sensor drivers includes a gyroscope driver.

24. electronic device of claim 23, wherein the gyroscope driver is communicatively coupled to at least one gyroscope.

25. The electronic device of claim 24, wherein the plurality of sensor drivers includes a light sensor driver.

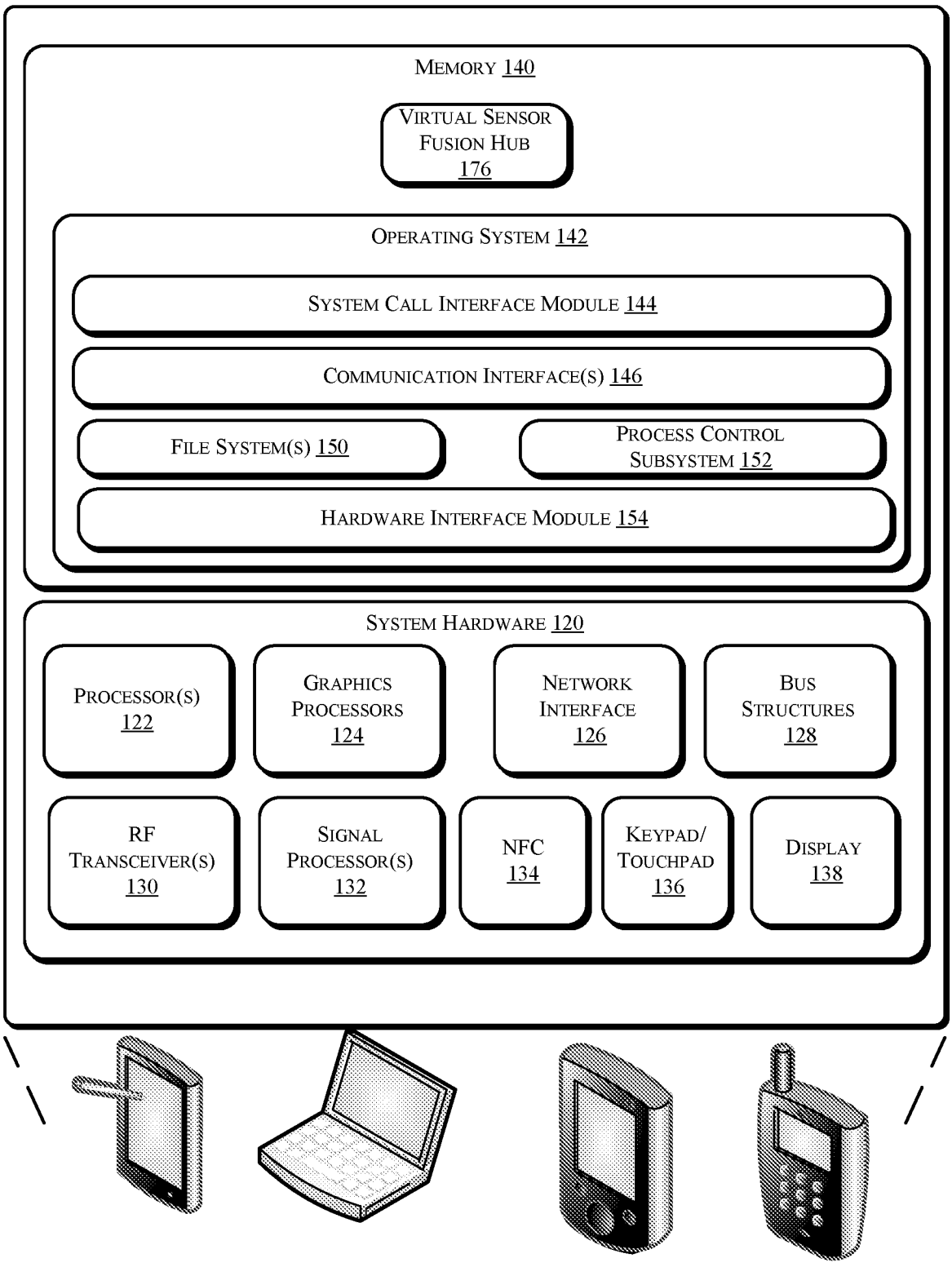

FIG. 1 Electronic Device 100

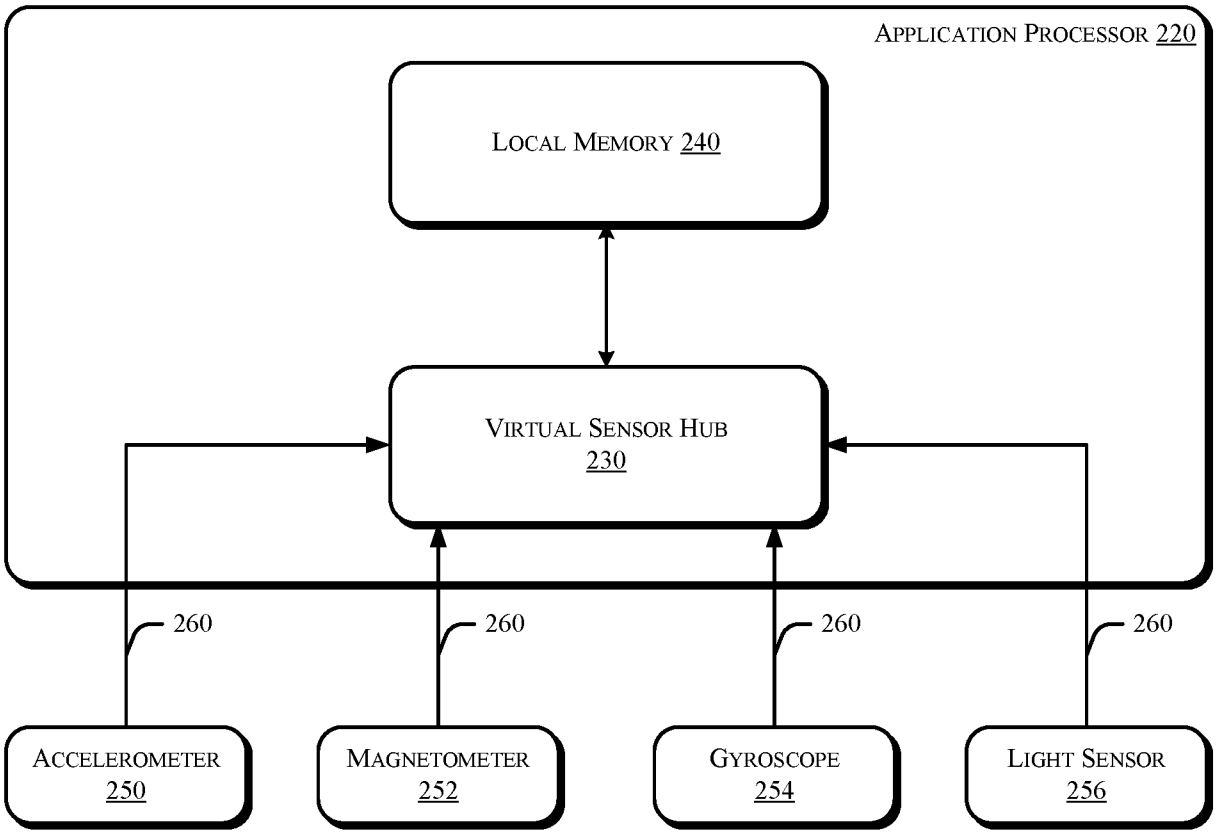
APPLICATION PROCESSOR 220
LOCAL MEMORY 240
VIRTUAL SENSOR HUB 230
260
260
260
260
ACCELEROMETER 250
MAGNETOMETER 252
GYROSCOPE 254
LIGHT SENSOR 256

FIG. 2

300

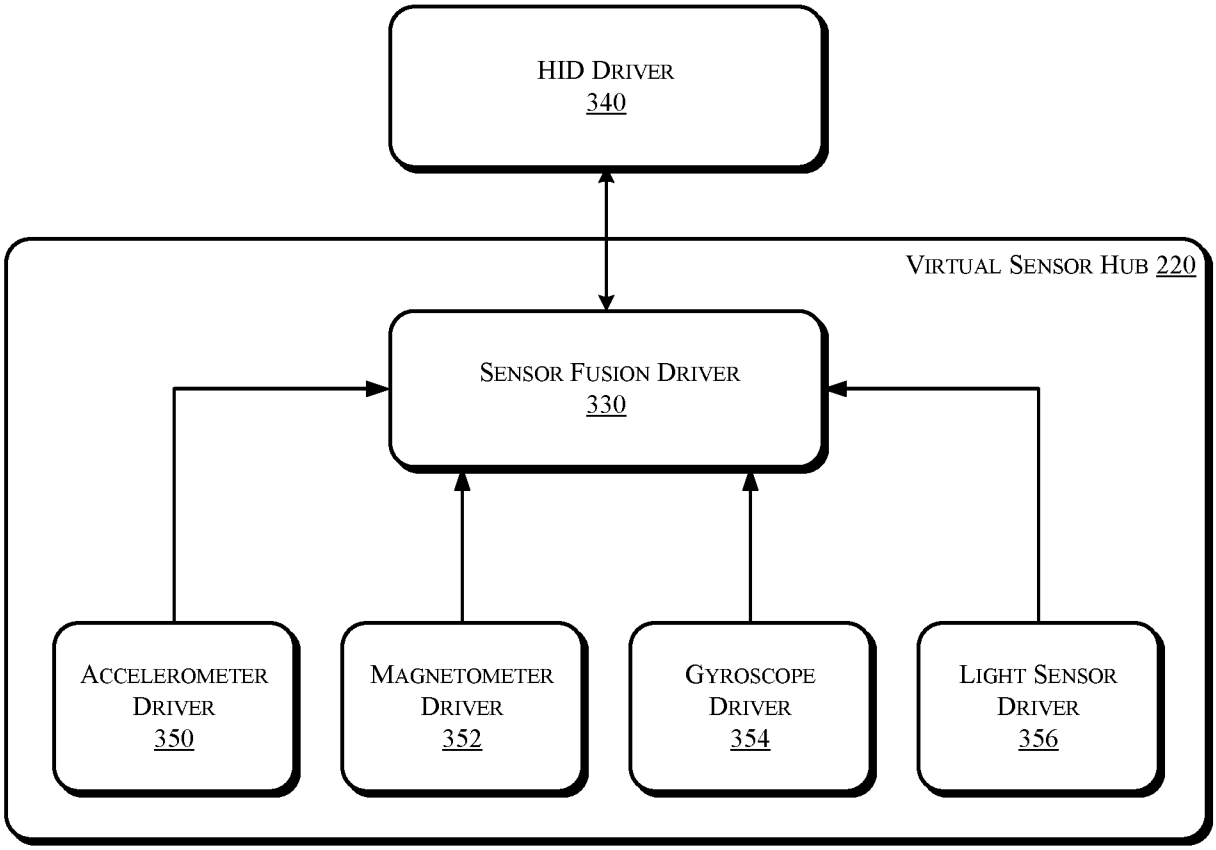
HID DRIVER
340
VIRTUAL SENSOR HUB 220
SENSOR FUSION DRIVER
330
ACCELEROMETER DRIVER
350
MAGNETOMETER DRIVER
352
GYROSCOPE DRIVER
354
LIGHT SENSOR DRIVER
356

FIG. 3

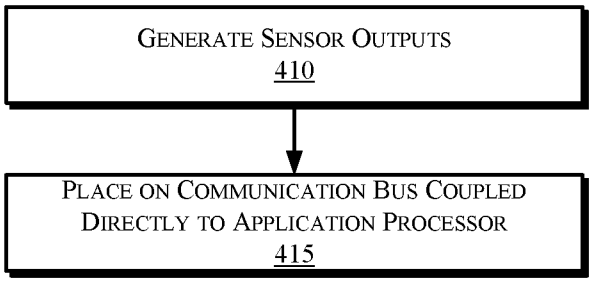
GENERATE SENSOR OUTPUTS
410
PLACE ON COMMUNICATION BUS COUPLED DIRECTLY TO APPLICATION PROCESSOR
415

FIG. 4

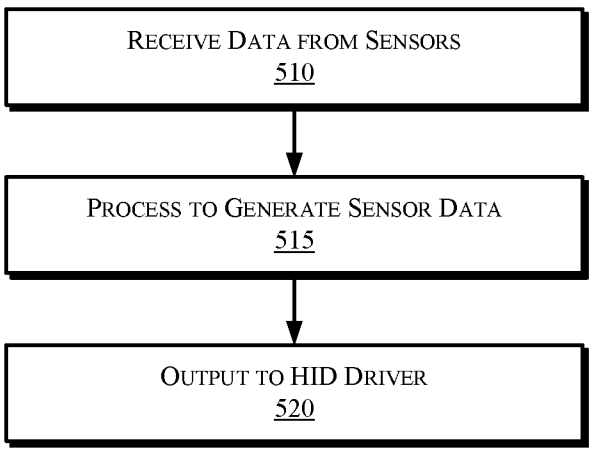
RECEIVE DATA FROM SENSORS
510
PROCESS TO GENERATE SENSOR DATA
515
OUTPUT TO HID DRIVER
520

FIG. 5

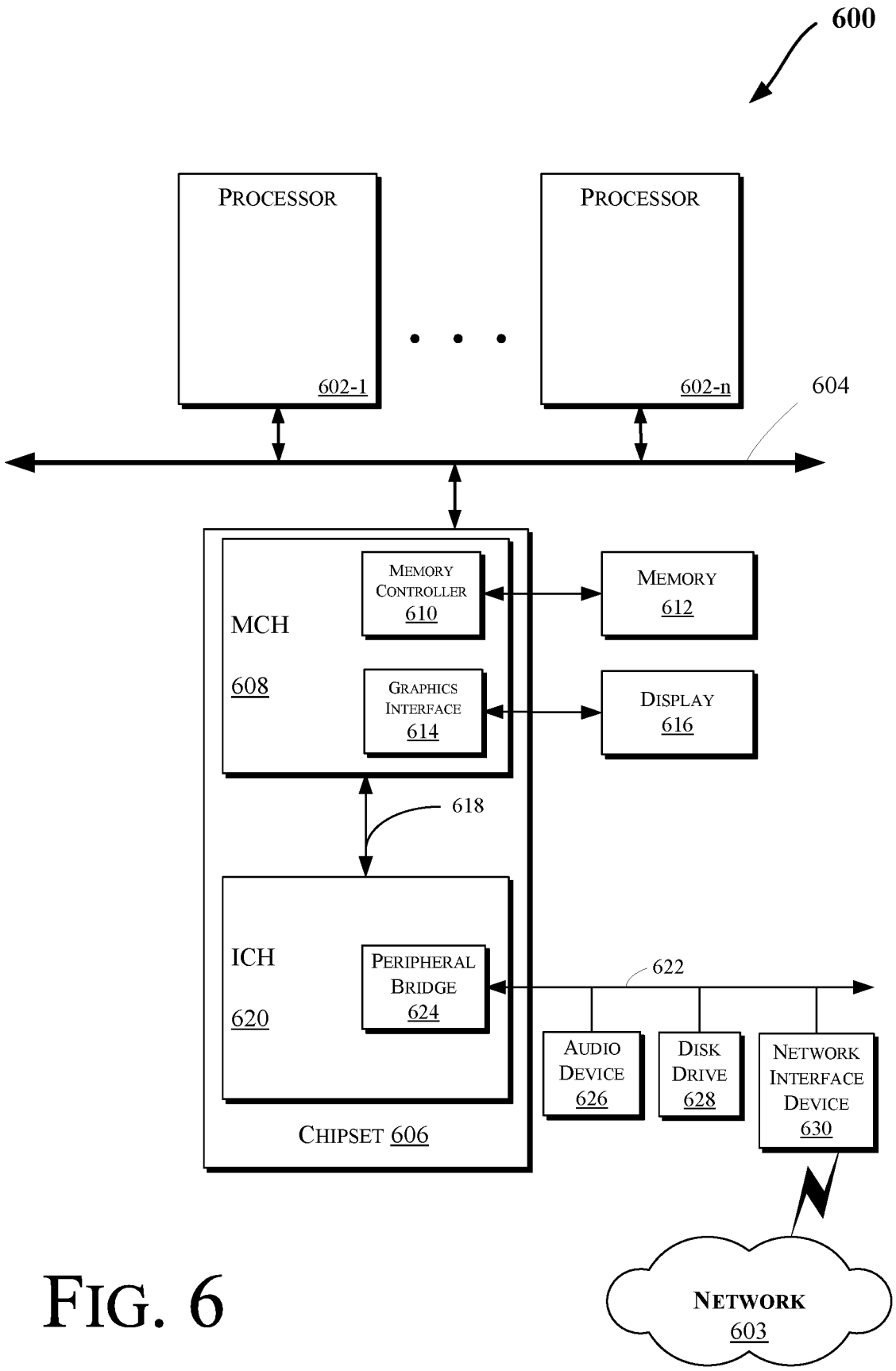
600
PROCESSOR
602-1
PROCESSOR
602-n
604
MCH
608
MEMORY CONTROLLER
610
GRAPHICS INTERFACE
614
MEMORY
612
DISPLAY
616
618
ICH
620
PERIPHERAL BRIDGE
624
622
AUDIO DEVICE
626
DISK DRIVE
628
NETWORK INTERFACE DEVICE
630
CHIPSET 606
NETWORK
603

FIG. 6

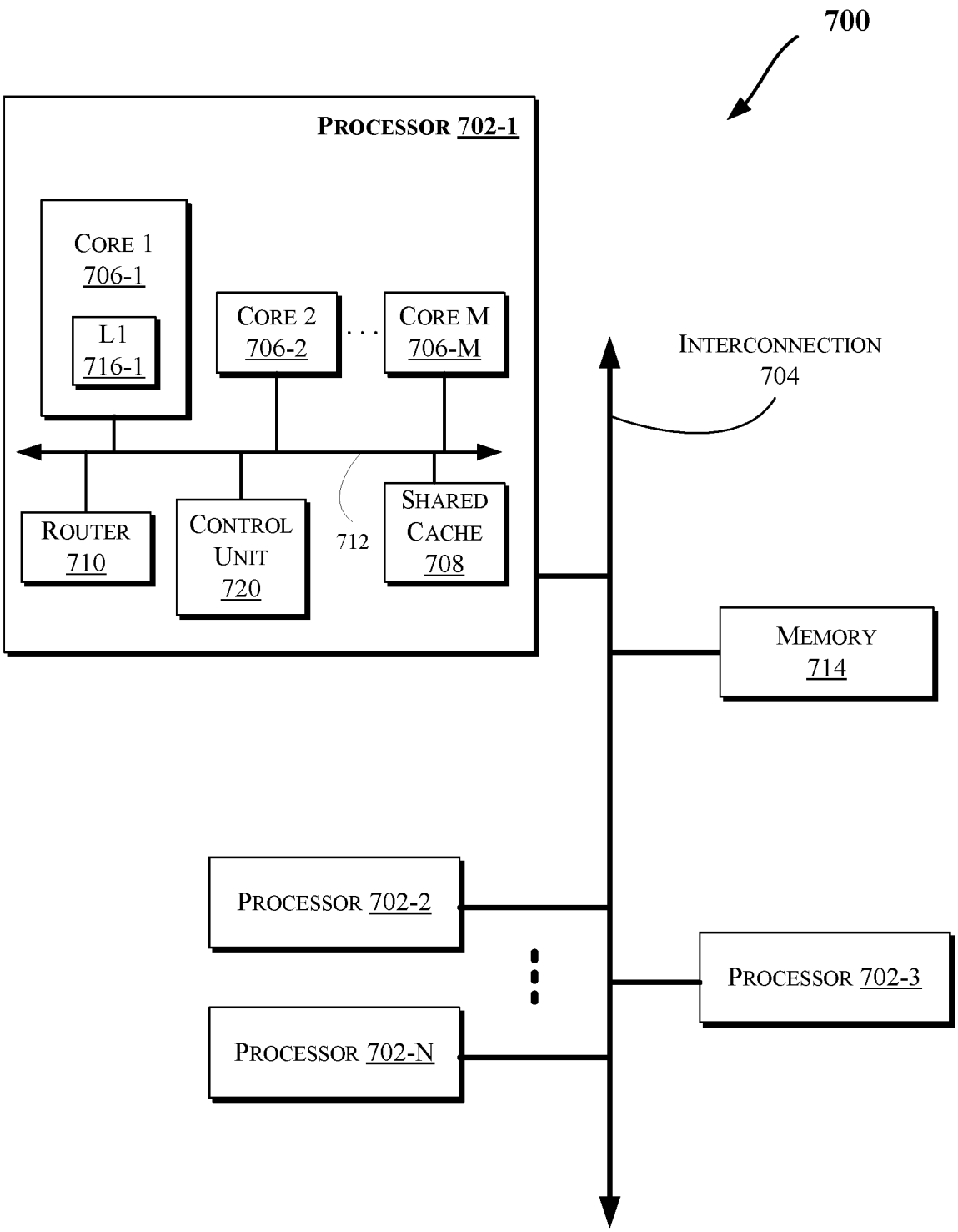
700
PROCESSOR 702-1
CORE 1
706-1
L1
716-1
CORE 2
706-2
CORE M
706-M
INTERCONNECTION
704
ROUTER
710
CONTROL
UNIT
720
712
SHARED
CACHE
708
MEMORY
714
PROCESSOR 702-2
PROCESSOR 702-3
PROCESSOR 702-N

FIG. 7

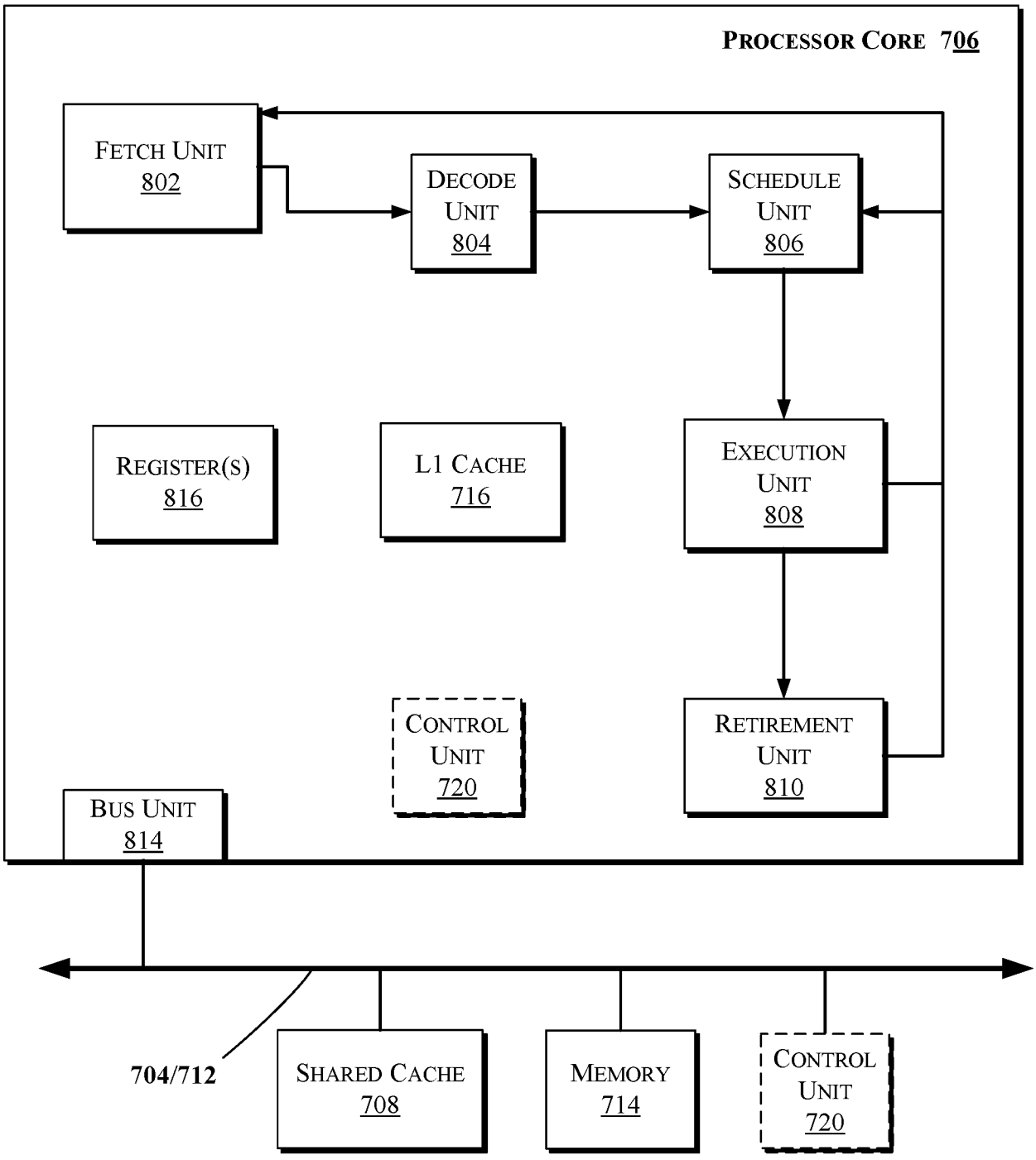
PROCESSOR CORE 706
FETCH UNIT 802
DECODE UNIT 804
SCHEDULE UNIT 806
REGISTER(S) 816
L1 CACHE 716
EXECUTION UNIT 808
CONTROL UNIT 720
RETIREMENT UNIT 810
BUS UNIT 814
704/712
SHARED CACHE 708
MEMORY 714
CONTROL UNIT 720

FIG. 8

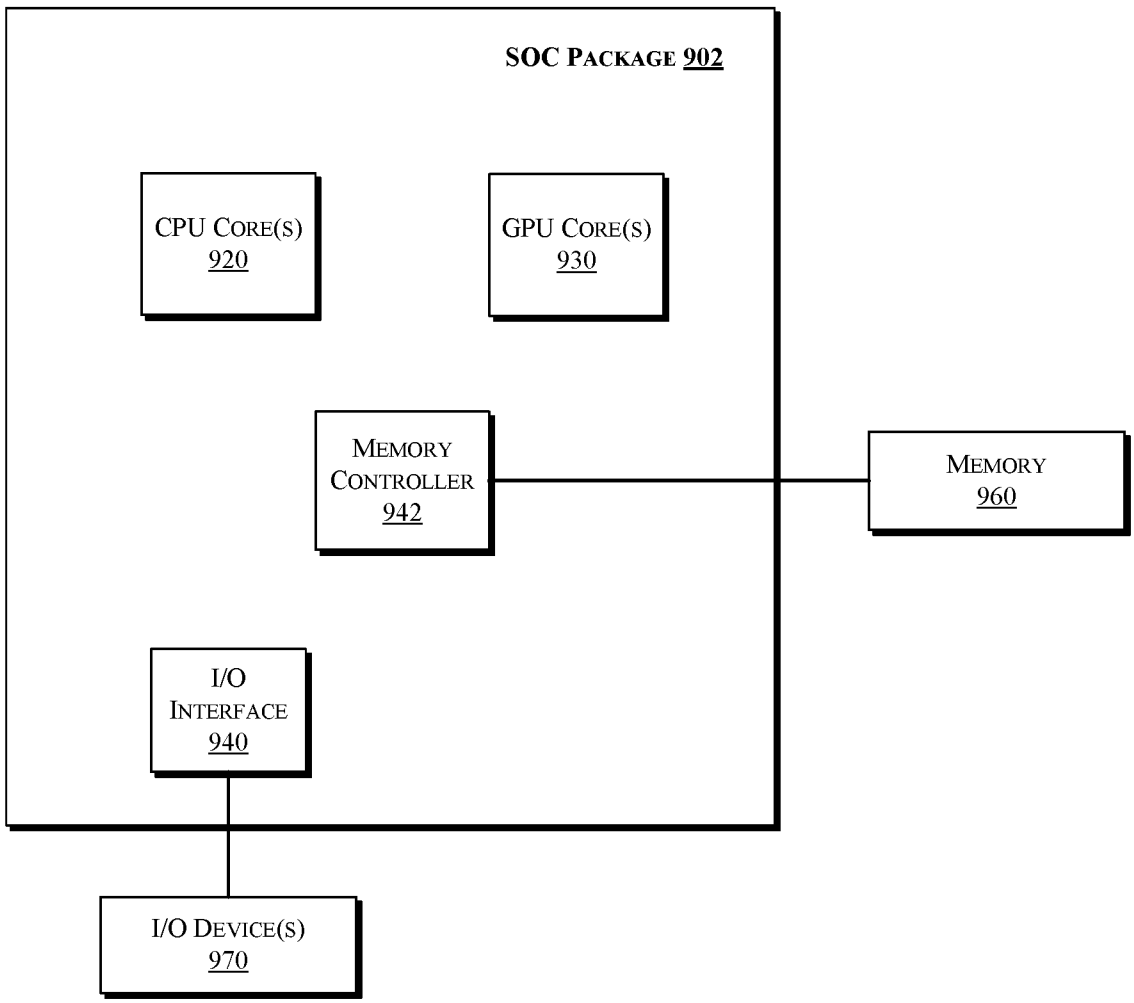
SOC PACKAGE 902
CPU CORE(S) 920
GPU CORE(S) 930
MEMORY CONTROLLER 942
MEMORY 960
I/O INTERFACE 940
I/O DEVICE(S) 970

FIG. 9

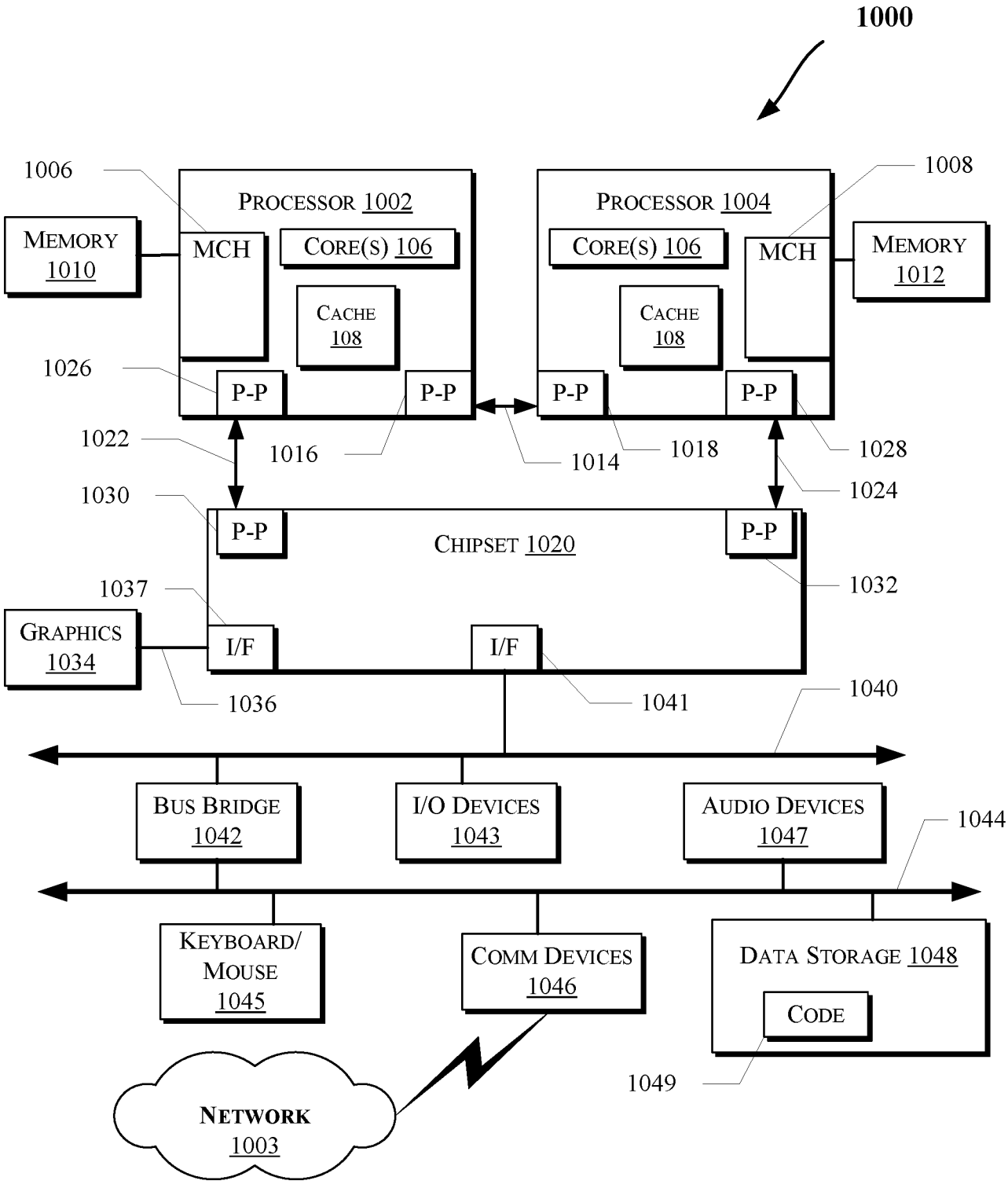
1000
1006
PROCESSOR 1002
MEMORY 1010
MCH
CORE(S) 106
CACHE 108
1008
PROCESSOR 1004
CORE(S) 106
MCH
MEMORY 1012
CACHE 108
1026
P-P
P-P
P-P
P-P
1022
1016
1014
1018
1028
1030
1024
P-P
CHIPSET 1020
P-P
1037
1032
GRAPHICS 1034
I/F
I/F
1036
1041
1040
BUS BRIDGE 1042
I/O DEVICES 1043
AUDIO DEVICES 1047
1044
KEYBOARD/ MOUSE 1045
COMM DEVICES 1046
DATA STORAGE 1048
CODE
1049
NETWORK 1003

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2014/081068

A. CLASSIFICATION OF SUBJECT MATTER

G06F9/48(2006.01)i; G06F 9/48(2006.01)i; G06F 9/305(2006.01)i; H04W 52/02(2009.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F, H04W

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,WPI,EPODOC: sensor、hub、driv???、data、fusion、low、power、consumption、application、processor?、instruction、logic、software、firmware、virtual

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN 102893257 A (INTEL CORP.) 23 January 2013 (2013-01-23) description paragraphs [0015]-[0023], [0027]-[0038]、figures 1-5	1-25
Y	ZHENG, Di et al. "A Component Deployment Framework Supporting Context-Awareness in Pervasive Computing Environment" *Computer Science*, Vol. Vol.33, No. No.11, 30 November 2006 (2006-11-30), pages 41-42, figures 2-3	1-25
Y	CN 102893589 A (NOKIA CORP.) 23 January 2013 (2013-01-23) description paragraphs [0023], [0028]-[0038], [0040]-[0048], [0072]-[0073]	1-25
Y	SONG, Dian. "Research on Context-aware Technology of Disabled Health Service for Intelligent Community" *Chinese Master's Theses Full-text Database Information Science and Technology*, No. N0.S2, 31 December 2013 (2013-12-31), pages 5-24	1-25
A	CN 1916828 A (SAP AG.) 21 February 2007 (2007-02-21) the whole document	1-25

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 March 2015	**27 March 2015**
Name and mailing address of the ISA/CN **STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA(ISA/CN)** **6,Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China** Facsimile No. **(86-10)62019451**	Authorized officer **XIANG,Wei** Telephone No. **(86-10)01062413541**

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 103548374 A (CITRIX SYSTEMS INC.) 29 January 2014 (2014-01-29) the whole document	1-25
A	WO 2012151115 A2 (FACEBOOK, INC.) 08 November 2012 (2012-11-08) the whole document	1-25

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2014/081068

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	102893257		23 January 2013	US	2012254878	A1	04 October 2012
				TW	201243728	A	01 November 2012
				KR	20130131458	A	03 December 2013
				EP	2695056	A1	12 February 2014
				JP	2014509765	A	21 April 2014
				WO	2012134546	A1	04 October 2012
CN	102893589	A	23 January 2013	US	2013057394	A1	07 March 2013
				WO	2011141761	A1	17 November 2011
				TW	201218736	A	01 May 2012
				KR	20130033378	A	03 April 2013
				EP	2569924	A1	20 March 2013
				KR	101437757	B1	05 September 2014
				CN	102893589	B	11 February 2015
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				US	7881862	B2	01 February 2011
				US	8352172	B2	08 January 2013
				US	2011066947	A1	17 March 2011
				US	2006217881	A1	28 September 2006
				CN	100432913	C	12 November 2008
CN	103548374	A	29 January 2014	US	2012284322	A1	08 November 2012
				EP	2697996	A1	19 February 2014
				WO	2012142088	A1	18 October 2012
WO	2012151115	A2	08 November 2012	US	2012280917	A1	08 November 2012