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PATENT SPECIFICATION (11) 1 593 863

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(19)

(54) IMPROVEMENTS IN OR RELATING TO CIRCUIT ARRANGEMENTS

(71) We, THE PLESSEY COMPANY LIMITED, a British Company of Vicarage Lane, Ilford, Essex, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to circuit arrangements and relates more especially to voltage multiplier circuit arrangements.

In our Patent Specification No. 1,561,980 there is described a voltage multiplier circuit that is especially suitable for solid state construction and which offers advantages over other similar forms of voltage multiplier. In particular in that application there is described a solid state voltage multiplier that lends itself for implementation using MOS or MNOS technologies and in which diode connected transistors are used in place of simple diodes. In equation (5) on page 8 of that application it is indicated that voltage multiplication occurs provided that:—

$$\left(\frac{C}{C+C_S}\right)V_\phi - V_D - \frac{I_{OUT}}{(C+C_S)f} > 0 \qquad (1)$$

where V_ϕ is the clock voltage and V_D is the forward diode voltage.

In the case where diode connected transistors are used, V_D becomes V_T, the transistor threshold voltage, so that equation (1) may be re-written:—

$$\frac{C}{C+C_S}V_\phi - V_T - \frac{I_{OUT}}{(C+C_S)f} > 0 \qquad (2)$$

Re-arranging equation (2) it is found that voltage multiplication occurs providing:—

$$V_\phi > \frac{C+C_S}{C}\left[V_T + \frac{I_{OUT}}{(C+C_S)f}\right] \qquad (3)$$

In fact a more exact solution would take into account the increase in V_T with source-substrate bias.

Nevertheless, from equation (3) it can be seen that for multiplication to occur $V_\phi > V_T$. Typically the effective V_T will be in the order of 5 volts and it is found that a clock voltage V_ϕ of approximatyly 7—8 volts is required. However, there are many applications where a maximum operating voltage of say 5 volts is required. In these applications the voltage multiplier that forms the basis of the aforesaid Patent Specification 1,561,980 will not function.

It is an object of the present invention to provide a voltage multiplier circuit arrangement that is based on that described in the aforementioned patent application, that incorporates transistors but which will operate on lower voltages.

According to the present invention there is provided a voltage multiplier circuit arrangement comprising a plurality of transistors connected in series between an input and an output of said arrangement, and first and second input lines arranged to have an alternating voltage applied between them, successive interconnections between adjacent transistors being connected via capacitors to alternate ones of the first and second input lines, the control electrode e.g. the gate or base electrode of each one of said transistors being connected to an interconnection of two adjacent transistors that are nearer the output of said arrangement than said one transistor and that is connected via one of said capacitors with the input line with which said one transistor is connected.

In carrying out the invention the transitors may take the form of field effect transistors e.g. of MOS or MNOS form or may take the form of bipolar transistors.

In a preferred arrangement for carrying out the invention, the plurality of transistors will be terminated in diode means, preferably provided in the form of a diode connected transistor, the output of said diode means being connected via a capacitor to an appropriate one of the input

lines and also connected to the control electrode of the last of the plurality of transistors.

Advantageously, further diode means will be provided connected to the last of the plurality of transistors for affording the output of said arrangement.

In one arrangement for carrying out the invention, the input of said arrangement may be connected to one or other of the first and second input lines, and advantageously the first and second input lines may have applied to them a respective one of two anti-phase clock signals.

Some exemplary embodiments of the invention will now be described, reference being made to the accompanying drawings, in which;

Figure 1, is a circuit diagram of the voltage multiplier circuit arrangement that form the basis of the aforementioned Patent Specification No. 1,561,980, in which diode connected transistors are used;

Figure 2, is a circuit diagram of a voltage multiplier circuit arrangement in accordance with the present invention which makes use of field effect transistors;

Figure 3, is a circuit diagram of a termination circuit for the voltage multiplier circuit arrangement of Figure 2, and;

Figure 4, is a circuit diagram of a voltage multiplier circuit arrangement in accordance with the present invention which is similar to that shown in Figures 2 and 3 but which makes use of bipolar transistors.

In Figure 1 of the drawings, there is depicted a voltage multiplier circuit of the form described in the aforementioned Patent Specification 1,561,980 which makes use of diodes in the form of diode connected field effect transistors. The arrangement consists of four transistors 1, 2, 3 and 4, the gate and source electrodes of which are connected together so that they operate as diodes, the diode connected transistors 1, 2, 3 and 4 being connected in series between an input 5 and an output 6. Alternate interconnections between adjacent ones of the transistors 1, 2, 3 and 4 are connected via capacitors 7 to one or other of two anti-phase clock lines referenced $\phi 1$ and $\phi 2$. The operation of the multiplier circuit is fully described in the aforementioned application. As described therein the input 5 may be a separate input as shown in Figure 1 or may be connected to one of the clock lines $\phi 1$ or $\phi 2$. Since the transistors 1, 2, 3 and 4 are each connected in the form of a diode, the voltage drop across each of them will equal the theshold voltage V_T and as has already been shown for multiplication to occur $V_T > V_\phi$ where V_ϕ is the clock voltage applied to the clock lines $\phi 1$ and $\phi 2$. Typically V_T may be in the order of 5 volts, thus requiring a clock voltage V_ϕ of say 7 to 8 volts.

In order to be able to reduce the clock voltage required so that the multiplier will operate on say 5 volts, it is necessary to reduce the effective voltage drop across the transistors 1, 2, 3 and 4 and this may be done by operating them as transistors rather than as diodes and making use of the fact that there is a progressive increase in voltage between the input 5 and the output 6. Thus, it should be possible to connect the gate electrode of each of the transistors 1, 2, 3 and 4 to a point of higher voltage so that they are turned harder 'ON' thus reducing the voltage drop across them. An arrangement of this form is depicted in Figure 2 of the accompanying drawing in which parts corresponding to those in Figure 1 have been accorded the same reference numerals. In this circuit, instead of connecting the transistors 1, 2, 3 and 4 as diodes, they are connected as transistors, the gate electrode of each of which is connected to the 'interconnection' between two adjacent ones of the transistors that is nearer the output 5 and is thus at a higher potential than its source electrode, thus causing it to be turned harder 'ON'. However, the interconnections between adjacent ones of the transistors 1, 2, 3 and 4 are associated with alternate ones of the clock lines $\phi 1$ and $\phi 2$ so that a phase difference occurs between adjacent interconnections. Because of this it is necessary to connect the gate electrode of one transistor to the interconnection between two transistors that is associated with the same clock voltage. Thus it is found that the gate electrode of one transistor is connected to the next but one interconnection between two transistors as shown in the circuit of Figure 2, although in theory it would be possible to connect it to the next-but-three or next-but-five interconnection etc. Thus in the circuit of Figure 2, the gate electrode of transistor 1 is connected to the interconnection of transistor 2 and 3; the gate electrode of transistor 2 is connected to the interconnection between transistors 3 and 4 etc.

With such an arrangement as described with reference to Figure 2, it is found that the circuit is self-limiting in that regardless of increasing clock voltage, the effective voltage drop across each of the transistors 1, 2, 3 and 4 will be equal to half the threshold voltage, i.e.

$$\frac{V_T}{2}.$$

If a next-but-three interconnection

arrangement is used then the effective voltage drop across each transistor will be equal to

$$\frac{V_T}{4},$$

and so on for the other possible connections.

Thus, for the multiplier circuit of Figure 2, it can be shown that voltage multiplication will occur if

$$V_\phi > \frac{V_T}{2}$$

and typically a clock voltage of approximately 4 to 5 volts is found satisfactory.

One problem with the multiplier circuit of Figure 2 is that it needs to be terminated so that gate electrode of the final one 4 of the transistors 1, 2, 3 and 4 can be correctly connected. This may be done as shown in Figure 3 by making use of a further transistor 8 connected in series with the transistors 1, 2, 3 and 4 and connected to the appropriate clock line via a capacitor 7, but by connecting the gate and source electrodes of the transistor 8 together so that it operates as a diode.

The gate electrode of the final one 4 of the transistors 1, 2, 3 and 4 is then connected to the drain electrode of the transistor 8 which is also connected to the $\phi 1$ clock line via a capacitor 7. An output from the circuit of Figure 3 may be derived from the drain electrode of the transistor 8 but more preferably is derived from the interconnection of the transistors 4 and 8 via a further transistor 9 the source and gate electrodes of which are connected together so that it operates as a diode to afford the output 6.

The voltage multiplier circuit arrangement so far considered with reference to Figures 2 and 3 of the accompanying drawings has been described as incorporating field effect transistors and may be advantageously constructed in solid state form using, for example, metal oxide silicon (MOS) or metal nitride oxide silicon (MNOS) technology. However the arrangement of Figures 2 and 3 may equally well be implemented using bipolar technology and a circuit arrangement of this form is shown in Figure 4 of the accompanying drawing. The parts of the arrangement of Figure 4 that correspond to those in Figures 2 and 3 have been accorded the same reference numerals and since it operates in exactly the same way as described for Figures 2 and 3 no further explanation is deemed necessary apart from saying that the voltage drop across each of the series connected transistors, apart from transistors 8 and 9 is

$$\frac{V_{BE}}{2}$$

where V_{BE} is the usual base-emitter voltage. In this case voltage multiplication will occur if

$$V_\phi > \frac{V_{BE}}{2}$$

One particularly envisaged application of the voltage multiplier circuit arrangement described with reference to Figure 2 with the terminating circuit of Figure 3 is in repertory diallers which are preferably constructed in MNOS form and are required to operate from a normal line voltage of approximately 5v.

WHAT WE CLAIM IS:—

1. A voltage multiplier circuit arrangement comprising a plurality of transistors connected in series between an input and an output of said arrangement and first and second input lines arranged to have an alternating voltage applied between them, successive interconnections between adjacent transistors being connected via capacitors to alternate ones of the first and second input lines, the control electrode e.g. the gate or base electrode of each one of said transistors being connected to an interconnection of two adjacent transistors that are nearer the output of said arrangement than said one transistor and that is connected via one of said capacitors with the input line with which said one transistor is connected.

2. A circuit arrangement as claimed in claim 1 in which the transistors take the form of field effect transistors.

3. A circuit arrangement as claimed in claim 1 in which the transistors take the form of bi-polar transistors.

4. A circuit arrangement as claimed in any preceeding claim in which the plurality of transistors is terminated in diode means.

5. A circuit arrangement as claimed in claim 4 in which the diode means is provided in the form of a diode connected transistor, the output of said diode means being connected via a capacitor to an appropriate one of the input lines and also connected to the control electrode of the last of the plurality of transistors.

6. A circuit arrangement as claimed in claim 4 or 5 in which further diode means is provided connected to the last of the

plurality of transistors for affording the output of said arrangement.

7. A circuit arrangement as claimed in any preceeding claim in which the input of said arrangement is connected to one or other of the first and second input lines.

8. A circuit arrangement as claimed in any preceeding claim in which the first and second input lines have applied to them a respective one of two antiphase clock signals.

9. A circuit arrangement as herein described with reference to and as illustrated in any one of Figures 2 to 4 of the accompanying drawings.

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1593863 COMPLETE SPECIFICATION
1 SHEET *This drawing is a reproduction of the Original on a reduced scale*

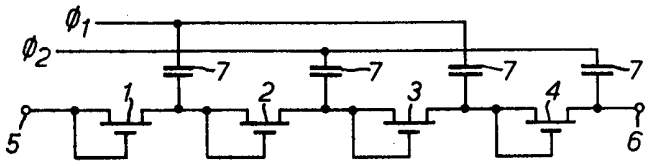

FIG. 1.

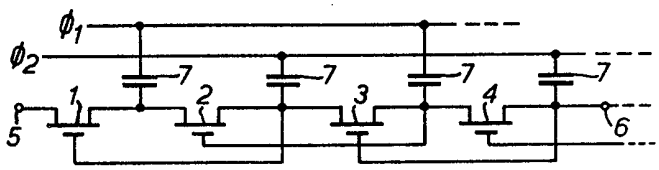

FIG. 2.

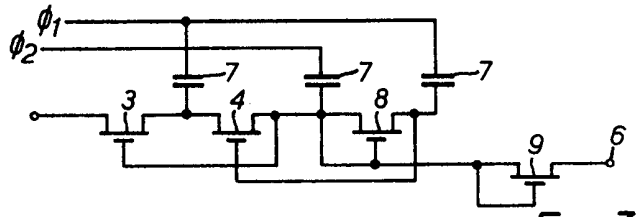

FIG. 3.

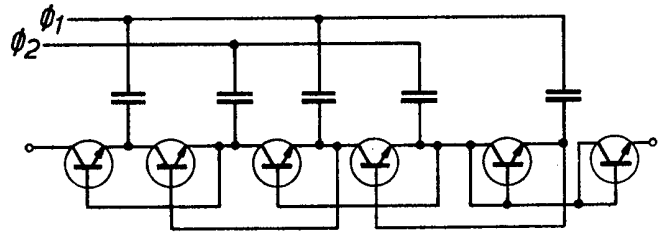

FIG. 4.