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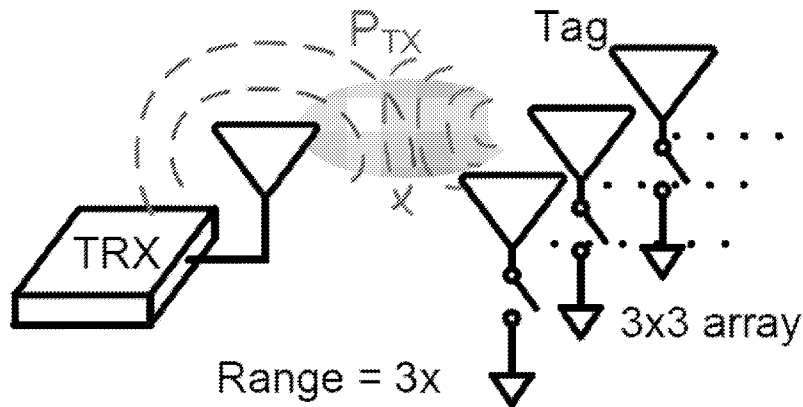(54) Title: SYSTEMS, METHODS, AND MEDIA FOR MULTI-ANTENNA, DIRECTIONAL BACKSCATTER TAGS

FIG. 1

(57) Abstract: Backscatter tags, comprising: antennas; single pole, multiple throw switches each switch (S) having pole terminal connected to one of the antennas, and each having first throw terminal (TT) connected to first side (FS) of inductor (I) for S, second TT connected to FS of capacitor (C) for S, third TT connected to fixed voltage level (FVL), fourth TT that is floating, wherein second side (SS) of I and SS of C are connected to the FVL; power combiner (PC) having inputs connected to fifth TT of each of two of the switches; power detector (PD) having an input connected to output of PC; analog to digital converter (ADC) having input connected to output of PD; hardware processor coupled to output of the ADC and coupled to control terminal of each of the switches.

[Continued on next page]

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SYSTEMS, METHODS, AND MEDIA FOR
MULTI-ANTENNA, DIRECTIONAL BACKSCATTER TAGS

Cross Reference to Related Application

[0001]   This application claims the benefit of United States Provisional Patent Application

No. 62/733,479, filed September 19, 2018, which is hereby incorporated by reference herein in

its entirety.

Statement Regarding Government Funded Research

Background

[0003]   Backscatter tags (e.g., RFID tags) are widely used for a variety of applications, such

as security applications, tracking merchandise and people, and storing information. The range of

the tags is limited because the tags frequently do not have their own power source (and only get

power from a received RF signal) or only have a limited power source.

[0004]   It is desirable to increase the range of backscatter tags.

Summary

[0005]   Systems, methods, and media for multi-antenna, directional backscatter tags are

provided. In some embodiments, systems for multi-antenna, directional backscatter tags are

provided, the systems comprising: a plurality of antennas; a plurality of single pole, multiple

throw switches each having a pole terminal connected to a corresponding one of the plurality of

antennas, and each having a first throw terminal connected to a first side of an inductor for that switch, a second throw terminal connected to a first side of a capacitor for that switch, a third throw terminal connected to a fixed voltage level, a fourth throw terminal that is floating, and a fifth throw terminal, wherein a second side of the inductor and a second side of the capacitor are connected to the fixed voltage level; a power combiner having inputs connected to the fifth throw terminal of each of two of the plurality of single pole, multiple throw switches and having an output; a power detector having an input connected to the output of the power combiner and having an output; an analog to digital converter having an input connected to the output of the power detector and having an output; a hardware processor coupled to the output of the analog to digital converter and coupled to a control terminal of each of the plurality of single pole, multiple throw switches.

Brief Description of the Drawings

[0006]   FIG. 1 is an example of a block diagram of a tagger reader and a multi-antenna tag in accordance with some embodiments.

[0007]   FIG. 2 is an example of four illustrations of different configurations of three antenna used to control a phase gradient in accordance with some embodiments.

[0008]   FIG. 3 is an example of a graph showing conjugating angle vs. spacing between antennas for four different phase gradients in accordance with some embodiments.

[0009]   FIG. 4 is an example of a graph showing link enhancement vs. angle of incidence in accordance with some embodiments.

[0010]   FIG. 5 is an example of four plots showing directionality improvements that can be realized using multiple antennas in a backscatter tag in accordance with some embodiments.

[0011]   FIGS. 6A, 6B, and 6C show examples of configurations for measuring received power in accordance with some embodiments.

[0012]   FIG. 7 is an example of graph showing normalized received signal strength indicator (RSSI) vs. angle of incidence in accordance with some embodiments.

[0013]   FIG. 8 is an example of a block diagram of a tag in accordance with some embodiments.

[0014]   FIG. 9 is an example of a block diagram of another tag in accordance with some embodiments.

[0015]   FIG. 10 is an example of process for controlling a tag in accordance with some embodiments.

Detailed Description

[0016]   In accordance with some embodiments, multi-antenna backscatter tags that backscatter directional beams to tag readers are provided. In some embodiments, using a 3x3 antenna array in a backscatter tag (as shown in FIG. 1) can provide up to a 19dB sensitivity enhancement and up to a 3x increase in range between the tag and its reader compared to the same characteristics for single antenna tags.

[0017]   In some embodiments, a compact phase conjugation technique for backscatter modulation can be used with a backscatter tag having a two-dimensional antenna array in order to achieve improved directivity of the backscatter signal in the direction of arrival of the signal being backscattered.

[0018]   In some embodiments, for each antenna of multi-antenna backscatter tag, an incoming RF signal can be reflected back by the backscatter antenna with different phase lags depending on its load. For example, in some embodiments, the load can be formed using open,

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short, inductive, and/or capacitive loads. In some embodiments, each antenna of a multi-antenna backscatter tag can switch between different arrangements of these loads to create a directional backscattered signal. These loads can also be used to implement quadrature phase shift keying (QPSK) modulation of the RF signal in some embodiments. QPSK modulation can be useful to convey a serial number of the tag, data stored in the tag, etc.

[0019]   To understand the principle of operation, assume that a linear array of three antennas with an antenna spacing of d is being used. For an incident signal at an angle θ_i, when operating in the far field, incident waves with wavelength λ received by two adjacent antennas have a phase difference of $\Delta\phi = 2\pi \cdot d \cdot sin(\theta_i)/\lambda$. To reflect the signal back in the direction of arrival, the reflected signal must have a phase difference of $-\Delta\phi$. Thus, the loads of adjacent antennas need to provide an extra phase difference of $\phi_A = -2\Delta\phi$. If the phase lag of the middle antenna is $\phi_r = 0$ degrees, the other two antennas require a phase lag of ϕ_A and $-\phi_A$.

[0020]   Using different arrangements of open, short, inductive, and capacitive loads, the phase gradient ϕ_A can be 0 degrees, 90 degrees, 180 degrees, and 270 degrees as shown in FIG. 2. For these values of ϕ_A, the corresponding angle of incidence (conjugating angle) at which the backscatter tag achieves maximum directivity of the reflected signal in the direction of arrival is plotted in FIG. 3 for increasing spacing between the antennas. By using an antenna spacing of 0.53λ, evenly spaced conjugating angles of 15 degrees, 30 degrees, 45 degrees, and 60 degrees can be obtained in some embodiments.

[0021]   For an N x N array, assuming the required horizontal and vertical phase gradients are ϕ_A and ϕ_B, the required phases for the $(i, j)^{th}$ antenna in the array are:

$$\phi_{ref}(i, j) = (i-(n+1)/2)\phi_A + (j-(n+1)=2)\phi_B,$$

where i and j are indices to the antennas in the antenna array of the tag and n is equal to N (i.e., the number of antennas in each dimension of the two-dimensional array. The tag needs to

determine the gradients ϕ_A and ϕ_B using a direction of arrival estimation). An N x N array can provide N^2 times the link enhancement (e.g., up to 19dB for a 3x3 array as shown in FIG. 4), thus N times the range. As shown in FIG. 5, for $\phi_B = 0$, the backscatter tag directivity is plotted at $\theta_i = 0$ degrees (portion (a) of FIG. 5), 30 degrees (portion (b) of FIG. 5), 45 degrees (portion (c) of FIG. 5), 60 degrees (portion (d) of FIG. 5) using the corresponding ϕ_A for a 3x3 array. The directivity improves by 9dB for the conjugating angles. For $\phi_B = 0$, the maximum achievable array factor is plotted with respect to the angle of incidence θ_i in FIG. 4. Limiting the loads to an open load, a shorted load, an inductive load, and a capacitive load leads to a quantization error in ϕ_A and a degradation of up to 2dB in the array gain.

[0022]   By changing the reference phase ϕ_r, while maintaining the phase gradients ϕ_A and ϕ_B, QPSK modulation can be implemented with directional backscattering. For a baseband signal mapped to a QPSK phase $\phi_m(t)$, the required phase for the $(i, j)^{\text{th}}$ antenna is:

$$\phi(i, j, t) = \phi_{\text{ref}}(i, j) + \phi_m(t).$$

[0023]   For an incoming wave at an angle of incidence θ_i, any two adjacent antennas in a 3x1 linear array receive signals $V_1(t) = A \cdot sin(\omega \cdot t)$ and $V_2(t) = A \cdot sin(\omega \cdot t + \phi)$, where $\phi = 2\pi \cdot d \cdot sin(\theta_i)/\lambda$, A is the maximum amplitude of the signals, ω is the angular frequency of the signal, and t is time. $V_1(t) + V_2(t) = 2 \cdot A \cdot sin(\omega \cdot t)cos(\phi/2)$. Adding the signals in-phase (FIGs. 6A-6C) and detecting the power received gives $P = 2 \cdot A^2 \cdot cos^2(\phi/2)$, θ_i can then be calculated by $\theta_i = sin^{-1}(\lambda \cdot cos^{-1}(\sqrt{P/(2A^2)})/(2\pi d))$. An example of the sum of the two signals normalized with the received power on one antenna is plotted as a first received signal strength indicator (RSSI$_1$) in FIG. 7. However, RSSI$_1$ is symmetric with respect to $\theta_i = 0$. The sign of θ_i can be evaluated using the derivative of RSSI$_1$, measured by connecting an inductor as shown in FIGS. 6B and 6C and calculating the difference in the received signal strengths (RSSI$_2$ and RSSI$_3$). An example of RSSI$_2$ - RSSI$_3$ is plotted in FIG. 7. Direction of arrival can be successfully estimated over a

range of θ_i from -60 degrees to +60 degrees. For $|\theta_i| > 60$ degrees, $RSSI_1$ is less than -13dB and the required phase gradient, $\phi_A = 0$ degrees.

[0024]   Turning to FIG. 8, a schematic 800 of an example of a tag architecture in accordance with some embodiments is provided. As shown, the tag can include an array of antennas 802 (e.g., such as a 3x3 array as illustrated). Any suitable number and any suitable type of antennas can be used in the array in some embodiments. For example, a 3x3 antenna array using patch antennas sized 3cm by 3.8cm with a 6.5cm center-to-center spacing on a 31mil-thick ISOLA 370HR substrate can be used for a 2.45GHz signal in some embodiments.

[0025]   Each antenna can be connected to a pole terminal of a single pole, multiple throw switch 804. This switch can be used to switch the antenna load for load modulation and determine the direction of arrival. Any suitable switch can be used as switch 804 in some embodiments, and the switch can have any suitable number of throw terminals. For example, in some embodiments, an SP5T switch (SKY13415) available from SKYWORKS SOLUTIONS, INC. of Woburn, Massachusetts can be used as switch 804. Moreover, in some embodiments, a combination of switches can be used to realize switch 804.

[0026]   As shown in the figure, the throw terminals of the switches can be connected to inductors 806, capacitors 808, a fixed voltage (e.g., such as a ground voltage), and inputs to power combiners in some embodiments. Any suitable inductor(s), capacitor(s), and fixed voltage(s) can be used in some embodiments. For example, in some embodiments, an inductor 806 can be an SMD 3nH 0201 inductor available from MURATA MANUFACTURING COMPANY, LTD. of Kyoto, Japan. As another example, in some embodiments, a capacitor 808 can be a 1.3pF 0402 capacitor available from AVX Corporation of Greenville, South Carolina, USA.

[0027]   Antennas 1 and 2 (Ant 1 and Ant 2) can provide a first pair of antennas and are connected to a first power combiner 810. Antennas 3 and 4 (Ant 3 and Ant 4) can provide a second pair of antennas and are connected to a second power combiner 812. Antennas 5 and 6 (Ant 5 and Ant 6) can provide a third pair of antennas and are connected to a third power combiner 814. Antennas 7 and 8 (Ant 7 and Ant 8) can provide a fourth pair of antennas and are connected to a fourth power combiner 816. And antenna 9 (Ant 9) can provide a reference antenna.

[0028]   As shown, the outputs of the four power combiners (810, 812, 814, and 816) and antenna 9 can each be connected to a rectifier (e.g., rectifiers 818 and 820). Any suitable power combiners can be used in some embodiments. For example, in some embodiments, a SP-2U2+ available from Mini-Circuits of Brooklyn, New York can be used.

[0029]   The five rectifiers can be also connected to the inputs of five analog to digital converters (this connection and the analog to digital converters (ADCs 822 and 824) are only shown for the first pair of antennas and the second pair of antennas for clarity of the figure). The ADCs can be used to digitize the output of the power detectors. Any suitable ADCs can be used in some embodiments.

[0030]   As shown in FIG. 8, the analog to digital converters can be part of a Micro-Controller Unit (MCU) 826 in some embodiments. The MCU can also include a controller that determines the direction of arrival (DoA) and the required load configuration (for controlling the direction of the backscatter), a baseband modulator (for QPSK modulation), and a local oscillator. Any suitable MCU can be used in some embodiments. For example, in some embodiments, the MCU can be implemented using a Teensy 3.6 MCU available from Paul Stoffregen of Sherwood, Oregon.

[0031] FIG. 9 provides a more specific example of a schematic of a portion of a tag in accordance with some embodiments. As illustrated, FIG. 9 only shows two antennas, two switches (and associated inductors and capacitors), a single power combiner, and a single power detector for purposes of clarity. It should be understood that replicas of these components could be provided for each pair of antennas in a tag having any suitably sized array in some embodiments.

[0032] As shown in FIG. 9, each antenna can be connected to a single pole, multiple throw switch, which can be implemented using part number 863-1583-1-ND from Skyworks Solutions, Inc. of Woburn, Massachusetts in some embodiments. One throw terminal of each switch can be connected to one side of a 3nH inductor (which can be for a 2.4GHz implementation; any other suitable value can be used in some embodiments), whose other side is connected to a fixed voltage level, such as ground. Another throw terminal of each switch can be connected to the fixed voltage level, such as ground. Still another throw terminal of each switch can be floating. Yet another throw terminal of each switch can be connected to one side of a 1.2pF capacitor (which can be for a 2.4GHz implementation; any other suitable value can be used in some embodiments), whose other side is connected to the fixed voltage level, such as ground. Still another throw terminal of each switch can be connected to the input of a power combiner. In some embodiments, the power combiner can be implemented using part number SP-2U2+ from Mini-Circuits of Brooklyn, New York. The output of the power combiner can be connected to the input of a power detector, which can be implemented using part number LT5538 from Analog Devices of Norwood, Massachusetts. The output of the power detector can be connected to analog to digital converter input of an MCU. In some embodiments, the MCU can be implemented using a Teensy 3.6 MCU available from Paul Stoffregen of Sherwood, Oregon.

[0033] Turning to FIG. 10, an example 1000 of a process that can be implemented in an MCU in accordance with some embodiments is shown. As illustrated, after process 1000 begins, at 1002 the process can configure the switches for each antenna. For example, for Ant 1 (which is illustrated in FIG. 8 as having five sub-switches) to have $\Gamma_1=0$, S_1 can be configured to have the top sub-switch open, the second from the top (grounded) sub-switch closed, the inductor sub-switch and the capacitor sub-switch open, and the bottom sub-switch closed, and for Ant 2 (which is also illustrated in FIG. 8 as having five sub-switches) to have $\Gamma_2=0$, S_2 can be configured to have the top four sub-switches open and the bottom sub-switch open.

[0034] Next, at 1004, process 1000 can measure the received signal strength indication (RSSI) from Ant 1 as $RSSI_{ref,A}$. Alternatively, in some embodiments, $RSSI_{ref,A}$ can be measured using a dedicated reference antenna, such as the center antenna in FIG. 8, in which case 1002 and 1004 can be modified accordingly.

[0035] Then, at 1006, process 1000 can re-configure the switches for each antenna. For example, for Ant 1 to have $\Gamma_1=0$, S_1 can be configured to have the top four sub-switches open and the bottom sub-switch closed, and for Ant 2 to have $\Gamma_2=0$, S_2 can be configured to have the top four sub-switches open and the bottom sub-switch closed.

[0036] At 1008, process 1000 can then measure $RSSI_A$ using an analog to digital converter coupled to the center antenna of FIG. 8 by a rectifier or power detector, and then calculate $RSSI_{norm}$ (in dB) as $RSSI_A$ (in dB) minus $RSSI_{ref,A}$ (in dB).

[0037] Next, at 1010, process 1000 can evaluate $|\theta_i|$ using:

$$\theta_i = sin^{-1}(\lambda.cos^{-1}(\sqrt{RSSI_{norm}/4})/(2\pi d)).$$

where d is the distance between the antennas, λ is the wavelength of the received signal.

[0038] Then, at 1012, process 1000 can re-configure the switches for each antenna. For example, for Ant 1 to have $\Gamma_1=1i$, S_1 can be configured to have the top two sub-switches open,

the inductor sub-switch closed, the capacitor sub-switch open, and the bottom sub-switch closed, and for Ant 2 to have $\Gamma_2=-1i$, S_2 can be configured to have the top two sub-switches open, the inductor sub-switch open, the capacitor sub-switch closed, and the bottom sub-switch closed. At 1012, process 1000 can then measure $RSSI_2$.

[0039]   At 1014, process 1000 can then re-configure the switches for each antenna. For example, for Ant 1 to have $\Gamma_1=-1i$, S_1 can be configured to have the top two sub-switches open, the inductor sub-switch open, the capacitor sub-switch closed, and the bottom sub-switch closed, and for Ant 2 to have $\Gamma_2=1i$, S_2 can be configured to have the top two sub-switches open, the inductor sub-switch closed, the capacitor sub-switch open, and the bottom sub-switch closed. At 1014, process 1000 can then measure $RSSI_3$.

[0040]   Next, at 1016, process 1000 can determine the sign of $RSSI_2$ minus $RSSI_3$ and infer from that sign the sign of $|\theta_i|$.

[0041]   Then, at 1018, process 1000 can map θ_i to ϕ_A (the horizontal phase gradient).

[0042]   At 1020, process 1000 can repeat steps 1002-1018 as described above using Ant 3, Ant 4, S3, and S4 instead of Ant 1, Ant 2, S1, and S2, respectively, for the vertical phase gradient (ϕ_B). Alternatively, steps similar to steps 1002-1018 using Ant 3, Ant 4, S3, and S4 instead of Ant 1, Ant 2, S1, and S2, respectively, can be performed in parallel to steps 1002-1018 for the vertical phase gradient (ϕ_B) in some embodiments.

[0043]   Finally, at 1022, the tag can be configured and modulated for data. For example, QPSK modulation can be used to transmit data such as a serial number, data stored in the tag, etc.

[0044]   In some embodiment, other antennas in an array can also be used in process 1000 to improve accuracy. For example, each RSSI measurement made for antennas 1 and 2 of FIG. 8 can also be made for antennas 5 and 6 of FIG. 8 and the average of the two RSSI measurements

used. As another example, each RSSI measurement made for antennas 3 and 4 of FIG. 8 can also be made for antennas 7 and 8 of FIG. 8 and the average of the two RSSI measurements used.

[0045]   In some embodiments, assuming area constrained applications, using N times the carrier frequency with antenna aperture similar to 1x1 array improves the range $\sqrt{N^3}$ times. In some embodiments, increasing the number of antennas and antenna loads allows higher order modulations with narrower beams for more efficient data transfer or security from unwanted readers.

[0046]   In some embodiments, direction of arrival estimation performance can be improved by mitigating interference using band select filters placed before each power detector.

[0047]   Although specific components are described herein, it should be apparent that other components can be used to provide the same or similar functions and/or additional functions in some embodiments. For example, while an MCU is described herein as performing certain processes, it should be apparent that any suitable hardware processor (e.g., microprocessor, controller, digital signal processor, dedicated logic, and/or any other suitable circuitry) can be used to perform some or all of these processes in some embodiments. As another example, in some embodiments, memory and/or storage can be used to store programs, data, and/or any other suitable information in some embodiments. For example, memory and/or storage can include random access memory, read-only memory, flash memory, hard disk storage, optical media, and/or any other suitable memory.

[0048]   In some embodiments, at least some of the above described blocks of the process of FIG. 10 can be executed or performed in any order or sequence not limited to the order and sequence shown in and described in connection with the figure. Also, some of the above blocks of FIG. 10 can be executed or performed substantially simultaneously where appropriate or in

parallel to reduce latency and processing times. Additionally or alternatively, some of the above described blocks of the process of FIG. 10 can be omitted.

[0049]   In some embodiments, any suitable computer readable media can be used for storing instructions for performing the functions and/or processes herein. For example, in some embodiments, computer readable media can be transitory or non-transitory. For example, non-transitory computer readable media can include media such as non-transitory forms of magnetic media (such as hard disks, floppy disks, and/or any other suitable magnetic media), non-transitory forms of optical media (such as compact discs, digital video discs, Blu-ray discs, and/or any other suitable optical media), non-transitory forms of semiconductor media (such as flash memory, electrically programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), and/or any other suitable semiconductor media), any suitable media that is not fleeting or devoid of any semblance of permanence during transmission, and/or any suitable tangible media. As another example, transitory computer readable media can include signals on networks, in wires, conductors, optical fibers, circuits, any suitable media that is fleeting and devoid of any semblance of permanence during transmission, and/or any suitable intangible media.

[0050]   Although the invention has been described and illustrated in the foregoing illustrative embodiments, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the details of implementation of the invention can be made without departing from the spirit and scope of the invention, which is limited only by the claims that follow. Features of the disclosed embodiments can be combined and rearranged in various ways.

What is claimed is:

1.   A system for a multi-antenna, directional backscatter tag, comprising:

a plurality of antennas;

a plurality of single pole, multiple throw switches each having a pole terminal connected to a corresponding one of the plurality of antennas, and each having a first throw terminal connected to a first side of an inductor for that switch, a second throw terminal connected to a first side of a capacitor for that switch, a third throw terminal connected to a fixed voltage level, a fourth throw terminal that is floating, and a fifth throw terminal, wherein a second side of the inductor and a second side of the capacitor are connected to the fixed voltage level;

a power combiner having inputs connected to the fifth throw terminal of each of two of the plurality of single pole, multiple throw switches and having an output;

a power detector having an input connected to the output of the power combiner and having an output;

an analog to digital converter having an input connected to the output of the power detector and having an output;

a hardware processor coupled to the output of the analog to digital converter and coupled to a control terminal of each of the plurality of single pole, multiple throw switches.

2.   The system of claim 1, wherein the fixed voltage level is ground.

3.   The system of claim 1, wherein hardware processor is configured to configure:

a first switch of the two of the plurality of single pole, multiple throw switches so that the pole terminal of the first switch is connected to the fifth throw terminal of the first switch but not

to the first pole terminal, the second pole terminal, the third pole terminal, or the fourth pole terminal of the first switch; and

a second switch of the two of the plurality of single pole, multiple throw switches so that the pole terminal of the connected switch is connected to the fifth throw terminal and the third throw terminal of the second switch but not to the first pole terminal, the second pole terminal, or the fourth pole terminal of the second switch.

4.   The system of claim 3, wherein hardware processor is further configured to configure:

the first switch of the two of the plurality of single pole, multiple throw switches so that the pole terminal of the first switch is connected to the fifth throw terminal of the first switch but not to the first pole terminal, the second pole terminal, the third pole terminal, or the fourth pole terminal of the first switch; and

the second switch of the two of the plurality of single pole, multiple throw switches so that the pole terminal of the connected switch is connected to the fifth throw terminal of the second switch but not to the first pole terminal, the second pole terminal, the third pole terminal, or the fourth pole terminal of the second switch.

5.   The system of claim 4, wherein hardware processor is further configured to configure:

the first switch of the two of the plurality of single pole, multiple throw switches so that the pole terminal of the first switch is connected to the fifth throw terminal and the first throw terminal of the first switch but not to the second pole terminal, the third pole terminal, or the fourth pole terminal of the first switch; and

the second switch of the two of the plurality of single pole, multiple throw switches so that the pole terminal of the connected switch is connected to the fifth throw terminal and the

second throw terminal of the second switch but not to the first pole terminal, the third pole

terminal, or the fourth pole terminal of the second switch.

6.   The system of claim 5, wherein hardware processor is further configured to configure:

        the first switch of the two of the plurality of single pole, multiple throw switches so that

the pole terminal of the first switch is connected to the fifth throw terminal and second throw

terminal of the first switch but not to the first pole terminal, the third pole terminal, or the fourth

pole terminal of the first switch; and

        the second switch of the two of the plurality of single pole, multiple throw switches so

that the pole terminal of the connected switch is connected to the fifth throw terminal and the

first throw terminal of the second switch but not to the second pole terminal, the third pole

terminal, or the fourth pole terminal of the second switch.

7.   The system of claim 3, wherein hardware processor is further configured to measure the

received power at two of the plurality of antennas.

8.   The system of claim 1, wherein the hardware processor is further configured to determine

a direction of arrival of an RF signal received at the plurality of antennas.

9.   The system of claim 8, wherein the hardware processor is further configured to configure

the plurality of single pole, multiple throw switches to cause the plurality of antennas to

backscatter an RF signal received at the plurality of antennas in the direction of arrival.

10.   The system of claim 1, wherein the hardware processor is further configured to QPSK modulate the plurality of antennas by controlling the plurality of single pole, multiple throw switches.
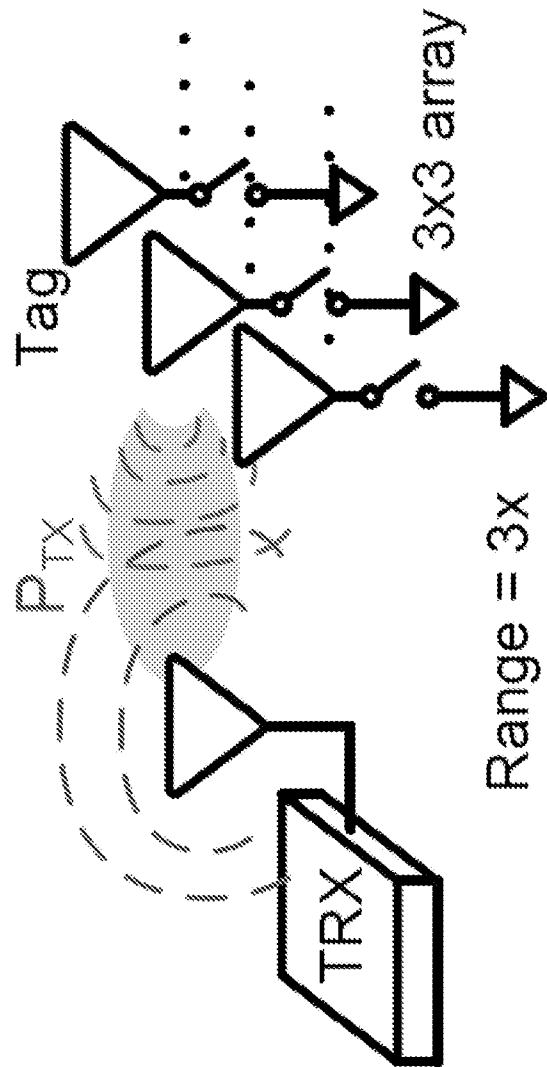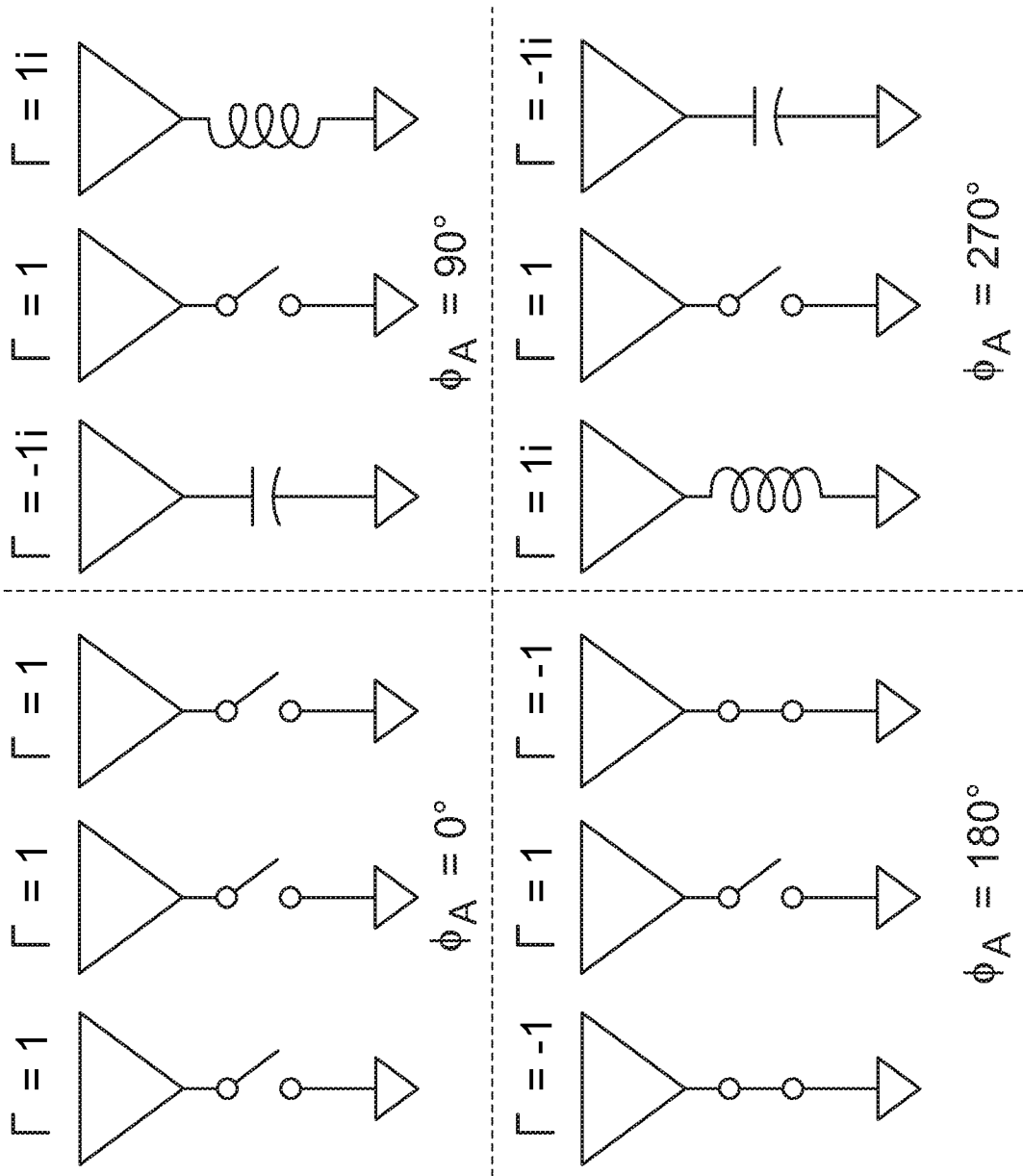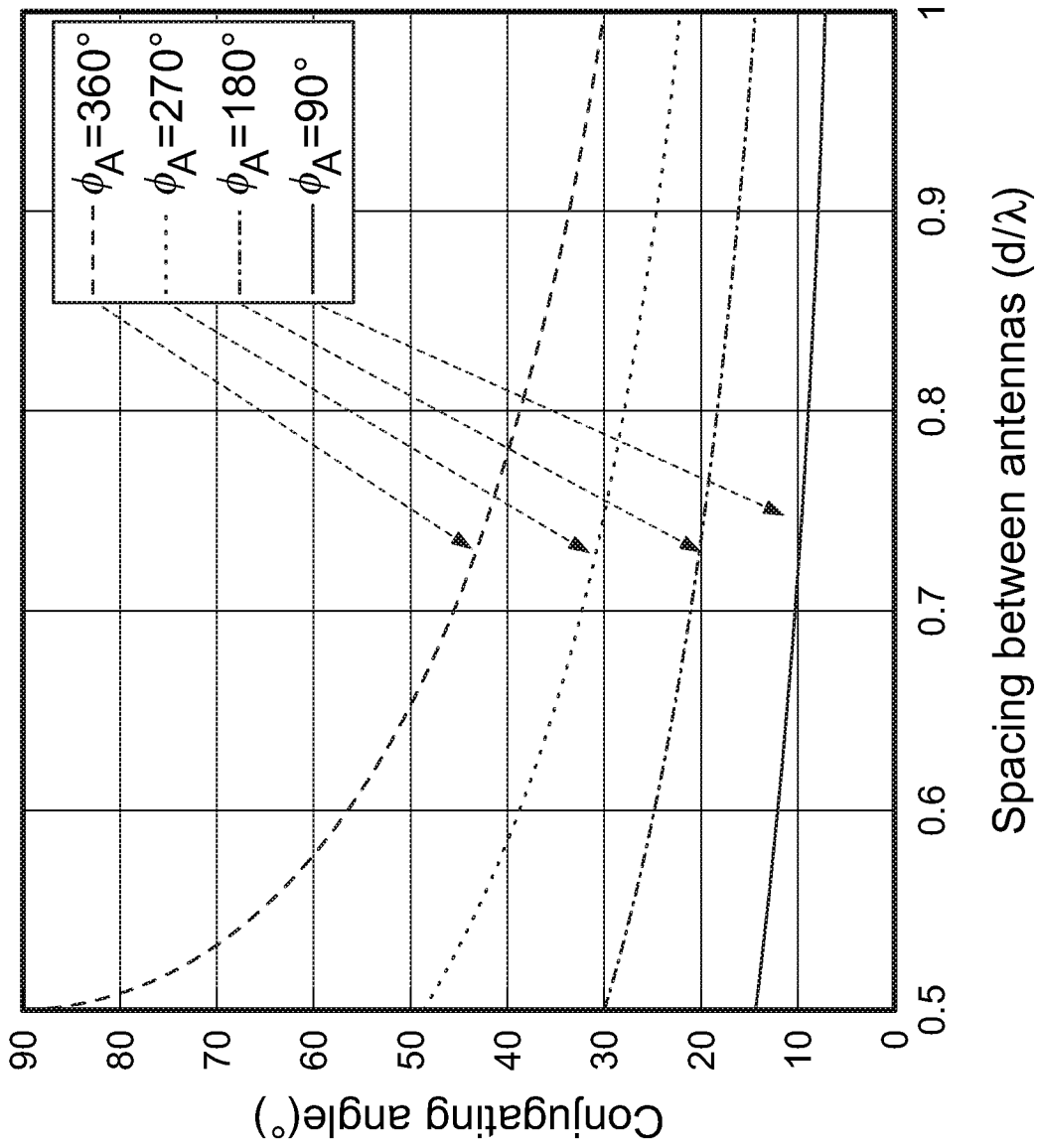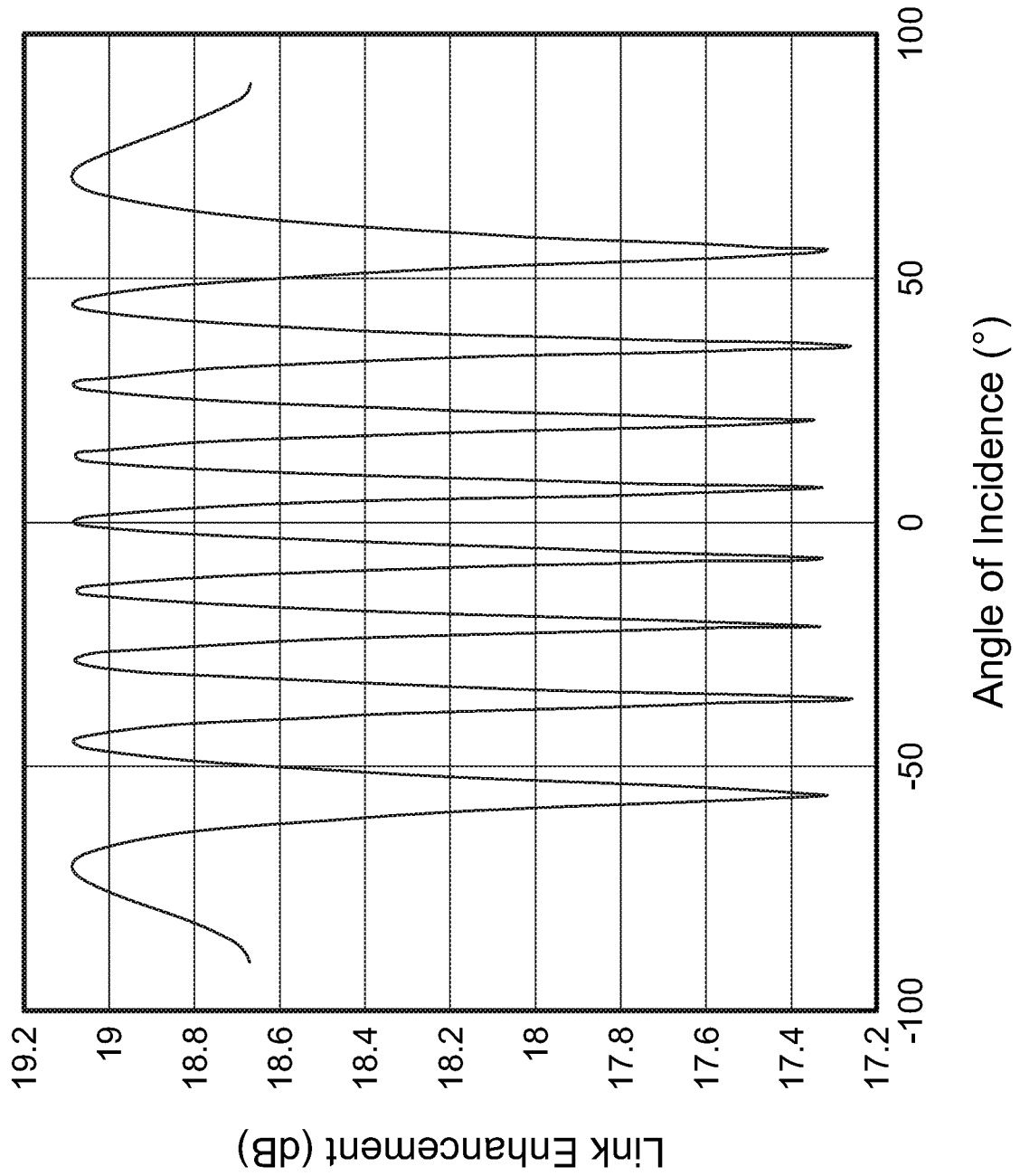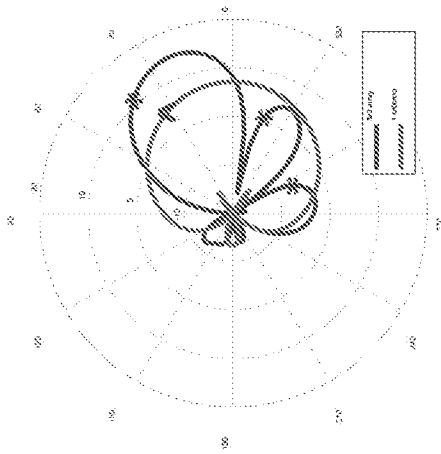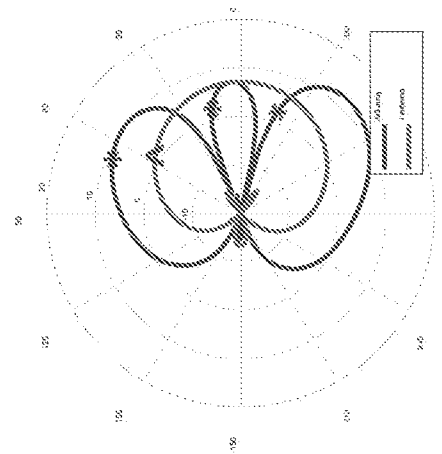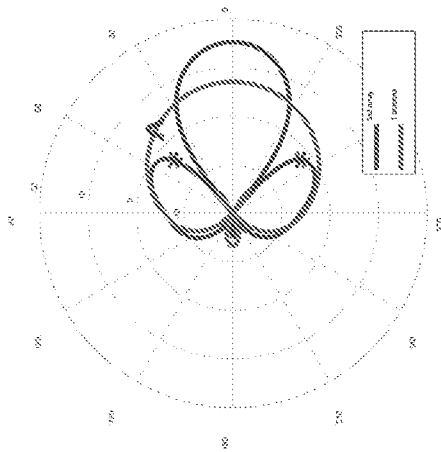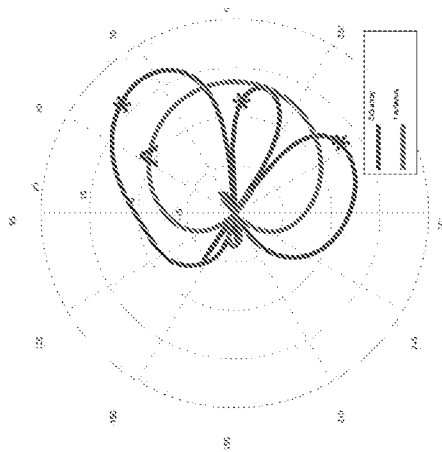
FIG. 1

FIG. 2

FIG. 3

FIG. 4

(a)

(b)

(c)

(d)

FIG. 5
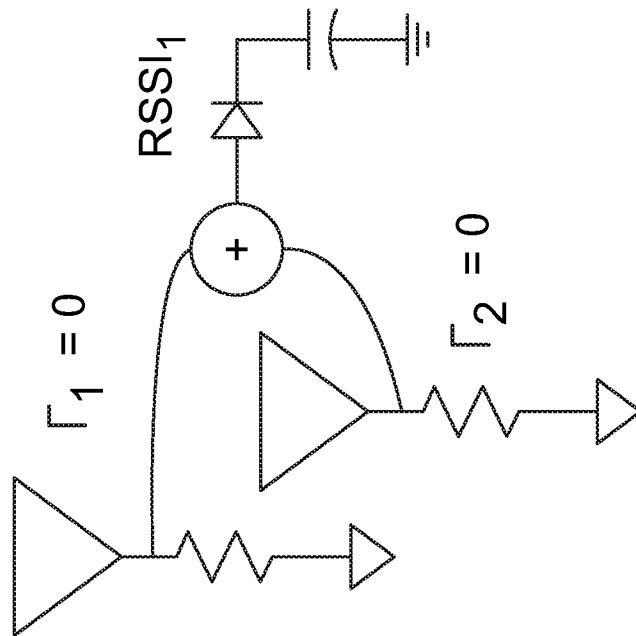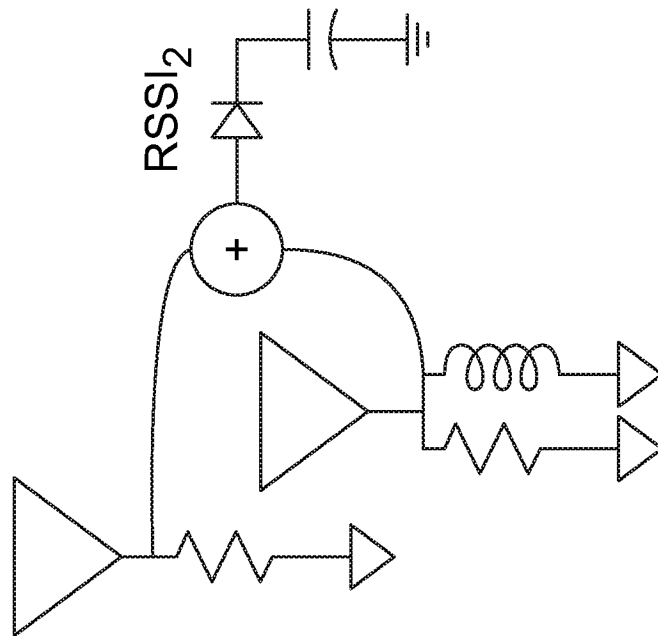
FIG. 6A

FIG. 6B
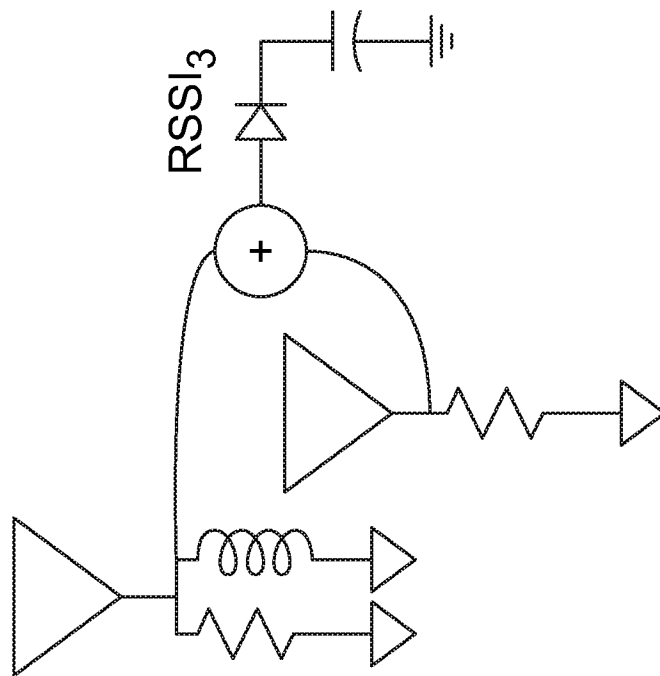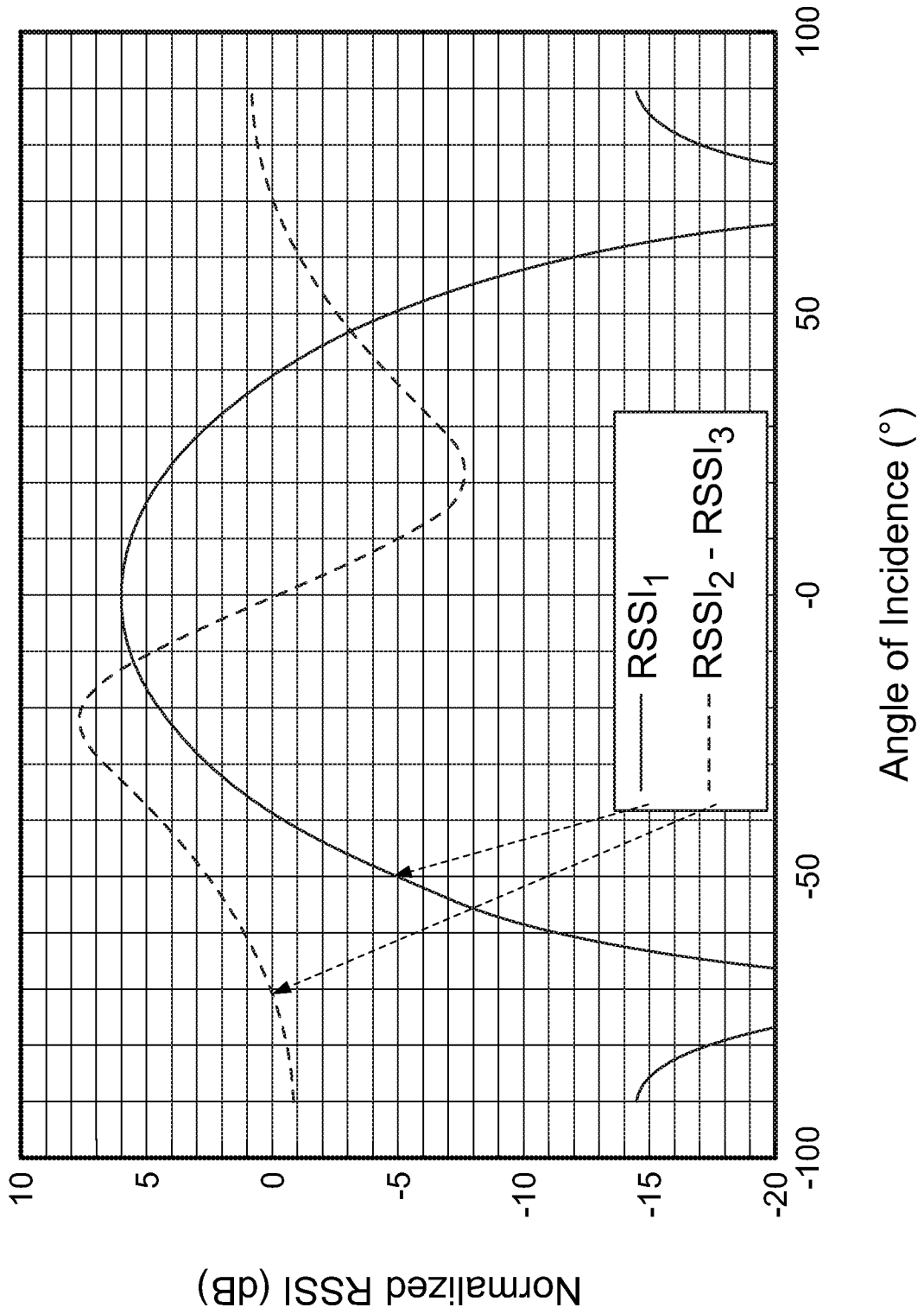
FIG. 6C

FIG. 7
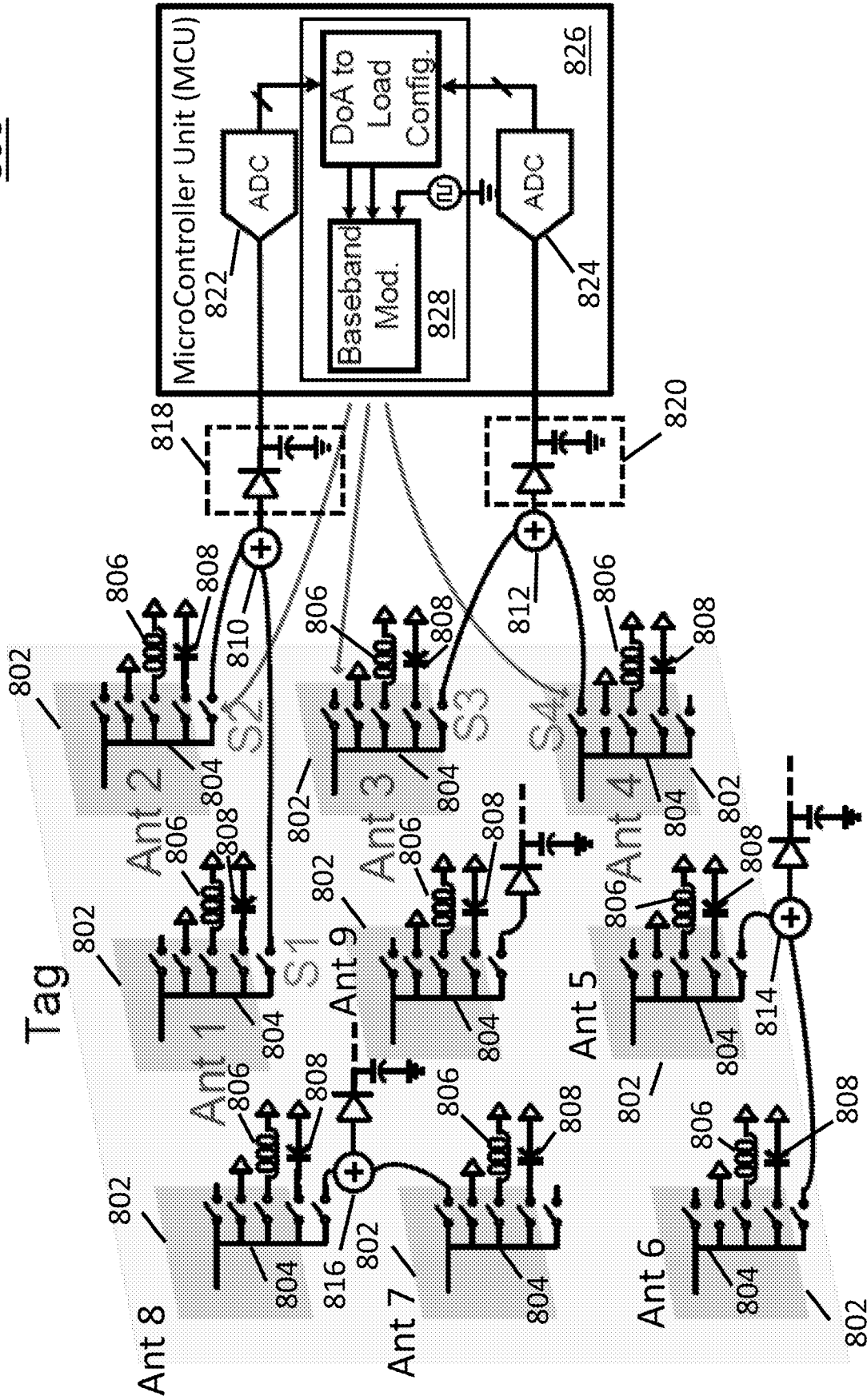
FIG. 8
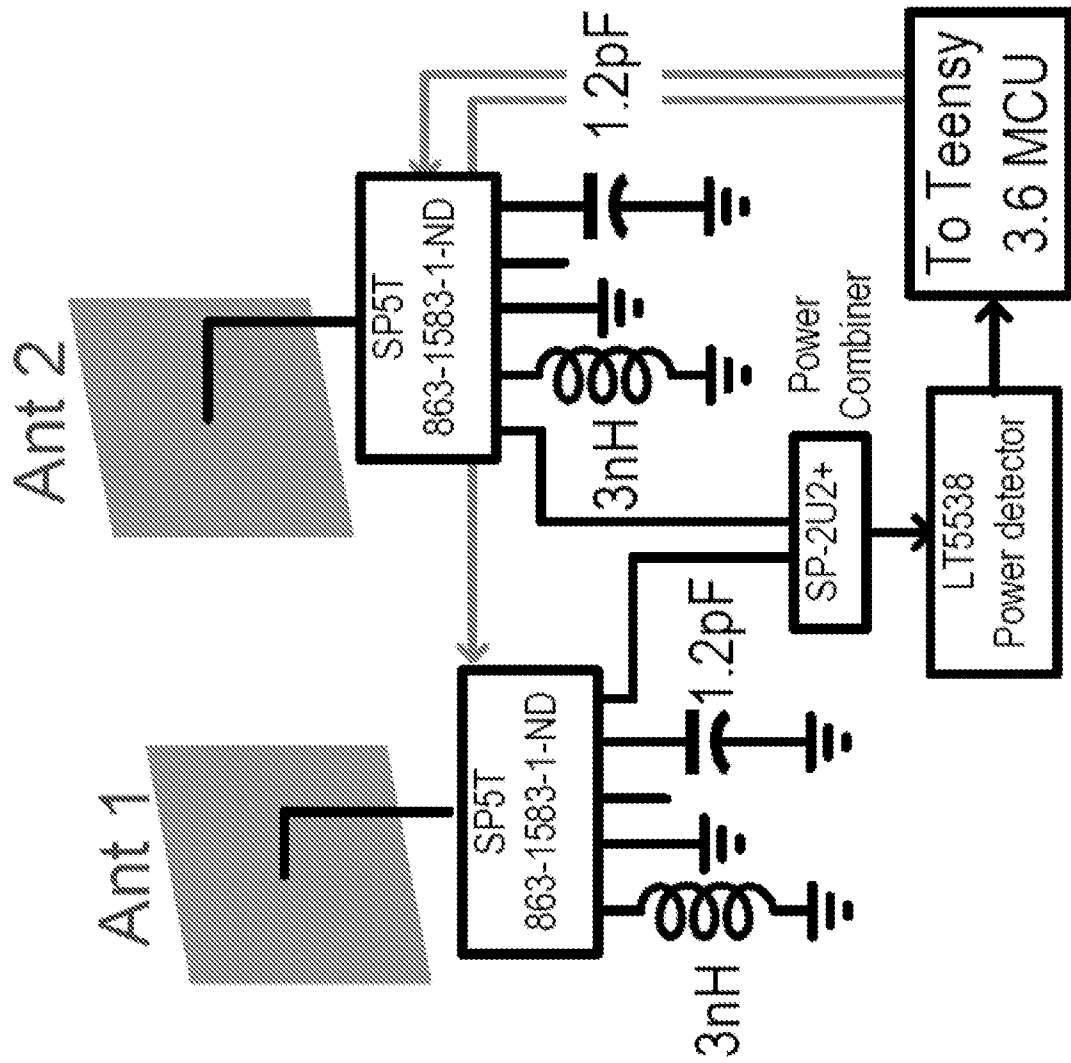
A 2.4GHz prototype implementation

FIG. 9

1000
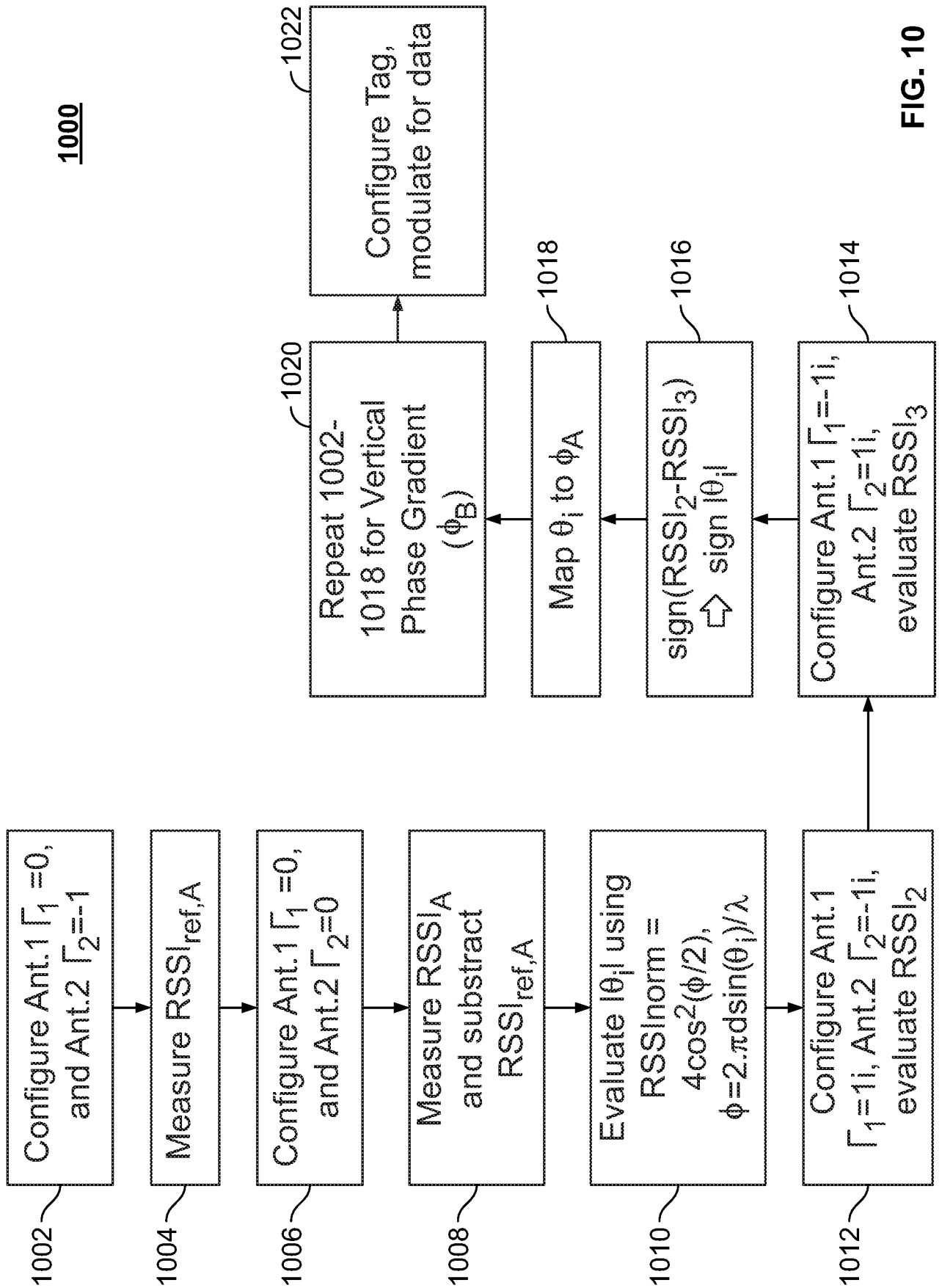
1022 Configure Tag, modulate for data

1020 Repeat 1002-1018 for Vertical Phase Gradient (ϕ_B)

1018 Map θ_i to ϕ_A

1016 sign($RSSI_2$-$RSSI_3$) ⇨ sign $|\theta_i|$

1014 Configure Ant.1 Γ_1=-1i, Ant.2 Γ_2=1i, evaluate $RSSI_3$

1002 Configure Ant.1 Γ_1=0, and Ant.2 Γ_2=-1

1004 Measure $RSSI_{ref,A}$

1006 Configure Ant.1 Γ_1=0, and Ant.2 Γ_2=0

1008 Measure $RSSI_A$ and subtract $RSSI_{ref,A}$

1010 Evaluate $|\theta_i|$ using $RSSInorm = 4cos^2(\phi/2)$, $\phi=2\pi dsin(\theta_i)/\lambda$

1012 Configure Ant.1 Γ_1=1i, Ant.2 Γ_2=-1i, evaluate $RSSI_2$

FIG. 10

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H04L 5/00; H04L 27/26; H04W 4/02 (2019.01)

CPC - G06K 19/073; G06K 7/10356; G06K 19/0723; G06K 19/07707; G06K 19/07709; H03H 11/245; H04L 5/0007; H04L 27/2602; H04L 27/34 (2019.08)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC - 340/10.1 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2015/0108210 A1 (ZHOU) 23 April 2015 (23.04.2015) entire document	1-10
A	WO 2017/132400 A1 (UNIVERSITY OF WASHINGTON) 03 August 2017 (03.08.2017) entire document	1-10
A	US 2008/0024279 A1 (GRAVELLE et al) 31 January 2008 (31.01.2008) entire document	1-10
A	US 8,390,431 B1 (DIORIO) 05 March 2013 (05.03.2013) entire document	1-10
A	US 9,680,533 B2 (GUDAN et al) 13 June 2017 (13.06.2017) entire document	1-10

☐ Further documents are listed in the continuation of Box C.   ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 November 2019	04 DEC 2019

Name and mailing address of the ISA/US	Authorized officer
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450	Blaine R. Copenheaver
Facsimile No. 571-273-8300	PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)