United States Patent [19]

Rowen

[11] **3,799,148**

[45] **Mar. 26, 1974**

[54] **TWO RECORDER APPARATUS FOR MONITORING HEART ACTION**

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[73] Assignee: **St. Mary's Hospital,** Milwaukee, Wis.

[22] Filed: **Jan. 13, 1972**

[21] Appl. No.: **217,475**

[52] **U.S. Cl.** ..... **128/2.06 A,** 128/2.06 G

[51] **Int. Cl.** **A61b 5/04**

[58] **Field of Search** ..... 73/DIG. 6; 307/235, 238; 324/76 R, 77 R, 78 D, 113; 340/415, 416, 248 A, 248 R, 248 B, 248 C, 253 Y, 253 Z, 253 R; 128/2.05 R, 2.06 A, 2.06 F, 2.06 G, 2.06 R, 2.06 Z

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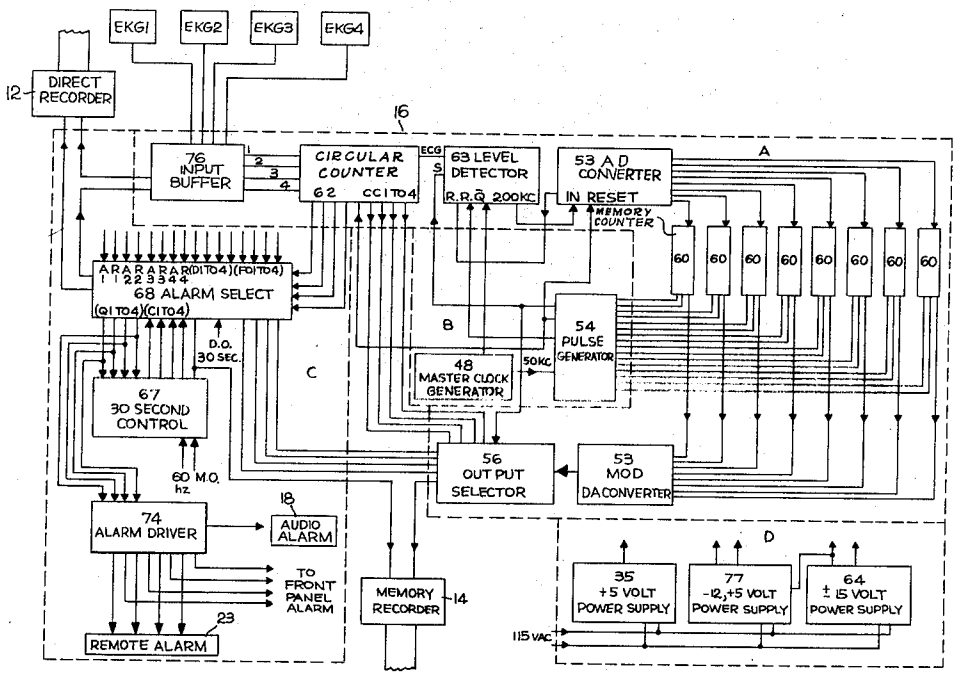
Primary Examiner—William E. Kamm
Attorney, Agent, or Firm—James E. Nilles

[57] **ABSTRACT**

Apparatus for monitoring the heart action of one or more coronary patients comprises an electrocardiograph (EKG) for each patient, a direct recorder connected to the EKG's for providing an electrocardiogram (ECG) of a patient's heart action in the event apparent heart action irregularity (arrhythmia) occurs, and a memory recorder for providing a reconstructed ECG of that patient's heart action during a 30 second interval just prior to onset of the apparent arrhythmia. The memory recorder is connected to a solid state memory unit which receives data from the EKG for each patient. Each EKG provides data in analog form and the solid state memory unit samples the analog, converts the sample analog to digital form (wherein binary numerical values correspond to amplitudes of the sample analog), stores the digital samples for about 30 seconds and reconverts the digital samples derived from any one of the EKG's to analog samples which are reconstructed into a wave form for use by the memory recorder on demand.

11 Claims, 18 Drawing Figures



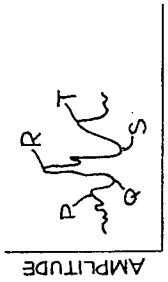


FIG.2

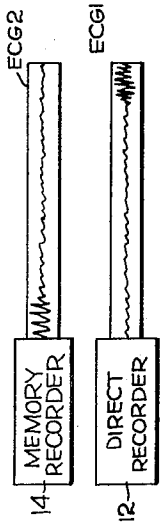


FIG.3

FIG.1

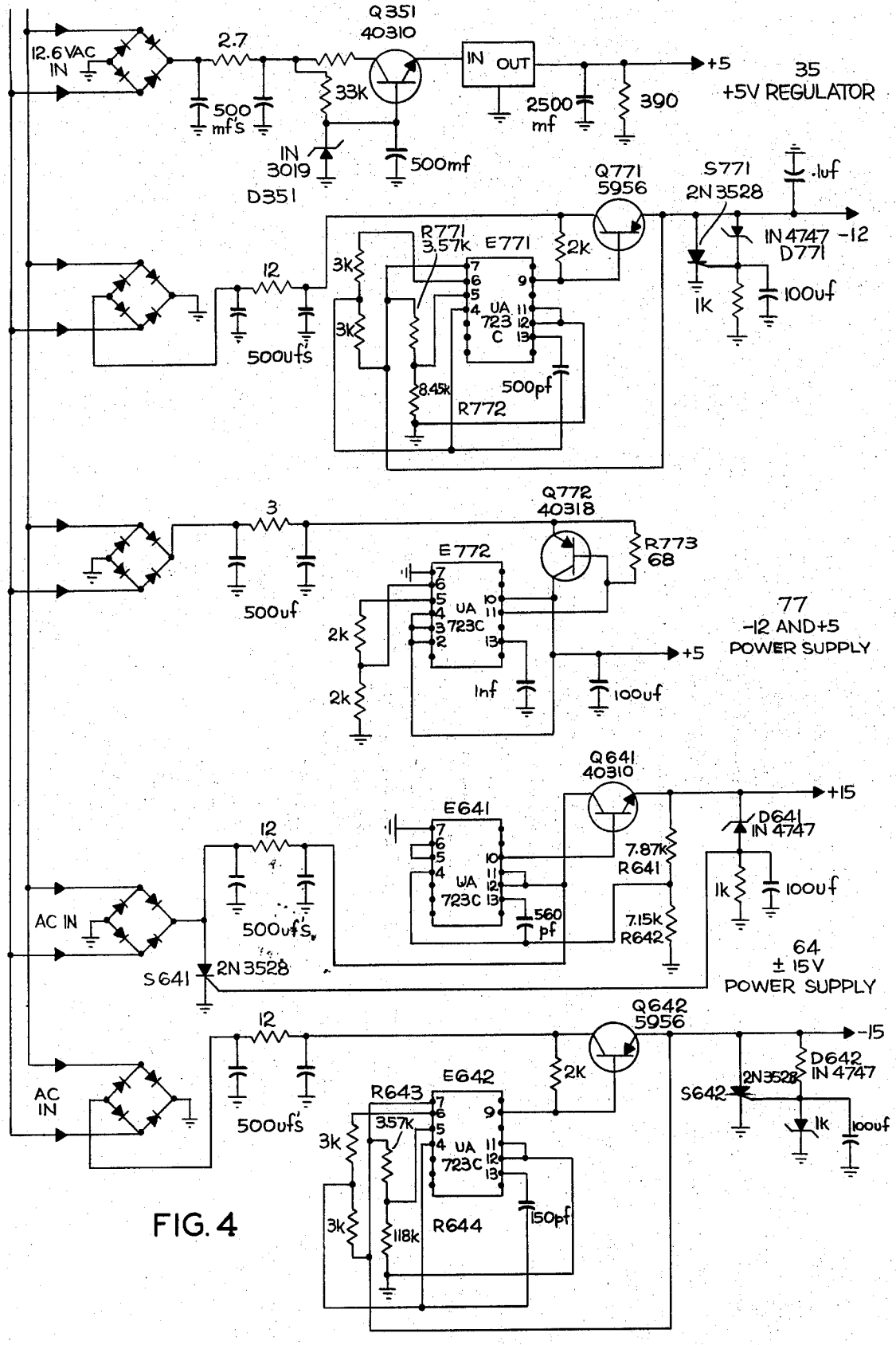

Q351
40310
12.6 VAC IN
2.7
500 mfs
33k
IN 3019
D351
500mf
IN OUT
2500 mf
390
+5
35
+5V REGULATOR
Q771
5956
S771
2N3528
.luf
IN4747
D771
-12
R771
3.57k
E771
2k
3k
3k
12
500ufs
UA 723 C
8.45k
R772
500pf
1k
100uf
Q772
40318
3
500uf
E772
R773
68
UA 723C
2k
2k
Inf
100uf
+5
77
-12 AND +5
POWER SUPPLY
Q641
40310
E641
+15
12
D641
IN 4747
7.87k
R641
1k
100uf
AC IN
500ufs
UA 723C
560 pf
7.15k
R642
S641
2N3528
64
± 15V
POWER SUPPLY
Q642
5956
12
-15
D642
IN 4747
2K
E642
R643
S642
2N3528
AC IN
500ufs
357k
3k
UA 723C
1k
100uf
3k
118k
R644
150pf

FIG. 4

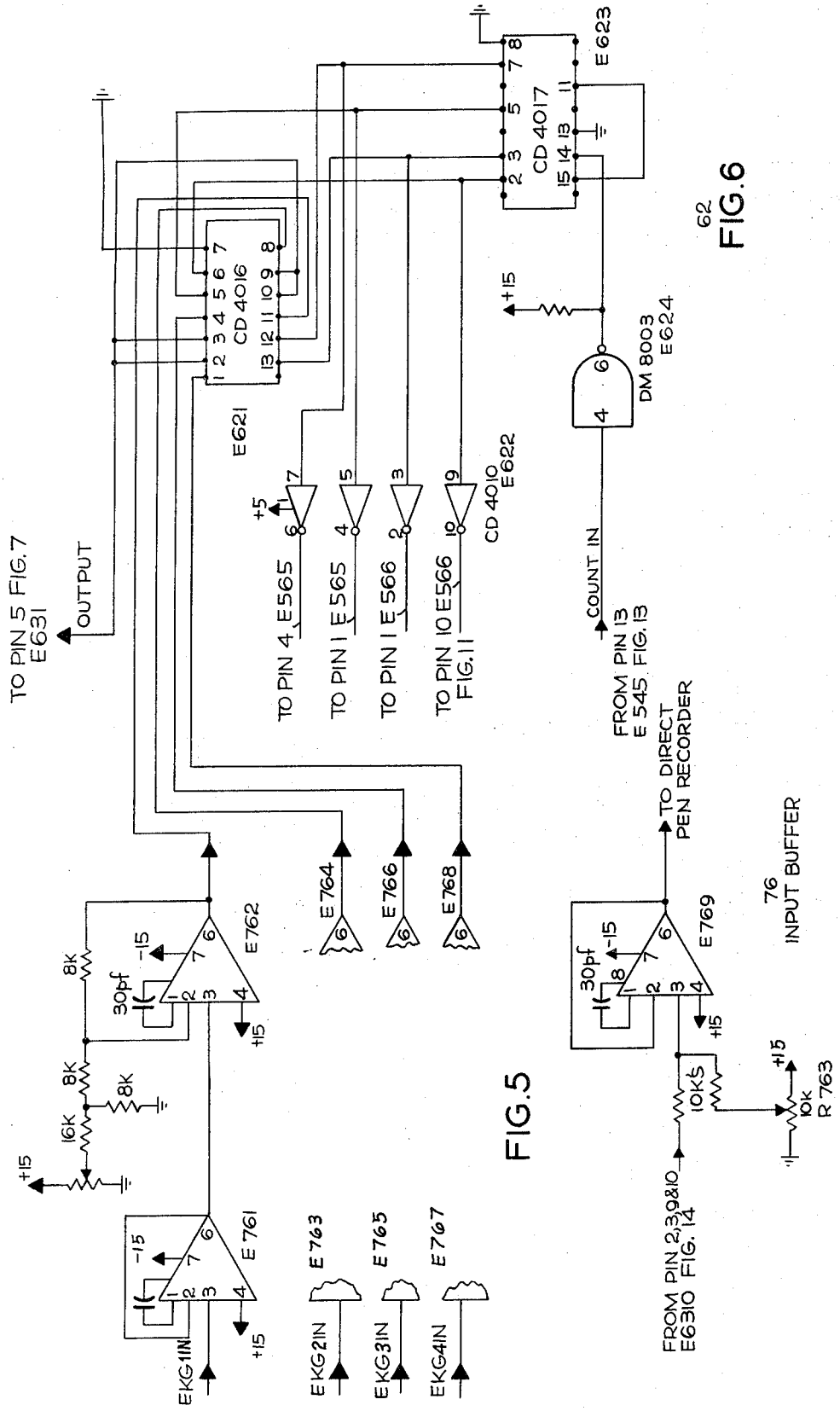

TO PIN 5 FIG. 7
E631
OUTPUT
CD 4016
E621
CD 4017
E623
CD 4010
E622
DM 8003
E624
+15
+5
TO PIN 4 E565
TO PIN 1 E565
TO PIN 1 E566
TO PIN 10 E566
FIG. 11
COUNT IN
FROM PIN 13
E 545 FIG. 13
TO DIRECT
PEN RECORDER
62
E762
E761
E763
E764
E765
E766
E767
E768
E769
8K
16K
30pf
-15
EKG1IN
EKG2IN
EKG3IN
EKG4IN
FROM PIN 2,3,9&10
E6310 FIG. 14
10KΩ
10K
R 763
76
INPUT BUFFER

FIG. 5

FIG. 6

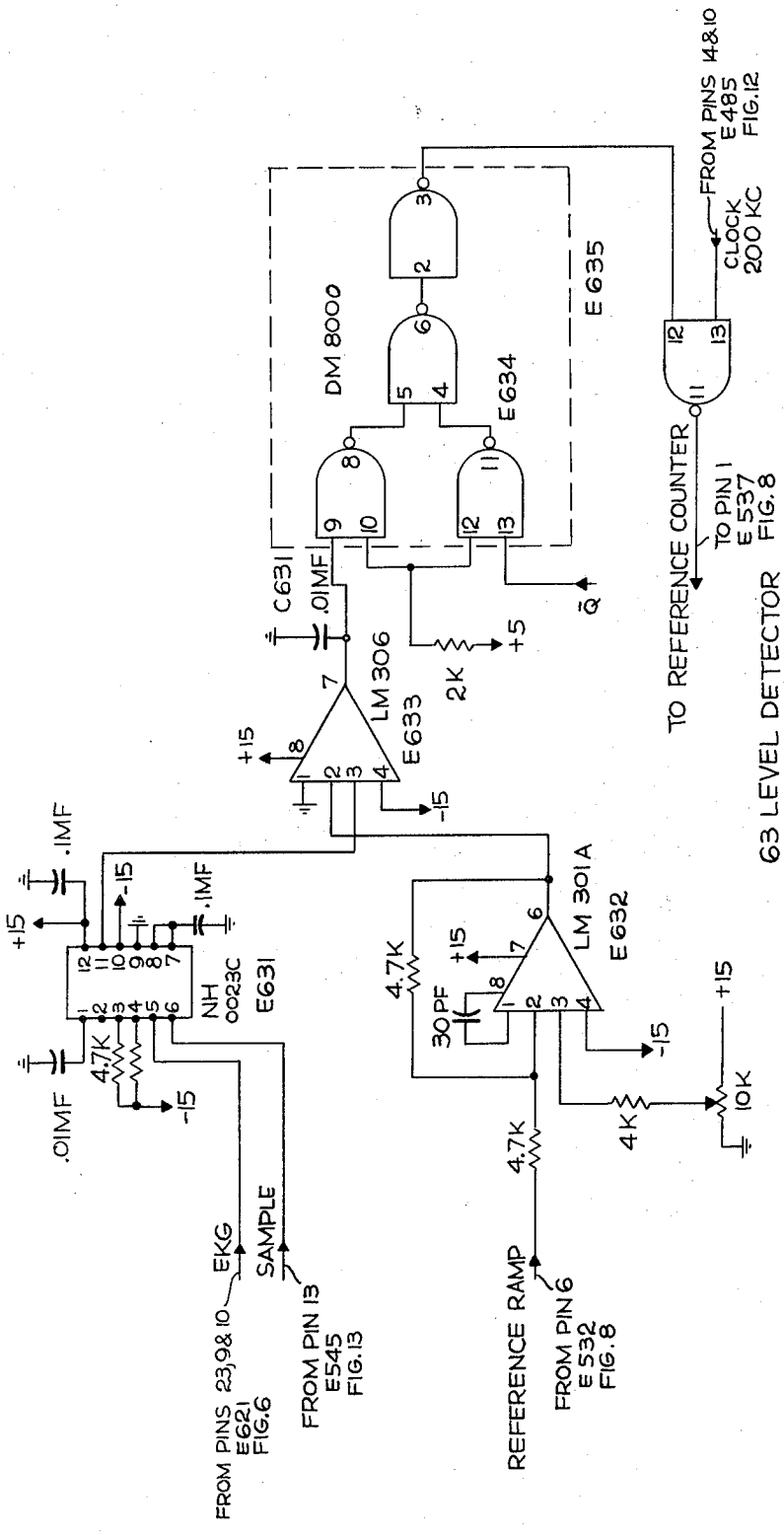

FROM PINS 14&10
E485
FIG.12
CLOCK
200 KC
E635
DM 8000
E634
TO REFERENCE COUNTER
TO PIN 1
E537
FIG.8
63 LEVEL DETECTOR
C631
.01MF
Q
+5
2K
LM 306
E633
+15
-15
.1MF
NH
0023C
E631
4.7K
.01MF
EKG
SAMPLE
FROM PINS 23,9& 10
E621
FIG.6
FROM PIN 13
E545
FIG.13
LM 301A
E632
30PF
4K
10K
REFERENCE RAMP
FROM PIN 6
E532
FIG.8

FIG.7

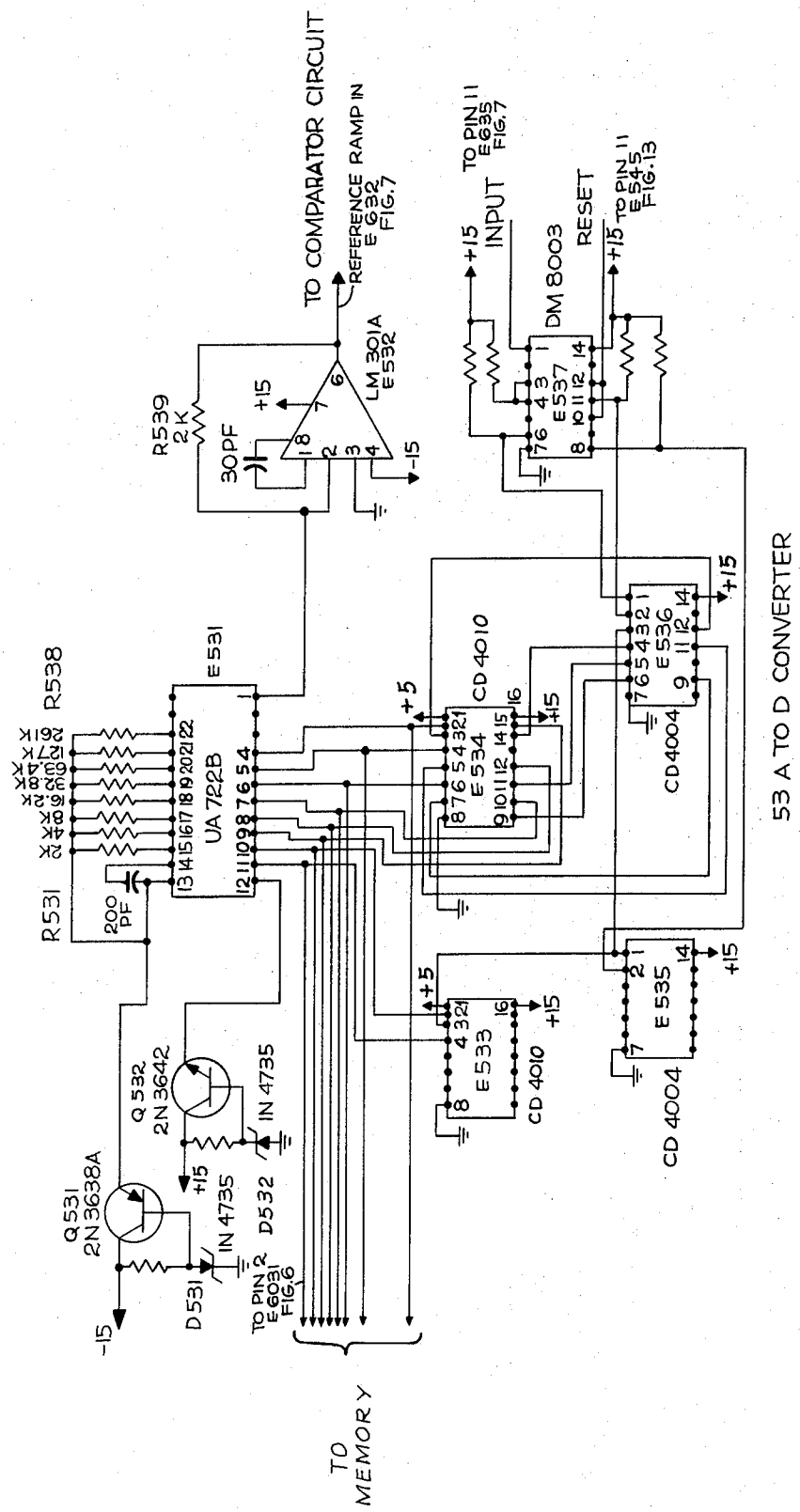

TO COMPARATOR CIRCUIT
REFERENCE RAMP IN
E 632
FIG. 7
LM 301A
E 532
R539
2K
30PF
+15
-15
TO PIN 11
E 635
FIG. 7
INPUT
DM 8003
RESET
TO PIN 11
E 545
FIG. 13
E 537
R538
E 531
UA 722B
R531
200 PF
CD 4010
E 534
E 536
CD 4004
E 533
E 535
Q 532
2N 3642
IN 4735
Q 531
2N 3638A
D 532
D 531
TO PIN 2
E 603
FIG. 6
TO MEMORY
53 A TO D CONVERTER

FIG. 8

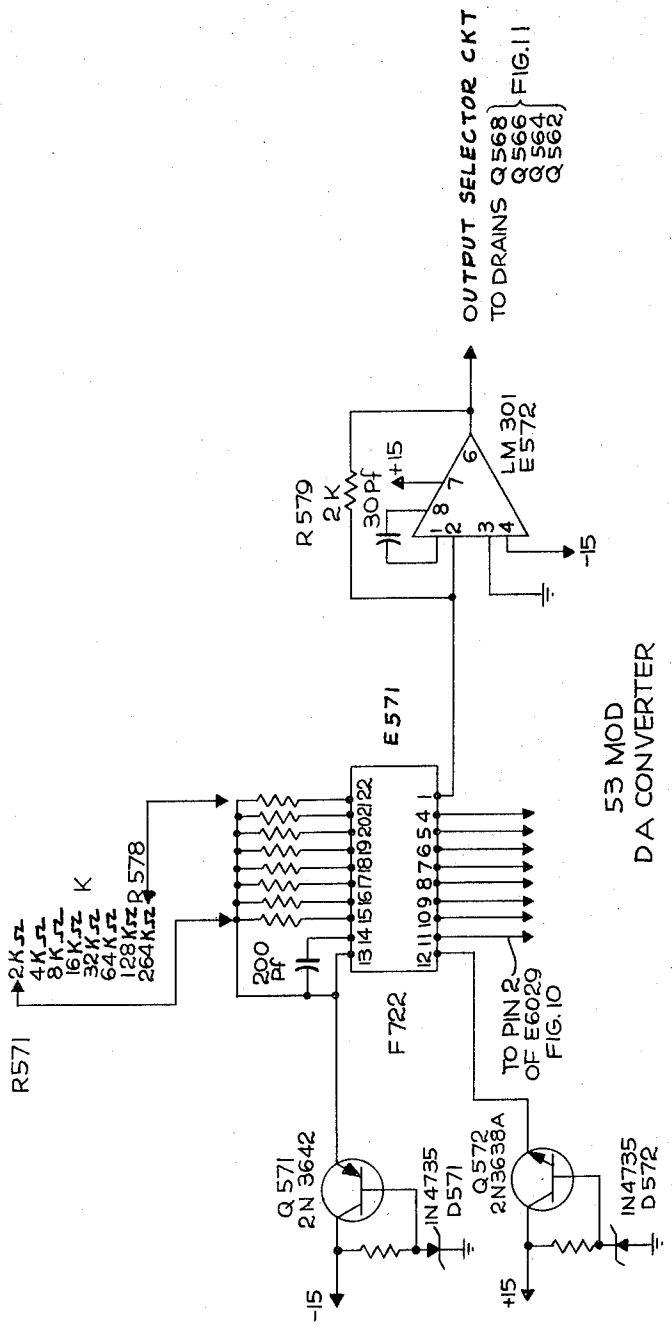

OUTPUT SELECTOR CKT
TO DRAINS Q568 Q566 Q564 Q562 } FIG.11
LM 301
E572
R 579
2 K
30 Pf
+15
-15
E571
R578
K
2K Ω
4K Ω
8K Ω
16K Ω
32K Ω
64K Ω
128K Ω
264K Ω
R571
200 Pf
F 722
TO PIN 2 OF E6029 FIG. 10
Q 571
2N 3642
IN4735
D571
Q 572
2N3638A
IN4735
D572
53 MOD
D A CONVERTER

FIG.9

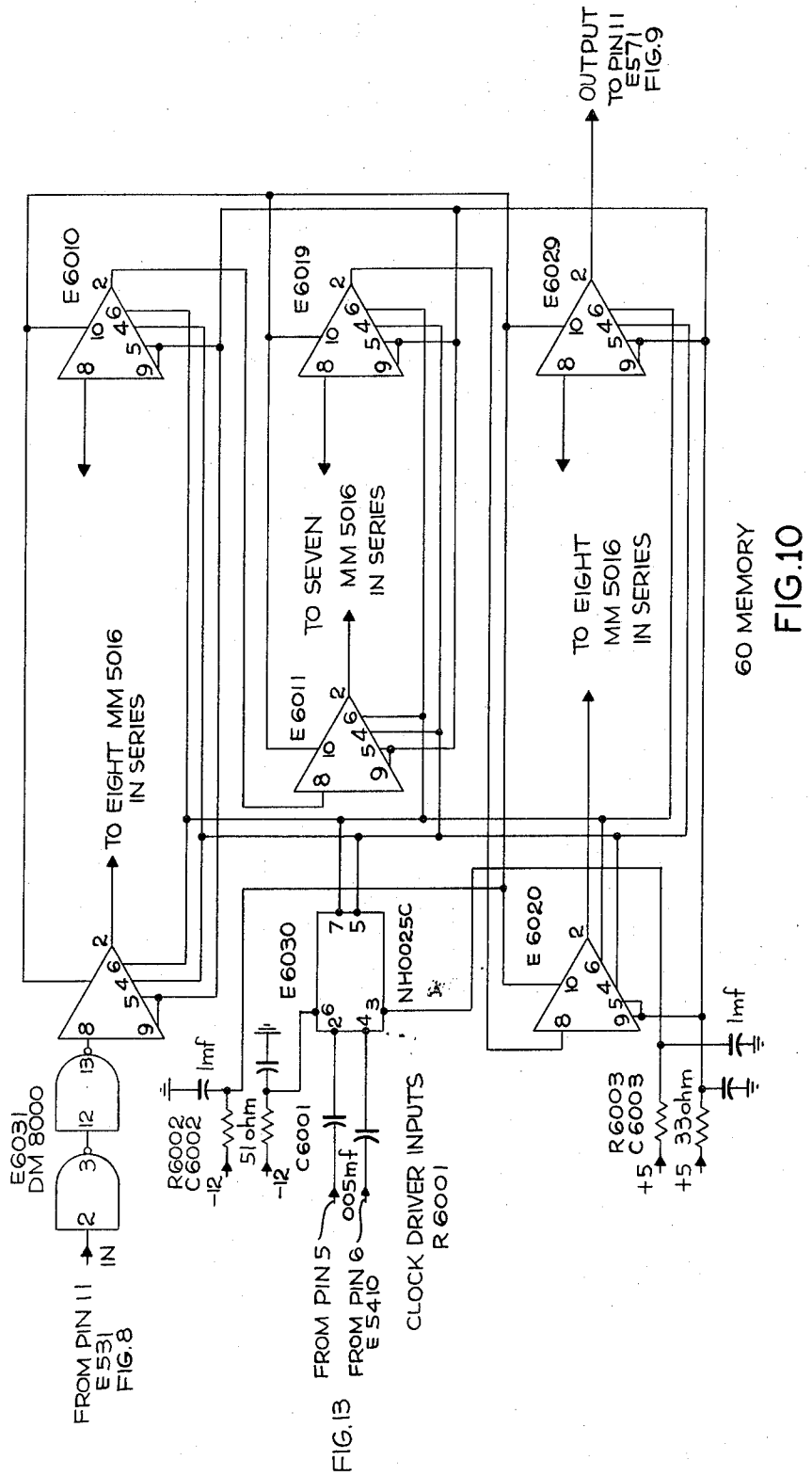

OUTPUT TO PIN 11 E571 FIG.9
E6010
E6019
E6029
TO SEVEN MM 5016 IN SERIES
TO EIGHT MM 5016 IN SERIES
TO EIGHT MM 5016 IN SERIES
60 MEMORY
E6011
E6030
NH0025C
E6020
E6031 DM 8000
FROM PIN 11 E531 FIG.8
IN
R6002 C6002
51ohm
C6001
FROM PIN 5
FROM PIN 6 E5410
.005mf
CLOCK DRIVER INPUTS R6001
R6003 C6003
+5
+5
33ohm
1mf
1mf
-12
-12

FIG.10

FIG.13

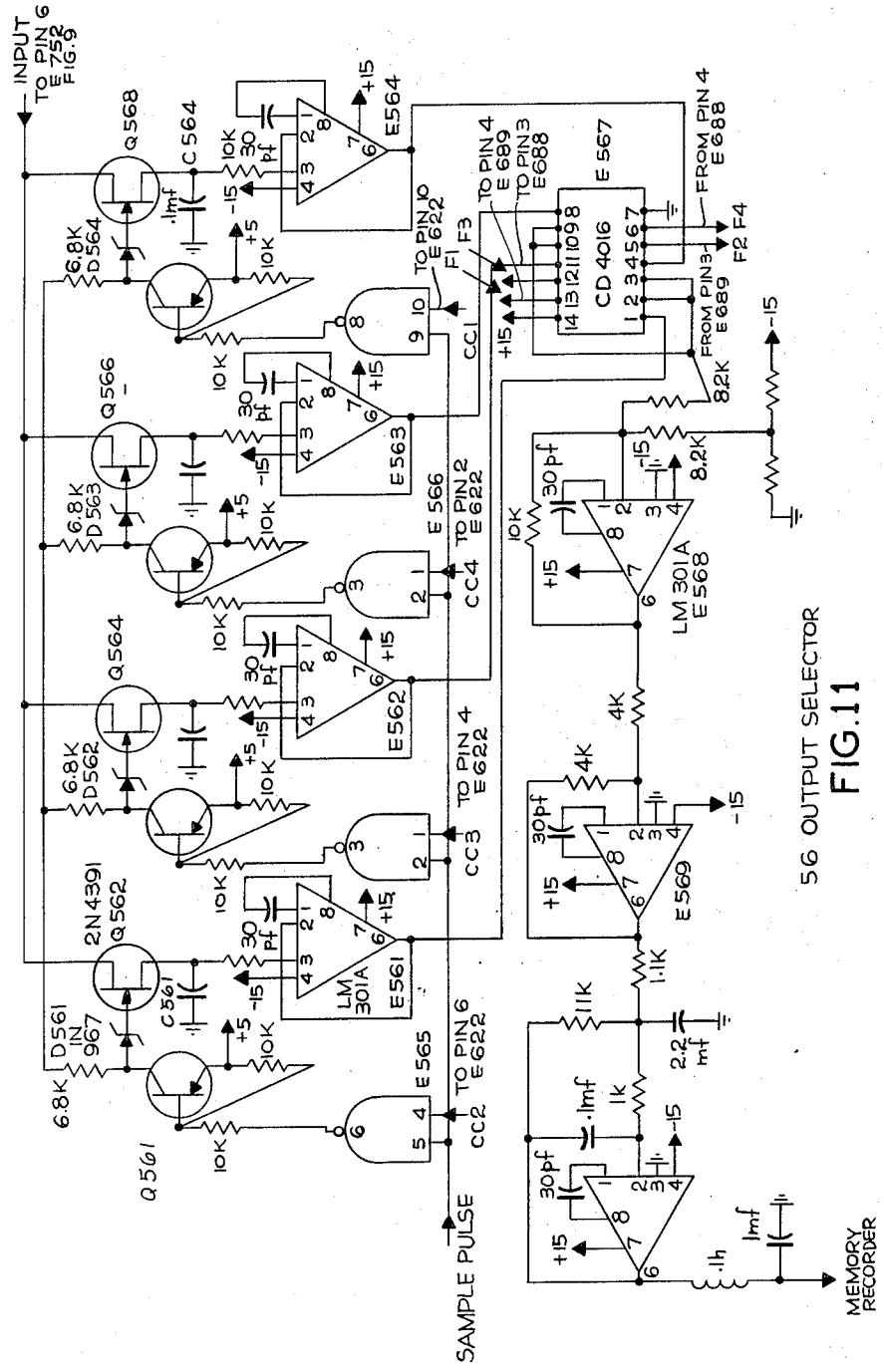

INPUT
TO PIN 6
E 752
FIG. 9
Q 568
C 564
.1mf
10K
30 pf
-15
+5
6.8K
D 564
E564
+15
TO PIN 10
E 622
F1 F3
TO PIN 4
E 689
TO PIN 3
E688
E 567
CD 4016
14 13 12 11 10 9 8
1 2 3 4 5 6 7
FROM PIN 4
E 688
F2 F4
FROM PIN 3
E 689
82K
Q 566
6.8K
D 563
E563
E 566
TO PIN 2
E 622
CC1
CC4
Q 564
6.8K
D 562
E562
TO PIN 4
E 622
CC3
2N4391
Q 562
D561
IN
967
C561
LM
301A
E561
E 565
TO PIN 6
E 622
CC2
Q 561
SAMPLE PULSE
LM 301A
E 568
8.2K
4K
30pf
E 569
1.1K
11K
2.2
mf
1K
.1mf
.1h
1mf
MEMORY
RECORDER
56 OUTPUT SELECTOR

FIG. 11

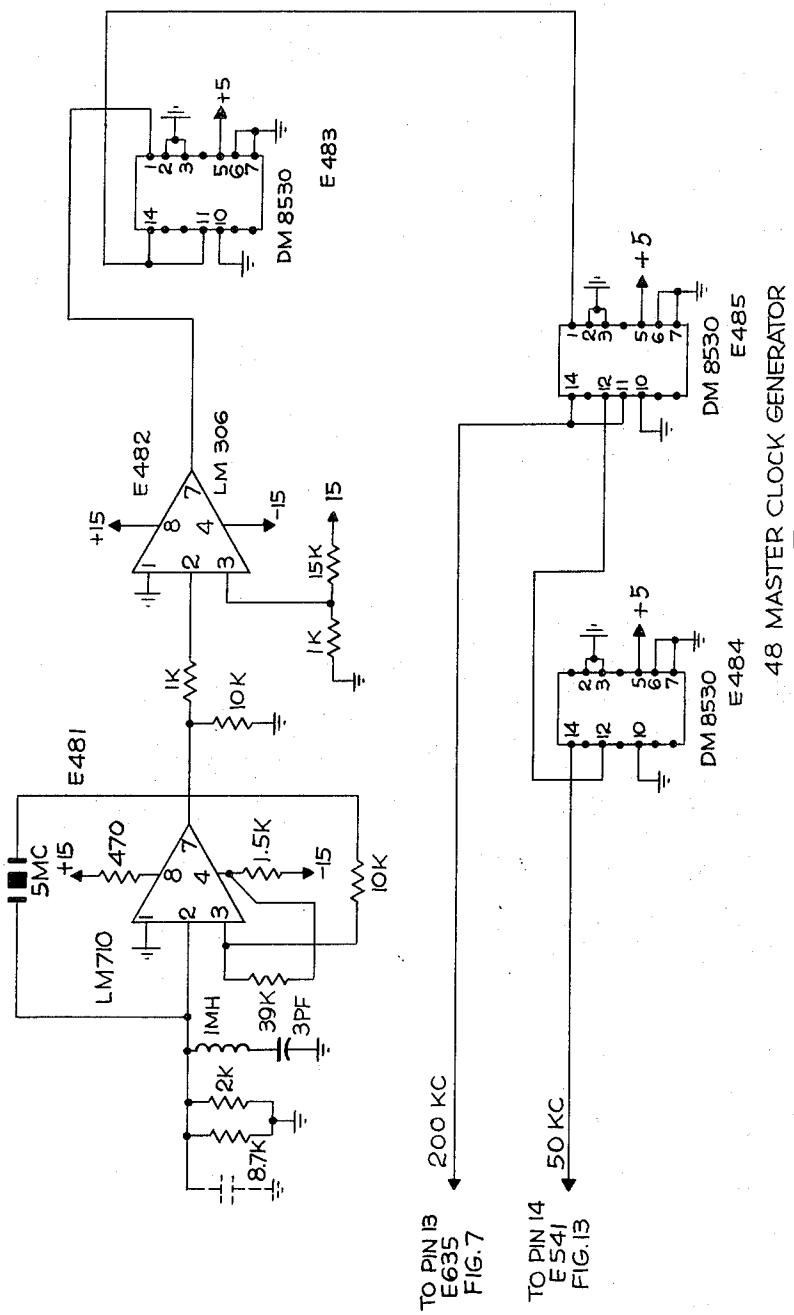


FIG. 12

48 MASTER CLOCK GENERATOR

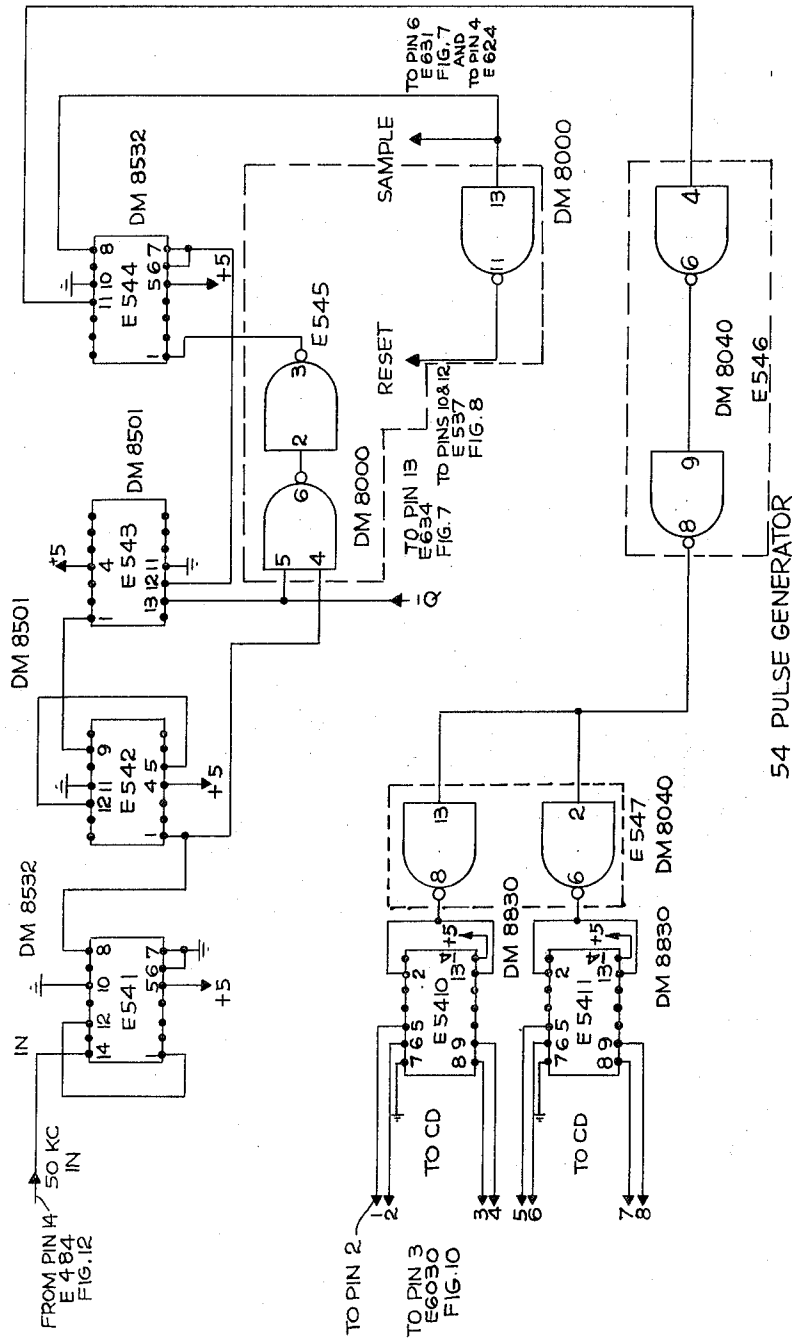
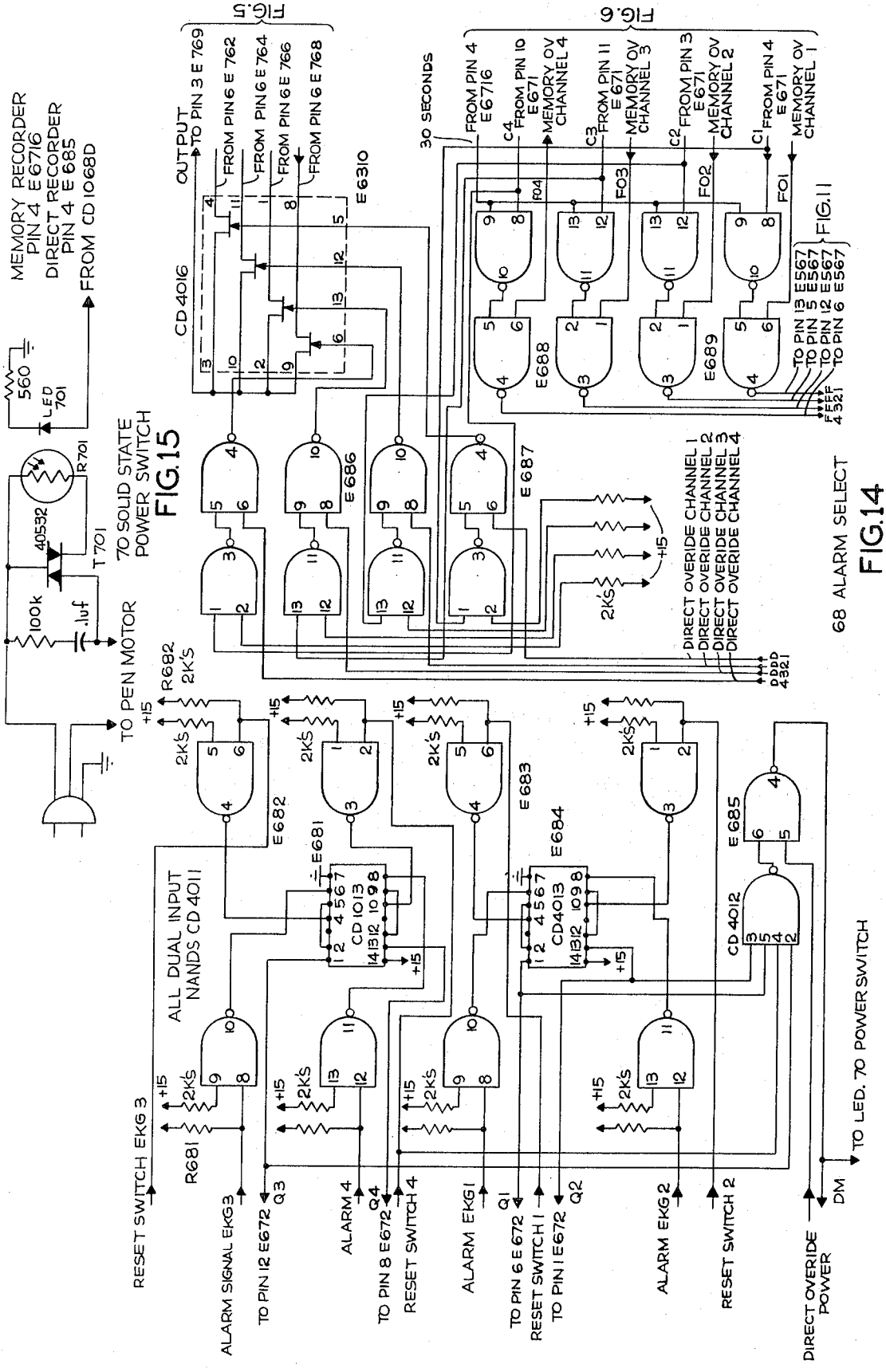

DM 8532
E544
DM 8501
E543
DM 8501
E542
DM 8532
E541
IN
50 KC IN
FROM PIN 14 E484 FIG.12
+5
SAMPLE
RESET
DM 8000
E545
TO PIN 13 E634 FIG.7
TO PINS 10 & 12 E537 FIG.8
TO PIN 6 E631 FIG.7 AND TO PIN 4 E624
DM 8040
E546
54 PULSE GENERATOR
DM 8040
E547
DM 8830
E5410
E5411
TO CD
TO PIN 2
TO PIN 3 E6030 FIG.10

FIG.13


MEMORY RECORDER PIN 4 E 6716
DIRECT RECORDER PIN 4 E 685
FROM CD 1068D
560
LED 701
R701
40532
T701
100k
.1uf
TO PEN MOTOR
TO SOLID STATE POWER SWITCH
FIG.15
FIG.5
FIG.6
CD 4016
OUTPUT
TO PIN 3 E 769
FROM PIN 6 E 762
FROM PIN 6 E 764
FROM PIN 6 E 766
FROM PIN 6 E 768
E 6310
30 SECONDS
FROM PIN 4 E 6716
FROM PIN 10 E 671
MEMORY OV CHANNEL 4
FROM PIN 11 E 671
MEMORY OV CHANNEL 3
FROM PIN 3 E 671
MEMORY OV CHANNEL 2
FROM PIN 4 E 671
MEMORY OV CHANNEL 1
C4
C3
C2
C1
F04
F03
F02
F01
E688
E689
TO PIN 13 E567
TO PIN 5 E567
TO PIN 12 E567
TO PIN 6 E567
FIG.11
E 686
E 687
R682 2K's
DIRECT OVERIDE CHANNEL 1
DIRECT OVERIDE CHANNEL 2
DIRECT OVERIDE CHANNEL 3
DIRECT OVERIDE CHANNEL 4
68 ALARM SELECT
FIG.14
ALL DUAL INPUT NANDS CD 4011
E682
E681
E683
E684
E685
CD 1013
CD4013
CD 4012
R681
RESET SWITCH EKG 3
ALARM SIGNAL EKG3
TO PIN 12 E672 Q3
ALARM 4
TO PIN 8 E672 Q4
RESET SWITCH 4
ALARM EKG1
TO PIN 6 E 672 Q1
RESET SWITCH 1
TO PIN 1 E672 Q2
ALARM EKG2
RESET SWITCH 2
DIRECT OVERIDE POWER
TO LED. 70 POWER SWITCH
DM
+15
2K's

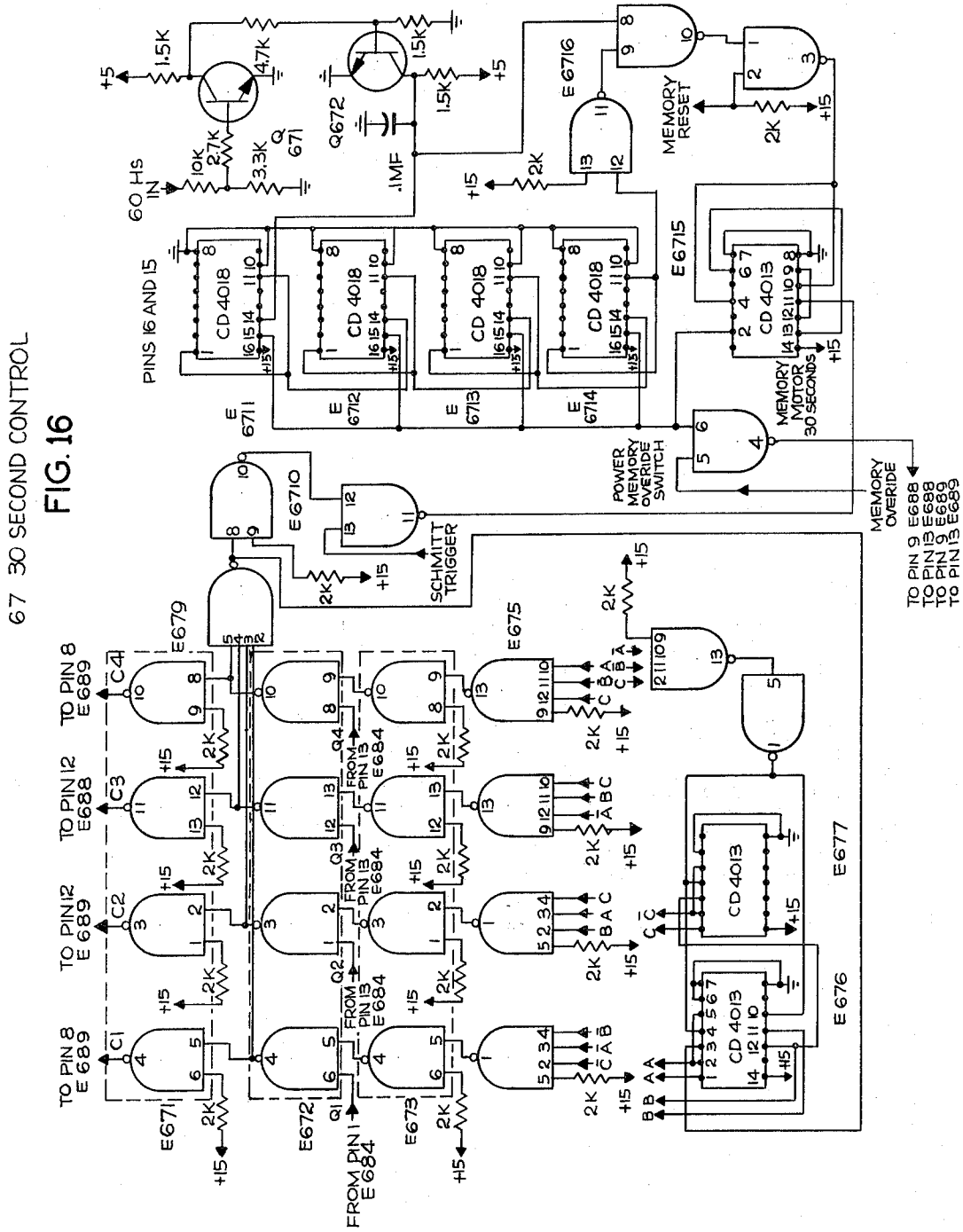
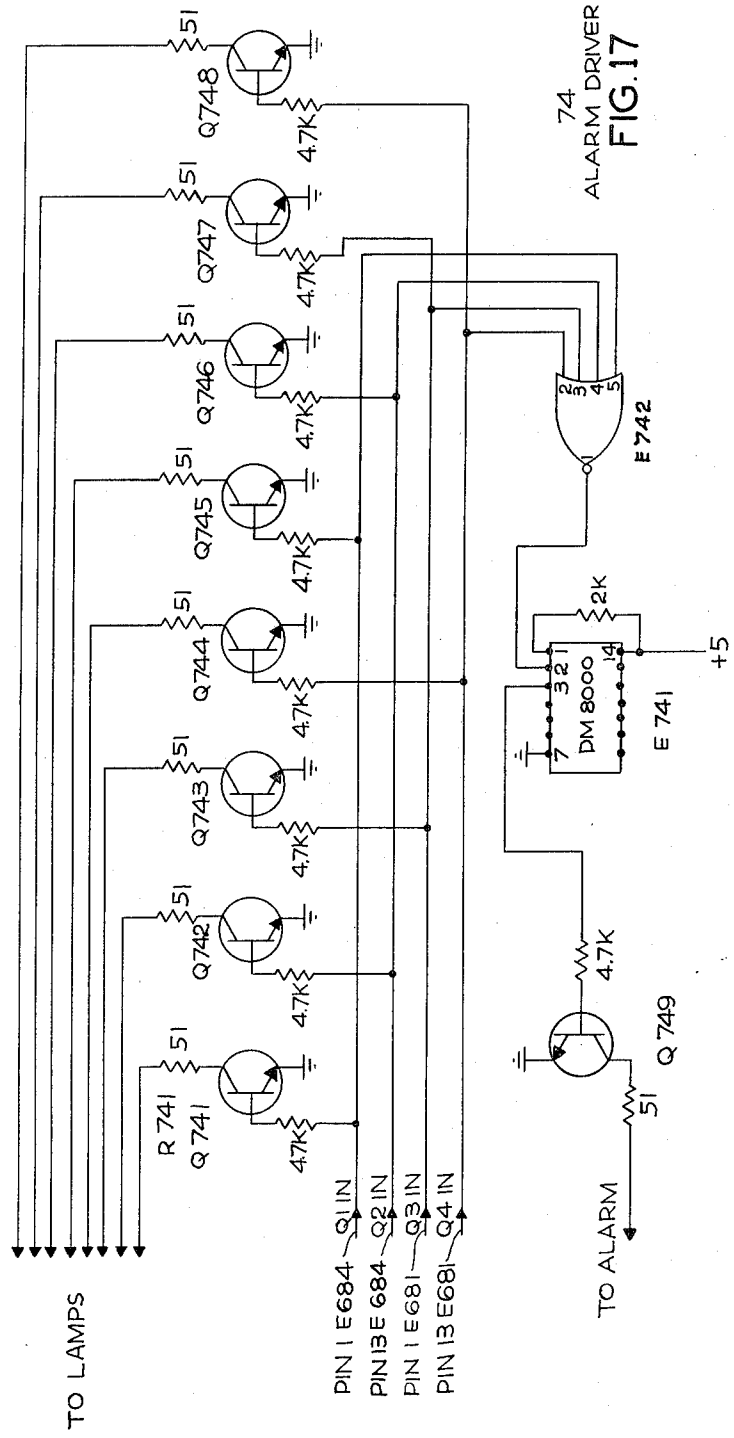
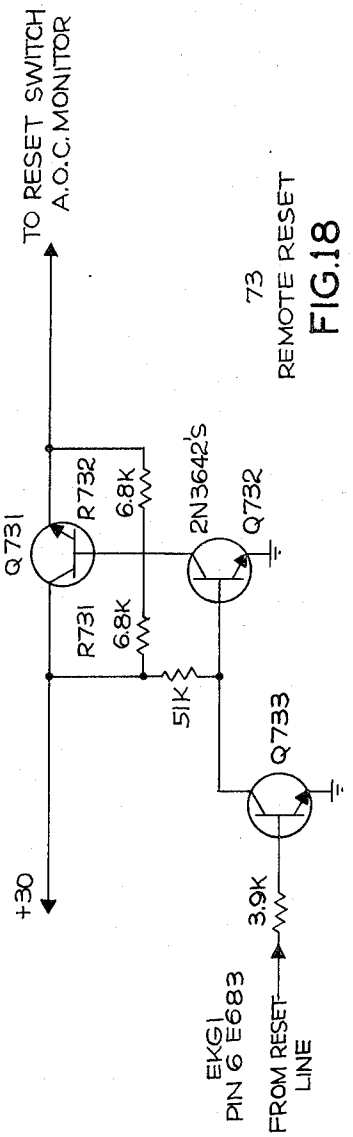

67 30 SECOND CONTROL
60 HS IN
PINS 16 AND 15
CD 4018
CD 4013
Q672
Q671
.1MF
MEMORY RESET
MEMORY MOTOR 30 SECONDS
POWER MEMORY OVERIDE SWITCH
MEMORY OVERIDE
SCHMITT TRIGGER
TO PIN 9 E688
TO PIN 13 E688
TO PIN 9 E689
TO PIN 13 E689
TO PIN 8 E689
TO PIN 12 E688
TO PIN 12 E689
TO PIN 8 E689
FROM PIN 11 E684
FROM PIN 13 E684
E679
E675
E677
E676
E671
E672
E673
E6710
E6711
E6712
E6713
E6714
E6715
E6716

FIG. 16


TO LAMPS
R 741
Q 741
Q742
Q743
Q744
Q745
Q746
Q747
Q748
51
4.7K
PIN 1 E684 Q1 IN
PIN 13 E 684 Q2 IN
PIN 1 E 681 Q3 IN
PIN 13 E681 Q4 IN
74
ALARM DRIVER
FIG.17
E742
DM 8000
E 741
2K
+5
Q 749
4.7K
TO ALARM


TO RESET SWITCH
A.O.C. MONITOR
+30
Q731
R732
6.8K
2N3642'S
Q732
R731
51K
Q733
3.9K
EKG1
PIN 6 E683
FROM RESET
LINE
73
REMOTE RESET
FIG.18

TWO RECORDER APPARATUS FOR MONITORING HEART ACTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to apparatus for monitoring the heart action of coronary patients. In particular, it relates to such apparatus wherein, in the event of apparent heart action arrhythmia, one recorder provides an electrocardiogram representing a patient's current heart action and another recorder, furnished with information from a memory unit, concurrently provides an electrocardiogram representing the patient's heart action for a 30 second interval just prior to onset of the apparent arrhythmia.

2. Description of the Prior Art

Hospitals having intensive care facilities for coronary patients usually employ some type of apparatus for continuously monitoring the heart action of each coronary patient so that remedial action can be taken swiftly in the event a patient's heart action becomes irregular or arrhythmatic.

Some monitoring apparatus comprises an electrocardiograph (hereinafter called an EKG) which includes sensors or electrodes for attachment to the patient's body and provides an electrical signal representative of the wave form of heart action. This signal is supplied to a recorder which provides an electrocardiogram (hereinafter called an ECG), usually in the form of a continuous strip of graph paper on which the wave form of heart action is traced. Since it is impractical to continuously operate and monitor the direct recorder, provision is made to actuate the recorder automatically in the event the EKG gives an indication of apparent heart arrhythmia and also actuate an alarm (audio, visual or both) to alert the person monitoring the apparatus. However, the ECG from the recorder only shows the heart action wave form from the time the recorder was turned on. With this information alone, it is sometimes impossible to conclude from the ECG whether the patient actually experienced heart action arrhythmia requiring immediate medical attention or whether a spurious signal from the EKG caused the direct recorder and alarm to be actuated. Such spurious signals can, for example, result from a sensor becoming detached from the patient or from a damaged sensor lead wire. To avoid this problem, the monitoring apparatus sometimes includes a memory unit which is selectively actuated by attending personnel to provide an ECG of heart action wave form which occurred during a short interval of time prior to the onset of the arrhythmia. By comparison of the two ECG's it is possible to determine with certainty whether an EKG malfunction or a true arrhythmatic condition occurred. In the latter case, more complete diagnostic information about heart action is also provided. The ECG from the memory unit is based on data stored therein and is, in fact, a reconstructed wave form of heart action. Heretofore, the memory unit has taken the form of an electrical tape recorder using a continuous strip or band of magnetic recording tape in which information from the EKG, translated into a signal form suitable for use on magnetic tape, is temporarily stored for a short interval and ready for use if needed to reconstruct an ECG for the memory recorder and then erased. In some prior art systems, the current ECG to the recorder was interrupted briefly by operating personnal so that information from the memory recorder could be preserved in permanent form. While such memory units are generally satisfactory, continuous use of the band of magnetic tape causes the oxide recording material thereon to gradually wear off. This eventually results in a low fidelity signal from the memory unit and a poorly reconstructed ECG and requires frequent tape replacement. In addition, the number of channels of information, i.e., the number of patients being monitored and the number of bits of data, i.e., which determine completeness of wave form reconstruction that can be stored on magnetic recording tape is limited. Furthermore, it was necessary for the operator to take positive action, i.e., operate a selector switch to retrieve information from the memory unit and to forego a portion of the current ECG in order to obtain a permanent record of the ECG from the memory unit. It is desirable, therefore, to provide improved monitoring apparatus of the aforesaid character and, particularly, improved memory units therefor which avoid or overcome the aforedescribed disadvantages and have other advantages.

SUMMARY OF THE INVENTION

Apparatus in accordance with the present invention for monitoring the heart action of one or more coronary patients comprises an electrocardiograph (EKG) for each patient, one direct recorder for providing an electrocardiogram (ECG) of current heart action of any one of the patients experiencing apparent heart arrhythmia, one memory recorder for concurrently providing an ECG of that patient showing heart action for a short interval of time just prior to onset of the apparent arrhythmia, and one solid state memory unit connected to each EKG and to the memory recorder and capable of storing a plurality of channels (one for each EKG) of data for a short interval of time and for releasing the stored data on demand to the memory recorder in a form suitable for reconstruction of heart action wave form by the memory recorder.

Each EKG comprises sensors or electrodes for attachment to a patient and provides an electrical output signal in analog form representative of the wave form of heart action.

The direct recorder continually receives the analog signal from each EKG and is capable of providing an ECG for each patient at any given time. The direct recorder is actuated or turned on automatically to provide an ECG in response to an occurrence of apparent heart arrhythmia in the analog signal from any one of the EKG's.

The apparatus includes an alarm (audio or visual or both) which is actuated simultaneously with the direct recorder to alert the person monitoring the apparatus and to indicate which patient is apparently experiencing arrhythmia.

The solid state memory unit also continually receives the analog signal from each EKG and comprises sampling means for sampling each one in succession at predetermined intervals of time, i.e., at a rate of 130 times per second per patient, to provide a series of sample analog signals. Analog to digital converter means are provided in the memory unit for converting each sample analog signal into a sample digital signal which has a binary numerical value which corresponds to the amplitude of the sample analog signal on which it is based.

Memory or storage means are provided in the memory unit for storing each sample digital signal for a predetermined interval of time, i.e, on the order of 30 seconds. Digital to analog converter means are provided in the memory unit to recover each sample digital signal from the storage means at the rate of 130 times per second per patient and to convert each series of sample digital signals into a reconstructed analog signal representing prior output from an EKG.

Each reconstructed analog signal is available on demand from the memory unit for use by the memory recorder to provide a reconstructed ECG for any one of the EKG's. Occurrence of an apparent heart arrhythmia in the analog signal from any one of the EKG's causes the memory recorder to be actuated automatically concurrently with the direct recorder and to display the reconstructed ECG for that patient apparently experiencing arrhythmia.

In practice, the memory recorder remains in operation for only thirty seconds, i.e., the length of the memory of the memory unit, but the direct recorder remains in operation until it is turned off and the monitoring apparatus is reset by the person operating the monitor.

In practice, the monitoring apparatus can be operated in the automatic mode, as described above, or the direct recorder can be selectively actuated by the operator (direct override mode) or the memory recorder can be selectively actuated by the operator (memory override mode).

DRAWINGS

FIG. 1 is a schematic diagram of apparatus in accordance with the invention for monitoring heart action;

FIG. 2 is a graph showing a typical heart action wave form;

FIG. 3 is a schematic view showing ECG's from the memory recorder and the direct recorder;

FIG. 4 is a wiring diagram of the power supply for the apparatus shown in FIG. 1;

FIG. 5 is a wiring diagram of the input buffer circuit;

FIG. 6 is a wiring diagram of the circular counter;

FIG. 7 is a wiring diagram of the level detector;

FIG. 8 is a wiring diagram of the analog to digital converter;

FIG. 9 is a wiring diagram of the digital to analog converter;

FIG. 10 is a wiring diagram of one of eight identical memory circuits;

FIG. 11 is a wiring diagram of the output selector circuit;

FIG. 12 is a wiring diagram of the master clock generator;

FIG. 13 is a wiring diagram of the pulse generator;

FIG. 14 is a wiring diagram of the alarm select circuit;

FIG. 15 is a wiring diagram of one of two identical solid state power switches;

FIG. 16 is a wiring diagram of the 30 second control circuit;

FIG. 17 is a wiring diagram of the alarm driver circuit; and

FIG. 18 is a wiring diagram of the remote reset circuit.

DESCRIPTION OF A PREFERRED EMBODIMENT

Apparatus in accordance with the present invention is used in an intensive care facility in a hospital to monitor the heart action of one or more coronary patients, i.e., four in the embodiment shown. As FIG. 1 shows, the monitoring apparatus comprises four electrocardiographs EKG1, EKG2, EKG3, and EKG 4 which are normally located in the patients' rooms. Each electrocardiograph (hereinafter referred to as an EKG) is understood to comprise sensors or electrodes for attachment to a patient and each EKG provides a continuous electrical output signal in analog form representative of the wave form of heart action. Each EKG is further adapted to monitor the amplitude of all portions of the wave form of heart action and to provide a control signal (usable to actuate a hi-low alarm or other equipment) in the event any portion of the wave form falls beyond predetermined upper and lower limits. In an actual embodiment of the invention each EKG was a Model 10915 manufactured by the American Optical Company.

FIG. 2 shows that the typical wave form of a single normal heart beat comprises pulse designated P, Q, R, S, and T and each pulse has an amplitude which normally falls within a certain normal range. In heart action arrhythmia, the amplitude of one or more of the pulses P, Q, R, S, and T exceeds the normal range. The sensors of an EKG sense normal heart action wave form and also arrhythmia.

The monitoring apparatus shown in FIG. 1 also comprises one direct recorder 12 for viewing the analog signal from each of the four EKG's and for providing an electrocardiogram (hereinafter referred to as an ECG) showing the current heart action of any one of the four patients. As FIG. 3 shows, ECG1 from direct recorder 12 takes the form of a strip of graph paper on which a motor driven pen (not shown) traces the wave form of heart action. Direct recorder 12 can be selectively actuated by the operator of the apparatus (direct override mode) or can be actuated automatically (automatic mode) as hereinafter described.

The monitoring apparatus shown in FIG. 1 also comprises one memory recorder 14 for receiving signals from a memory unit 16, hereinafter described, to provide an electrocardiogram ECG2 showing the heart action of any one of the four patients for a short interval of time, i.e., 30 seconds, prior to the time memory recorder 14 is actuated. FIG. 3 shows the ECG2 from memory recorder 14 is also a strip of graph paper on which a motor driven pen (not shown) traces heart action wave form. Memory recorder 14 can be selectively actuated by the operator of the apparatus (memory override mode) or can be actuated automatically (automatic mode) as hereinafter described.

In automatic mode, direct recorder 12 and memory recorder 14 are actuated automatically and simultaneously in the event any one of the four EKG's gives an indication that any one of the four patients apparently is experiencing arrhythmia. Recorder 14 operates for only 30 seconds (the length of time memory unit 16 provides a signal) but recorder 12 continues to operate until turned off by the operator.

In the event any one of the four EKG's indicates arrhythmia, an audio alarm 18 sounds to alert the operator and the appropriate one of four visual alarms 19,

20, 21 and 22 indicates which patient requires attention. If preferred, remote alarm means 23 may be utilized and located as desired.

In an actual embodiment of the invention, the recorders 12 and 14 were type TMD-25 recorders manufactured by Techni-Rite, Inc. of Warwick, Rhode Island.

Generally considered, solid state memory unit 16 continually receives at input buffer circuit 76 the analog signal from each EKG and comprises sampling means (circuit 62) for sampling each signal in succession at predetermined intervals of time, i.e., at a rate of one hundred and thirty times per second per EKG signal (520 total bits per second) to provide a series of sample analog signals. Analog to digital converter means (circuit 53) are provided in memory unit 16 for converting each sample analog signal into a sample digital signal which has a binary numerical value which is related to or corresponds to the amplitude of the sample analog signal on which it is based. Memory or storage means (the eight circuits 60) are provided in the memory unit for storing each sample digital signals for a predetermined interval of time, i.e., on the order of 30 seconds. Digital to analog converter means (circuit 53 MOD) are provided in memory unit 16 to recover each sample digital signal from the storage means at the rate of one hundred and thirty times per second per EKG and to convert each series of sample digital signals into a reconstructed analog signal representing prior output from an EKG.

Each reconstructed analog signal is available on demand from memory unit 16 for use by memory recorder 14 to provide a reconstructed ECG for any one of the EKG's. Occurrence of an apparent heart arrhythmia in the analog signal from any one of the EKG's causes the memory recorder to be actuated concurrently with direct recorder 12 and to display the reconstructed ECG for the patient apparently experiencing arrhythmia.

FIG. 1 shows a schematic or block diagram of the circuitry of memory unit 16 which, for convenience in understanding, is divided into four functional segments (defined by dotted lines and designated A, B, C and D) and each segment comprises a plurality of circuits shown as boxes having a designation number and an appropriate legend. Each circuit shown in FIG. 1 is also shown in more detail in another figure of the drawings. Each such circuit comprises integrated circuit devices (hereinafter called ICs), transistors, outboard components such as resistors and capacitors, or some combination of these components, and necessary wiring. In the drawings, the IC's and transistors bear a model number which is the standard industrial designation number therefor and indicates the nature and function of the component. These and other components also bear a designation number. Note that the first two prefix numbers in each designation number correspond to the identification number of the circuit in which they are used. Each outboard component (resistor or capacitor) referred to in the specification is identified by its electrical value or a designation number.

Referring to FIG. 1, memory unit 16 comprises segments and circuits generally described as follows.

Segment A relates to the flow of the four EKG signals within unit 16 itself and comprises the following circuits:

76 Input Buffer (FIG. 5)
62 Circular Counter (FIG. 6)
63 Level Detector (FIG. 7)
53 Analog to Digital Converter (FIG. 8)
53 MOD Digital to Analog Converter (FIG. 9)
60 Memory Circuits (FIG. 10)
56 Output Selector (FIG. 11)

Segment B relates to the memory timing pulses and comprises the following circuits:

48 Master Clock Generator (FIG. 12)
54 Pulse Generator (FIG. 13)

Segment C relates to the alarm and recorder circuitry as well as all analog signal routing and comprises the following circuits:

68 Alarm Select (FIG. 14)
67 30 Second Control (FIG. 16)
74 Alarm Driver (FIG. 17)
73 Remote Reset (FIG. 18)
70 Solid State Power Switch (FIG. 15)

Segment D relates to the power supplies for the entire unit and comprises the following circuits:

Circuit 77 providing −12 volts and +5 volts (FIG. 4)

Circuit 64 providing +15 volts and −15 volts (FIG. 4)

Circuit 35 providing +5 volts (FIG. 4)

DESCRIPTION OF SEGMENT D

Referring to FIGS. 1 and 4, the circuits 35, 77 and 64 are supplied with electric power from a conventional 115 volt a.c. source and provide regulated d.c. operating power at various voltage levels for memory unit 16 and other components of the monitoring apparatus.

Circuit 35 is a +5 volt d.c. supply. In its positive supply, resistor R641 and R642 are chosen to operate IC E 641 which controls the base voltage of series pass transistor Q641. In its negative supply, resistor R643 and R644 operate IC E642 which controls the base of transistor Q642.

Circuit 77 is a +5, −12 d.c. supply. It supplies voltage for the memory circuits 60 and each of its two outputs is supplied from a separate specially designed isolation transformer which minimizes leakage.

Other Figures in the drawings clearly indicate, by designations such as +5, −12, +15, −15, points at which power is supplied to a portion of a circuit.

DESCRIPTION OF SEGMENT A

Referring to FIG. 1, 5 and 6, circuit 76 is the means by which analog signals from each of the four EKG's enter memory unit 16 and also serves to route any one of the four signals to direct recorder 12. In circuit 76, IC E761 is a voltage follower to provide a high input impedance which matches the output impedance of each of the AOC Model 10715. EKG's, which output impedance is greater than 1 megohm. In circuit 76, IC E762 is a non-inverting amplifier with a variable DC offset which allows it to place the EKG on a three volt plateau. Circuit 76, therefore, will accept plus and minus 3 volt input voltages. This allows memory unit 16 to utilize a voltage level when a particular EKG channel is not in use. This approach has the advantage that memory unit 16 can be operated to monitor anywhere from one to four EKG's without the need to make special adjustments if less than four EKG's are in operation. More specifically, a number (which is half of 256 or 128) is automatically assigned for each EKG not in use and this number is operated upon by memory unit

16. In circuit 76, IC E769 removes the three volt plateau when a particular EKG has been routed to the direct recorder 12. The four outputs from the IC's E762, E764, E766, and E768 are set to circular counter circuit 62, shown in FIG. 6 and to alarm selector circuit 68. E769, although part of circuit 76, is completely disassociated from the input buffer. The buffering portion of the circuit 76 is done by E761, E763, E765, E767, E762, E764, and E768 and the three voltage level sets each having individual EKG channels.

Referring to FIGS. 1 and 6, circular counter circuit 62 receives four incoming analog signals, one from each of the four EKG's (and buffered by circuit 76), and utilizes them in IC E621 which is a four channel analog field effect transistor (FET) switch with a common output drain. A sample (5 volt) pulse from pulse generator circuit 54 (FIGS. 1 and 13) is fed to IC E624 in circuit 62 which converts the five volt pulse to a fifteen volt negative pulse and feeds it to drive IC E623 in circuit 62. IC E623 is wired as a divide-by-four counter. Each of the four outputs of IC E623 is fed to a gate of the four channel FET analog switch IC E621. In circuit 62, IC E622 is a voltage translator which enables IC E623 to rive TTL (Transistor Transistor Logic) circuitry. IC E623 is a type of device (commercially known as an RCA COS/MOS Type) which consumes very little power and is, therefore, unable to supply current to drive any other types of device other than those of the COS/MOS or family type. The output of IC E621 as in the form of successive portions or sample of the analog signal of each of the four EKG's.

Referring to FIGS. 1 and 7, there is shown the level detector circuit 63. The output signal of IC E621 in circular counter circuit 62 and a sample pulse are fed to IC E631 in level detector circuit 63, which is a sample and hold circuit. Its output is fed to IC E633, which is a voltage comparator, at the non-inverting input. IC E633 serves as a voltage reference for a voltage which will be generated in AD converter circuit 53, shown in FIG. 8. IC E632 receives the voltage generated in AD converter circuit 53 and inverts this voltage. This provides a stairstep generator from zero which can be compared to the output signal of input sample and hold IC E631. IC E633 (in FIG. 7) and E635 comprise an OR gate which controls the number of 200 KC pulses from master clock generator circuit 48 to be directed into AD converter circuit 53. The OR function consists of the state of the Q pulse (shown at point Q in FIG. 7) from pulse generator circuit 54 or the state of the output of the comparator IC E633 in circuit 63. When NOT Q is at the one state, it will not allow any pulses into AD converter circuit 53. This is important because at this time pulses are being produced to advance the memory shift registers to provide the AD converter circuit 53 with a reset pulse and IC E631 with a sample pulse. When Q pulse returns to zero, it AND's with the zero state of comparator IC E633 in circuit 63. Therefore, the output of IC E634 provides IC E635 with a one state and gates AD converter circuit 53 with 200 KC pulses. IC E634 is used to provide a turn-on or turn-off signal for the reference counter, depending upon whether the signal Q or $\overline{Q}$ originates first.

The output of IC E635 is determined either by the amplitude of the output of IC E631 or the pulse width of Q.

Referring to FIGS. 1 and 8, there is shown AD converter circuit 53. The pulse train output of IC E635 is fed into an eight stage binary counter via IC E537. IC E537 accepts the input and reset TTL levels and converts these levels to a plus fifteen volt level to drive binary counters E535 and E536. These are COS/MOS type binary counters which were selected because their output stairstep is superior in linearity. IC's E534 and E533 are voltage translators for the binary counters, IC E535 and IC E536. The output of circuit 53 drives both IC E571 in DA converter circuit 53 MOD (FIG. 9) and the eight memory circuits 60 (FIGS. 1 and 10). The output of IC E531 in circuit 53 (FIG. 8) is a stairstep generator which operates from the minus 6 volt reference towards zero and the positive travel thereof is determined by the binary input. IC E532 in circuit 53 is an operational amplifier which isolates IC E531 and establishes the amplitude of the steps. The output of IC E532 is referred to as the reference RAMP and is fed to the input of IC E632 in level detector circuit 63 (FIG. 7). IC's Q531 and Q532 supply minus and plus 6 volt operating voltages for IC E531.

Referring to FIGS. 1 and 10, it is seen that there are eight identical memory circuits 60 in unit 16. Each circuit 60 stores one of the eight binary bits, and provides 29 seconds of delay or memory. In circuit 60 (FIG. 10), IC E6031 is an AND gate used as an inverter to isolate the memory from the counter. There are 29 National MM5016 devices provided in each circuit board 60 to serve as dynamic shift registers containing 500 bits of delay. IC E6030 is a clocked driver which feeds the 29 shift registers MM5016 with phase-in and phase-out pulses or "steering" pulses, which accept and transfer the binary number. Capacitor C6002 and C6003 and resistor R6002 and R6003 serve as RF filters in series with the 12 volt power supply lines for each circuit 60. Capacitors C6001 and C6004, in series with the inputs to the clock lines, determine the clock driver output pulse width. The output of each memory circuit 60 is fed to DA converter circuit 53 MOD (FIG. 9).

Referring to DA converter circuit 53 MOD shown in FIGS. 1 and 9, it is to be understood that the operation of DA converter circuit 53 MOD is similar to AD converter circuit 53 (FIG. 8). In circuit 53 MOD, IC E571 accepts the eight "bits" of binary information from the memory circuit 60 and presents, for example, an analog voltage at the output of IC E572. The voltage at this output point is fed to output selector circuit 56 (FIG. 11).

Referring to FIGS. 1 and 11, the output selector circuit 56 selects the analog d.c. levels from DA converter circuit 53 MOD and reconstructs them into their original EKG waveform. Circuit 56 then presents the information to memory recorder 14, if instructed to do so by alarm selector circuit 68 (FIGS. 1 and 14) via the four channel FET switch IC E567 in circuit 56 (FIG. 11). The output of DA converter circuit 53 MOD feeds four identical sample and hold circuits. One such circuits, for example, comprises transistor Q561, transistor Q562, IC E561 shown in circuit 56 (FIG. 11), which reconstruct the wave form for the channel 2, i.e., EKG 2. Pulse CC 2 in circuit 56 and received from circuit 62, the circular counter, is gated with a sample pulse to provide accurate timing to gate the proper d.c. level from DA converter circuit 53 MOD (FIG. 9) into the appropriate sample hold at the appropriate time. Transistor Q561 closes FET transistor switch Q562 and allows capacitor C561 to charge to the proper voltage level. IC E561 isolates charging capacitor C561 from

the output switch. When IC E567 of circuit 56 (FIG. 11) is directed to present an output or reconstructed ECG, stage IC E568 removes the three volt "plateau" and IC's E569 and E570 together form an amplifier with a gain of 5 from d.c. to 100 cycles. This stage removes the "steps" created by the AD-DA conversion. The output of IC E570 is fed directly to the input of memory recorder 14.

SEGMENT B

Referring to FIGS. 1 and 12, circuit 48 is a master clock generator. In circuit 48 IC E481 is the master clock oscillator. Positive feedback is provided from the output of IC E481 via the series resonant impedance of a crystal 5 MC to the non-inverting input of IC amplifier E481. The d.c. operating level thereof is biased, so that the oscillations take place in the linear region of the output dynamic range, thereby ensuring self-starting under all conditions. IC E482 buffers the oscillator and drives IC E483, which is a divide-by-five counter. The 1 megacycle output of IC E483 is fed to IC E485, which divides by 5 and again by 2. The signal from the divide-by-5 section of IC E485 is fed to level detector circuit 63 (FIG. 7) at a frequency of 200 KC. The second segment of IC E485 sends a 100 KC signal to IC E484. IC E484 divide by 2 and sends a 50 KC signal to IC E541 in pulse generator circuit 54 (FIG. 13).

Referring to FIGS. 1 and 13, pulse generator circuit 54 generates all the control signals which manipulate data in the memory portion of unit 16. In circuit 54, IC E541 receives a 50 KC signal from master clock generator circuit 48 (FIG. 12) and divides this by twelve. The output of IC E541 is fed to a divide-by-four stage IC E542 and to the IC's in circuit E545. IC E543 receives the output of IC E542 and produces a Q signal (see FIG. 13) and a NOT Q condition. Referring back to the previous circuit description of level detector circuit 63 (FIG. 7), it was stated that when NOT Q was in the one state the input to the binary counter was disabled. Therefore, referring to FIG. 13, when Q is in the one state, the output of IC E541 is gated with Q and inverted in stage E545 which comprises two IC's. The output of E545 is in the form of four symmetrical pulses fed to IC E544. IC E544 is a divide-by-6 counter enabled by the opposite state of Q on its reset line (terminal 11 of DM8000). This ensures that the following stages receive no input pulses during that time when the analog input voltage is being analyzed. There are two output pulses from IC E544. The first pulse if inverted twice by the two IC's in stage E546 to isolate IC E544. The output of stage E546 is fed to IC's in stage E547, and from there to the IC's E5410 and E5411. These stages produce the phase and drive pulse for the clock drivers located in the memory circuit 60. The second output of IC E544, which corresponds to its fourth input, produces the sample pulse which is fed to circular counter circuit 62 (FIG. 6), level detector circuit 63 (FIG. 7) and output selector circuit 56 (FIG. 11). The output at this point is also inverted to produce the binary counter reset pulse.

SEGMENT C

Referring to FIGS. 1 and 14, alarm select circuit 68 operates the four output analog transistors Q562, Q564, Q566 and Q568 (in circuit 56 in FIG. 11) and the power circuits to the recorders 12 and 14 (shown in FIG. 1) in all modes of operation. In circuit 68 FIG. 14, four IC E682 devices (each a dual input nand gate) and IC E481 (a dual R S flip flop device) are now described to illustrate how all the alarms on the four remote alarms operate. For example, assume that the alarm for EKG3 shown in FIG. 1 has been actuated. Initially, the output of IC E681 (circuit 68 in FIG. 14) is at zero, and its R S inputs are at zero. As pin 8 of the input nand A3 of IC E682 is grounded, R3 goes to the one state requiring Q3 to go to the one state. Q3 is fed to 30 second control circuit 67 (FIG. 16) to turn on the power to memory recorder 14 (FIG. 1). It must be noted that there are two inputs to the recorders 12 and 14, a signal input and a power input. Q3 also is fed to a four input nand gate CD4012 (in circuit 68 in FIG. 14) serving as an OR gate. The output of CD 4012 feeds terminal 6 of IC E685. IC E685 is a dual input nand gate the terminal 4 of which operates the a.c. power (DM) in direct recorder 12. The other input terminal 5 of IC E685 is connected to the +15 volt power supply through a resistor and the direct override switch (DO). If either input to IC E685 is grounded by the actuation of the DO switch or by Q3 turning on, the a.c. power to the recorder is turned on. Q3, when fed to thirty second control circuit 67 (FIG. 16), causes return of a corresponding pulse designated C3 (see IC E671 in circuit 67). It also causes return of the thirty second pulse which is being simultaneously fed to the a.c. power control of memory ecorder 14 shown in FIG. 16. Signal C3 is fed to IC E688 (see FIG. 14) along with the 30 second pulse to be gated, and the output of this nand gate is ORed with the signal section of the memory override switch. When either pin 4 or 5 of IC E688 is grounded, control pulse F3 (see FIG. 14 and 11) will be sent to output selector circuit 56 (FIG. 11) and allow the proper gate on the output FET to send the analog information to memory recorder 14. IC E687 in FIG. 14 operates in a similar manner with signal C3 and the signal section of the direct override switch. Signal C3 is inverted and ORed with D3 (see FIG. 14), the direct override switch. If either pin 5 or pin 6 of IC E687 in FIG. 14 is grounded, the wave form signal for EKG3 would be sent to direct recorder 12 through the FET switch E681 shown in FIG. 14, and circuit 76 (FIG. 6). Signal Q3 is also sent to alarm driver circuit 75 (FIG. 17) to initiate an audio and visual alarm.

Referring to FIGS. 1 and 16, 30 second control circuit 67 continually monitors each of the four EKG's for an alarm condition, i.e., departure of heart wave form amplitude from within predetermined limits. If an alarm occurs at one EKG, it is necessary to isolate that EKG in order to eliminate false signals from interfering if alarms also occur at other EKG's. This is accomplished by using circular counter IC E676 and IC E677. The input thereto is from a 60 cycle square wave generator comprising transistor Q672 and Q671 shown in FIG. 16. The square wave generator is gated into the circular counter by IC E6710. If signal Q3 in circuit 68 (FIG. 14) goes to the one state, signal Q3 is ANDed at pins 12 and 13 of IC E671 in FIG. 16 which sends signal C3 back to alarm circuit 68 in FIG. 14 and, via IC E679 (FIG. 16), disables the input to the circular counter (IC's E676 and E677). IC E6715 in FIG. 16 is a dual RS flip flop device which controls the reset lines in 30 second control circuit 67 (FIG. 16), namely, IC's E6711 through E6714. The position transition at pin 1

of IC E679 sends the Q state of IC E6715 to ground. Pins 5 and 6 of IC E6710 form an OR gate for the thirty second control pulse. Either a ground caused by the positive transition of IC E679 or a ground from the memory override switch will initiate a 30 second control pulse. As pin 2 of IC E6715 is grounded, the output of the Schmitt trigger (see FIG. 16) is fed to the data input line of the 30 second timer state. This disables the output of IC E6716. When the timer interval is completed, the output of IC E6714 will fall to ground enabling IC E6715 to pass the 60 cycle generator output. The output of IC E6716 resets both sides of the flip-flops and the cycle is completed. Another cycle will not occur to drive the audio and visual alarms will a Q3 signal of alarm select circuit 68 is reset.

Referring to FIGS. 1 and 17, the purpose of the alarm driver circuit 74 is, in the event of a Q state, to drive the appropriate front panel alarm lamp, remote alarms 23 and audio alarm 18. All transistors Q741 through Q748 in circuit 74 are wired as lamp drivers. IC E742 is a four input nor which operates audio alarm 18 through transistor Q749 when any one of the four EKG alarm conditions are exceeded.

FIG. 15 shows one of two solid state power switches which utilize a light emitting diode LED 701 and a photocell R701 in the gate circuit of a Triac T701 to turn the a.c. power on and off to both recorders 12 and 14.

FIG. 18 shows a remote reset circuit 73 which is located in the bedside EKG unit itself. When an alarm occurs a high or low alarm relay is operated by means of an SCR (not shown). Circuit 73 opens the circuit to the SCR allowing it to reset itself. The positive potential in the reset switch of unit 16 when not in the reset mode biases transistor Q731 to the "on" state. The transistors Q732 and Q733 control the on-off state of Q731.

RESUME

Although the invention is disclosed herein as embodied in apparatus for monitoring heart conditions, it is apparent that it could be embodied in apparatus for monitoring other kinds of activities (such as industrial processes) which involve a wave form in analog form and wherein, upon occurrence of a departure from a normal wave form on one or more channels, it is desirable to have access to a permanent record showing wave form conditions immediately before and after the departure.

Apparatus for monitoring four channels of information presented in analog wave form, such as from four electrocardiograph devices, includes a direct recorder and a memory recorder which are actuated simultaneously when the amplitude of any portion of the wave form from any one channel departs from predetermined limits. The direct recorder presents a record or electrocardiogram of conditions during a short interval (30 seconds) just prior to actuation of the recorder. The memory recorder record is based on a wave form reconstructed from information stored in a memory unit and received from the four electrocardiograph devices. In the memory unit, and analog wave from each device is sampled, the sample analog is converted to a digital signal and assigned a binary number corresponding to amplitude, the digital signal is stored for 30 seconds and then reconverted to an analog signal, and a series (one for each channel) of reconverted analog signals are reconstructed into an analog wave form ready for use by the memory recorder, if required.

I claim:

1. Apparatus for monitoring at least one activity which can be represented in wave form and wherein portions of said wave form have a normal amplitude but exhibit departure therefrom upon occurrence of some event, said apparatus comprising:

detecting means for continuously detecting said activity and for continuously providing a signal in the form of a wave corresponding to the wave form of said activity,

first means for receiving, recording and visually displaying said signal,

memory means for continuously receiving and storing said signal in the form of a stored signal for a predetermined length of time,

converter means for receiving said stored signal from said memory means and for continuously converting it into a reconstructed signal in the form of a wave,

second means for receiving, recording and visually displaying said reconstructed signal concurrently with the disply of another signal by said first means,

and means for actuating said first means and said second means simultaneously with each other to cause them to display their signals upon the occurrence of said event.

2. Apparatus according to claim 1 wherein said activity being monitored can be represented in analog wave form and wherein said first and second means record and display their respective signals in analog wave form.

3. Apparatus for monitoring at least one activity which can be represented in analog wave form and wherein portions of said wave form have a normal amplitude but exhibit departure therefrom upon occurrence of some event, said apparatus comprising:

detecting means for continuously detecting said activity and for continuously providing a signal in the form of an analog wave corresponding to the wqve form of said activity,

first means for receiving, recording and visually displaying said signal in analog wave form,

sampling means for receiving an analog wave form signal from said detecting means and for sampling said analog wave form signal at predetermined intervals of time and for providing a series of sample analog signals,

analog to digital converting means for receiving and converting said sample analog signals into sample digital signals,

memory means for continuously receiving and storing said sample digital signals in the form of stored signals for a predetermined length of time,

converter means including digital to analog converter means for receiving said sample digital signals from said memory means and for continuously converting them into a reconstructed signal in the form of an analog wave,

second means for receiving, recording and visually displaying said reconstructed analog wave signal concurrently with the display of another analog wave signal by said first means,

and means for actuating said first means and said second means simultaneously with ach other to cause

them to display their signals upon the occurrence of said event.

4. Apparatus according to claim 3 wherein said event which effects actuation of said first and second means is a predetermined change in amplitude in a portion of the wave form of the activity being monitored.

5. Apparatus according to claim 4 including a plurality of said detecting means responsive to said detecting means for monitoring a plurality of activities simultaneously, each of said detecting means providing a signal representative of the activity which it is monitoring;

wherein said sampling means successively samples each of said analog signals from said plurality of detecting means;

and wherein said memory means stores sample analog signals in successive order.

6. Apparatus for monitoring at least one activity which can be represented in analog wave form and wherein portions of said wave form have a normal amplitude but exhibit departure therefrom upon occurrence of some event, said apparatus comprising:

detecting means for detecting said activity and for providing an analog signal in the form of a continuous wave corresponding thereto,

first recorder means for receiving, recording and visually displaying said analog signal,

sampling means for receiving and sampling said analog signal from said detecting means at predetermined intervals of time and for providing a series of sample analog signals,

analog to digital converter means for receiving and converting said sample analog signals into sample digital signals,

each digital signal having a binary numerical value related to the amplitude of the sample analog signal on which it is based,

memory means for receiving and storing said digital signals for a predetermined length of time,

digital to analog converter means for receiving said digital signals from said memory means and for converting them into a reconstructed analog signal,

second recorder means for receiving, recording and visually displaying said reconstructed analog signal concurrently with the display of an analog signal by said first recorder means, and means for actuating said first and second recorders means simultaneously when said event occurs.

7. Apparatus for simultaneously monitoring a plurality of activities, each of which can be represented in analog wave form and wherein portions of said wave form have a normal amplitude but exhibit departure therefrom upon occurrence of some event, said apparatus comprising:

a plurality of detecting means for detecting said activities, and for providing analog signals in the form of continuous waves corresponding thereto,

each detecting means monitoring one activity and providing one analog signal,

first recorder means for receiving, recording and visually displaying said analog signals,

said first recorder means comprising means to display one analog signal from one detecting means at any given time,

sampling means for continuously receiving and sampling said analog signals from said plurality of detecting means and for providing a series of sample analog signals,

said sampling means sampling each of the plurality of analog signals at successive predetermined intervals of time,

analog to to digital converter means for receiving and converting said sample analog signals into sample digital signals,

each digital signal having a binary numerical value related to the amplitude of the sample analog signal on which it is based,

memory means for receiving and storing said digital signals for a predetermined length of time,

said memory means comprising a plurality of stages and including means whereby said digital signals being stored are moved from one stage to another,

digital to analog converter means for receiving said digital signals from said memory means and for converting them into a series of reconstructed analog signals,

and second recorder means for receiving, recording and visually displaying said reconstructed analog signals concurrently with the display of analog signals by said first recorder means,

said second recorder means comprising means to display at any given time only one reconstructed analog signal originating from one of said plurality of detecting means.

8. Apparatus according to claim 7 including means responsive to said detecting means for actuating said first and second recorder means simultaneously when said event occurs.

9. Apparatus according to claim 8 wherein said activity being monitored is heart activity and wherein said event is heart arrhythmia.

10. Apparatus according to claim 9 wherein said detecting means is an electrocardiograph,

and wherein said first and second recorder means provide electrocardiograms.

11. Apparatus according to claim 8 wherein said first and second recorder means are actuated by that one of said detecting means which senses a departure from normal amplitude in the wave form of the activity it monitors.

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