(12) UK Patent Application (19) GB (11) 2 250 361 (13) A

(43) Date of A publication 03.06.1992

(21) Application No 9124027.5

(22) Date of filing 12.11.1991

(30) Priority data
(31) 02308170 (32) 13.11.1990 (33) JP

(71) Applicant
Mitsubishi Denki Kabushiki Kaisha

(Incorporated in Japan)

No 2-3 Marunouchi 2-chome, Chiyoda-ku, Tokyo, Japan

(72) Inventor
Yoshikado Sanemitsu

(74) Agent and/or Address for Service
Marks & Clerk
57-60 Lincoln's Inn Fields, London, WC2A 3LS, United Kingdom

(51) INT CL[5]
G06F 13/38

(52) UK CL (Edition K)
G4A AGB AMX

(56) Documents cited
US 4025906 A

(58) Field of search
UK CL (Edition K) G4A AFL AGB AMX
INT CL[5] G06F 13/38

(54) IC Card attribute identification

(57) An IC card with outputs its own attribute information (eg type, size and access time of memory) and comprises data storage means (4-7), buffer means (8, 9) for the storage means, control means (2) for controlling the output state of the storage and buffer means, and attribute information setting means (10) (eg: pullup resistors) containing the attribute information of the IC card.

The attribute setting means is located between the storage means and the buffer means such that the attribute information determines the buffer output when the storage means is inactive (ie: High impedance O/P).

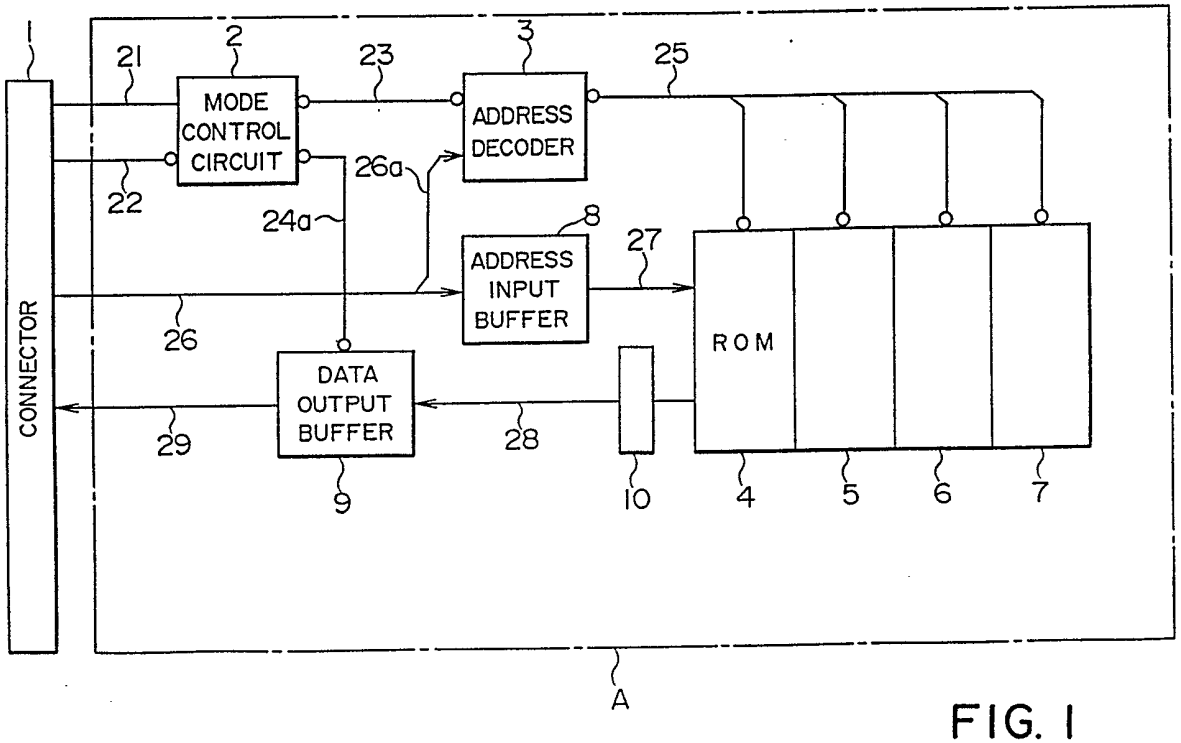
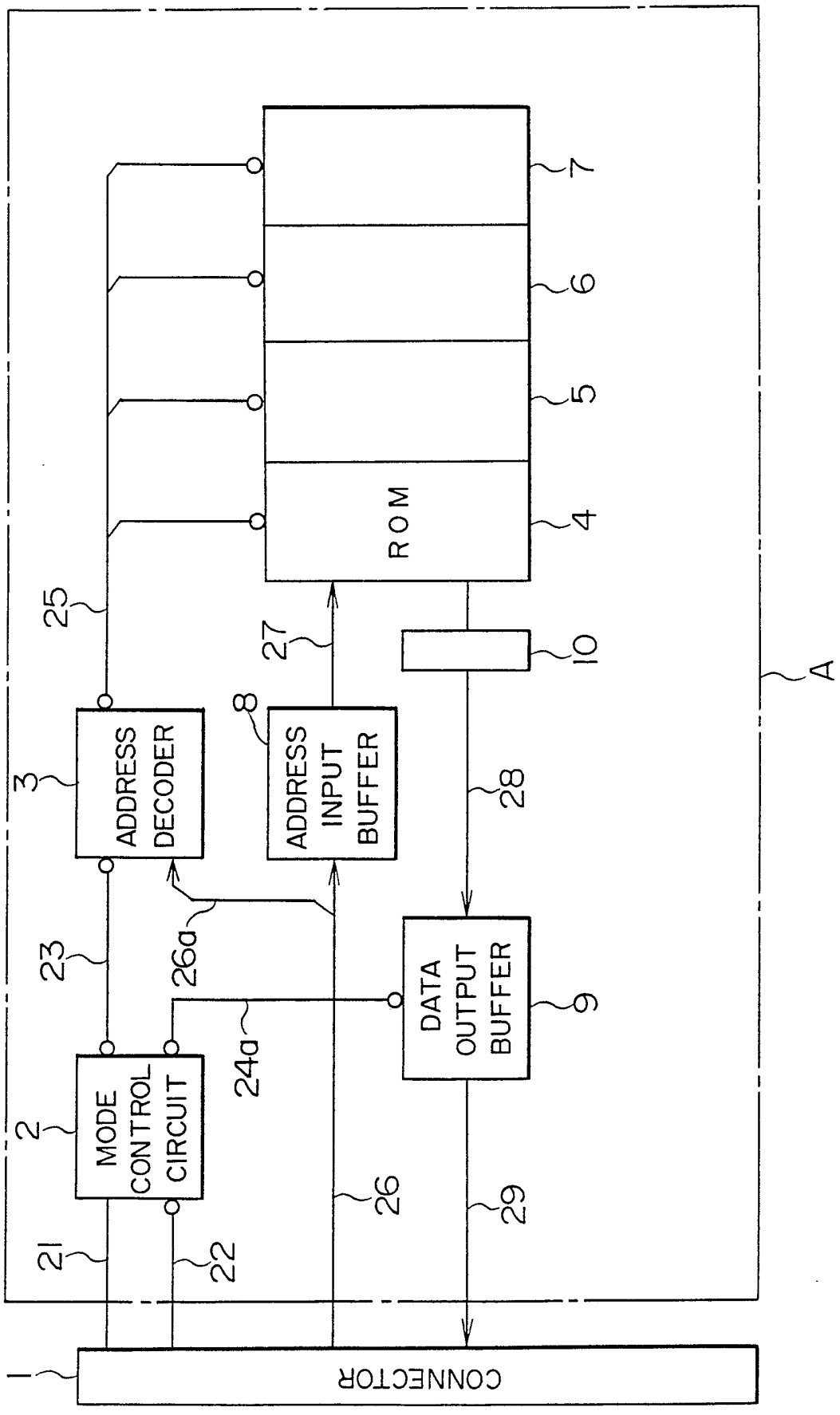


FIG. 1

GB 2 250 361 A

FIG. 1


ROM
4
5
6
7
ADDRESS DECODER
3
ADDRESS INPUT BUFFER
8
MODE CONTROL CIRCUIT
2
DATA OUTPUT BUFFER
9
10
A
CONNECTOR
1
21
22
23
24a
25
26
26a
27
28
29

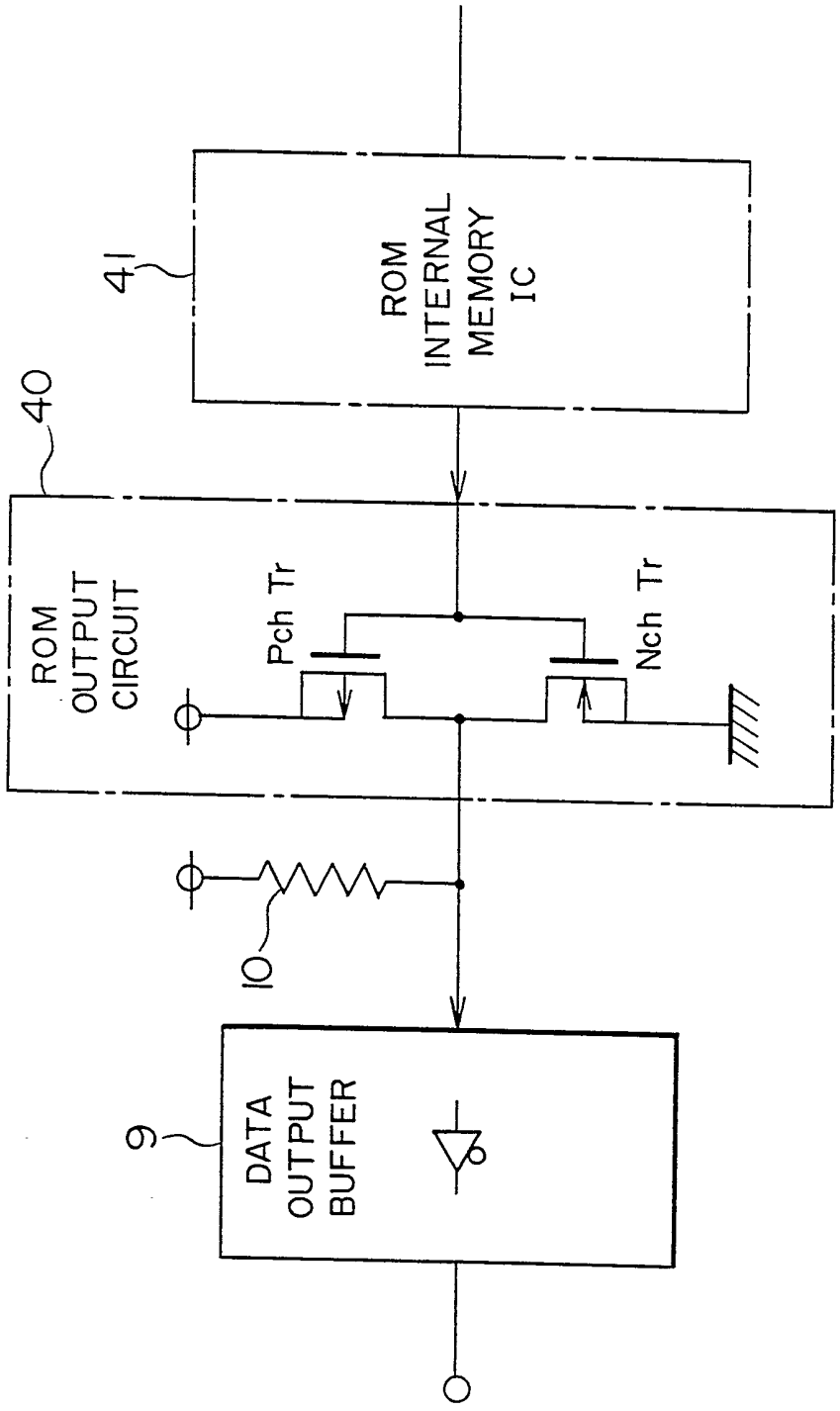

41
ROM
INTERNAL
MEMORY
IC
40
ROM
OUTPUT
CIRCUIT
Pch Tr
Nch Tr
10
9
DATA
OUTPUT
BUFFER

FIG. 2

FIG. 3

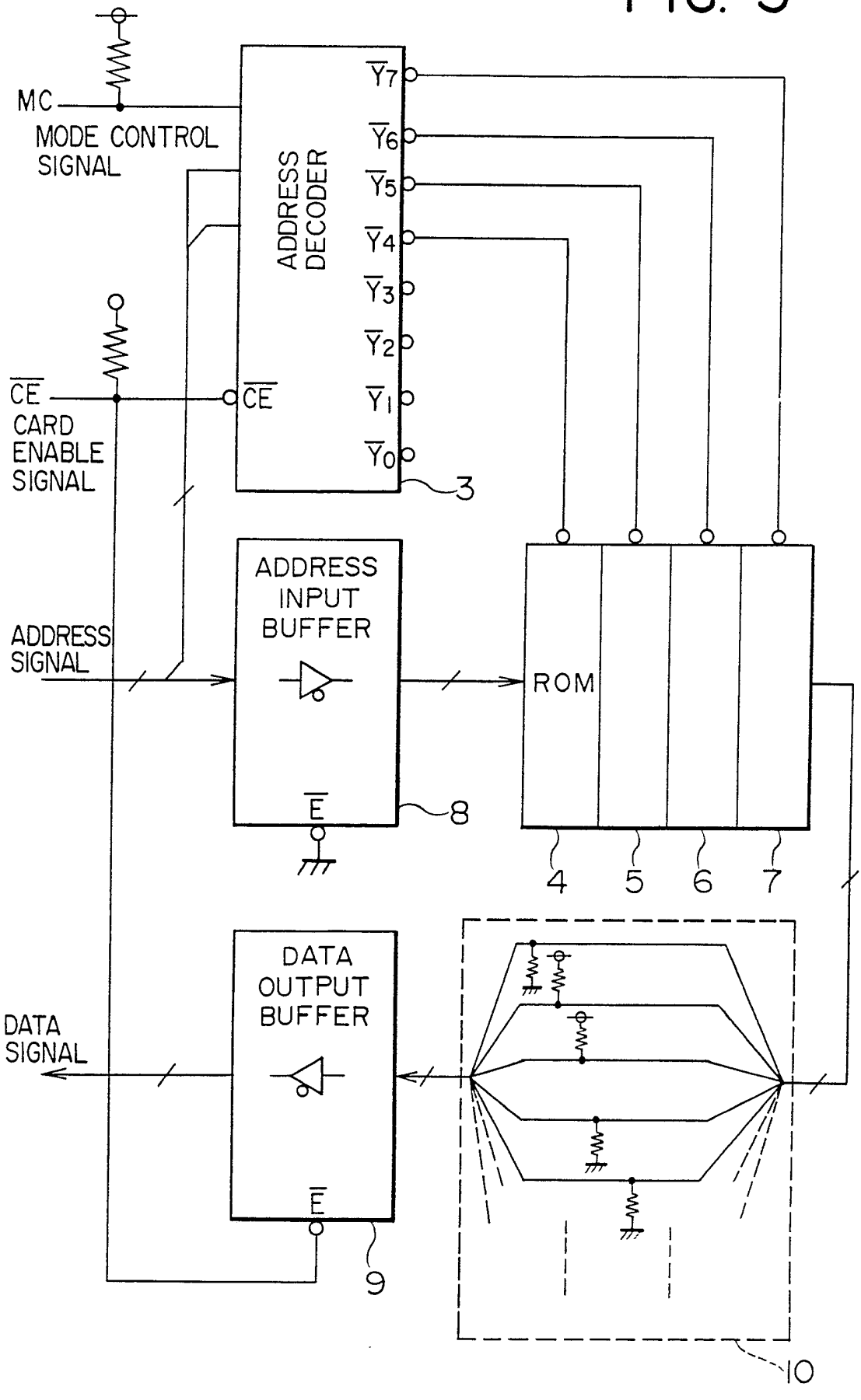

MC
MODE CONTROL SIGNAL
ADDRESS DECODER
$\overline{Y}_7$
$\overline{Y}_6$
$\overline{Y}_5$
$\overline{Y}_4$
$\overline{Y}_3$
$\overline{Y}_2$
$\overline{Y}_1$
$\overline{Y}_0$
$\overline{CE}$
$\overline{CE}$
CARD ENABLE SIGNAL
3
ADDRESS INPUT BUFFER
ADDRESS SIGNAL
$\overline{E}$
8
ROM
4
5
6
7
DATA OUTPUT BUFFER
DATA SIGNAL
$\overline{E}$
9
10

FIG. 4 PRIOR ART

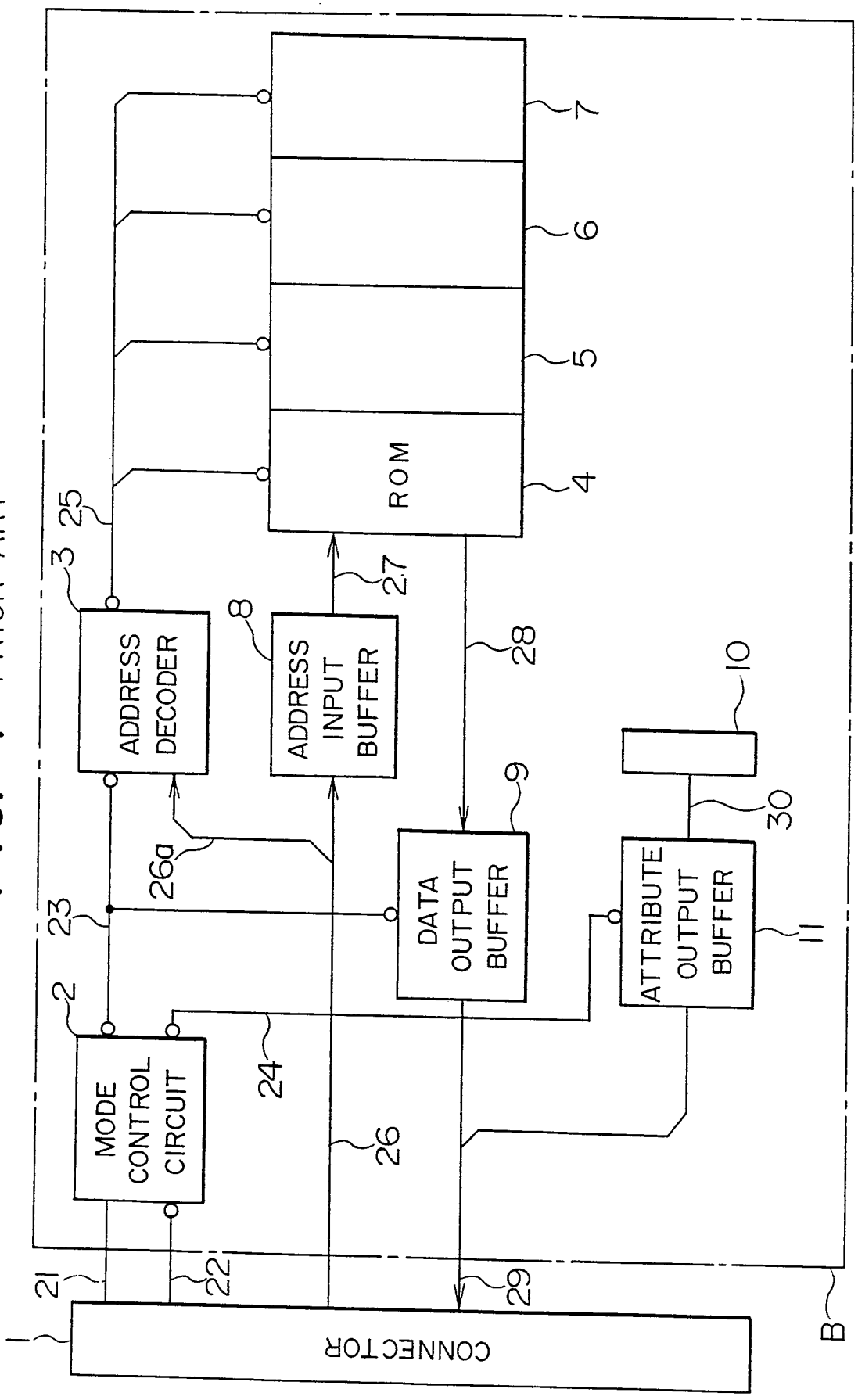


FIG. 5 PRIOR ART

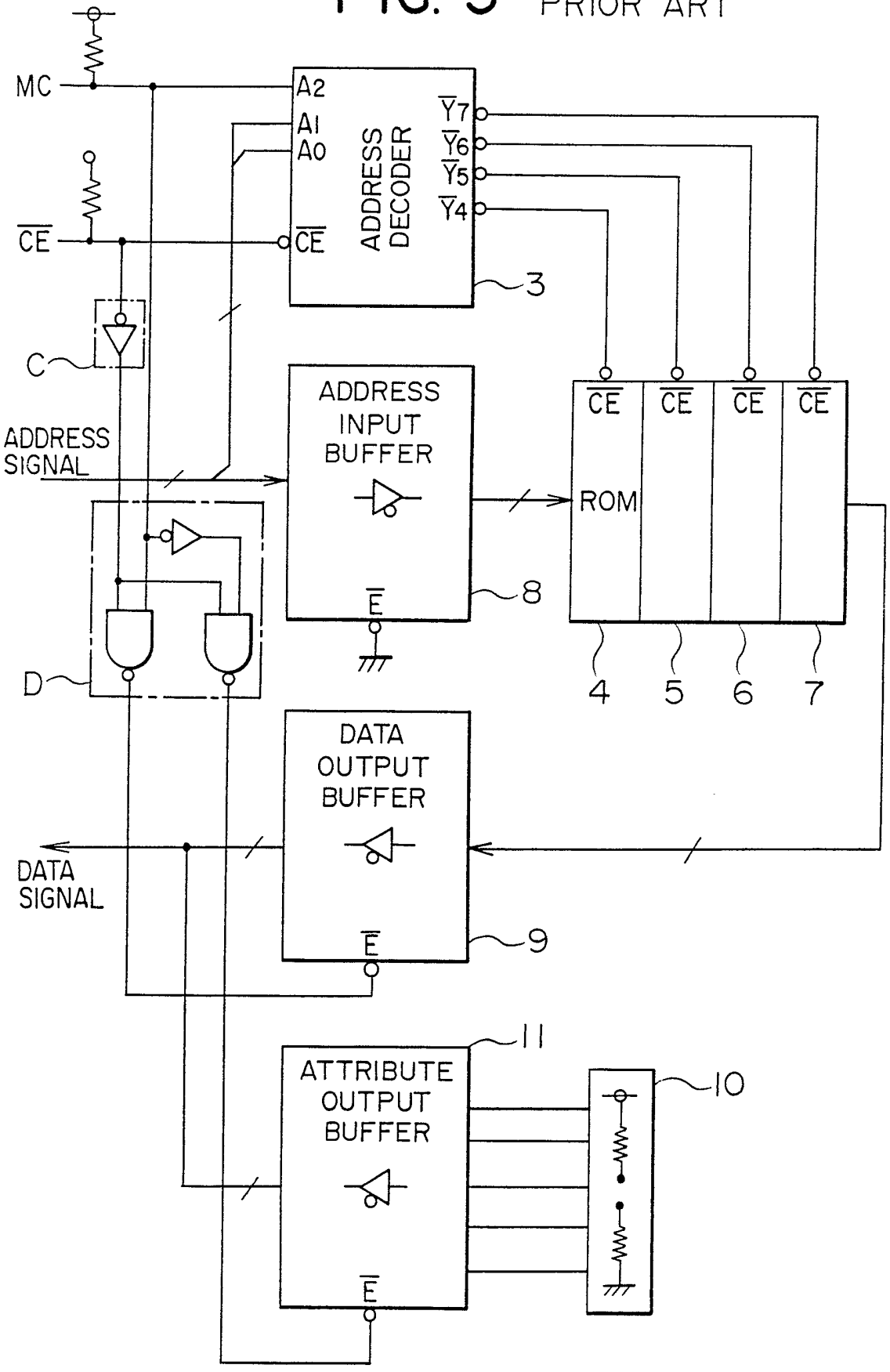
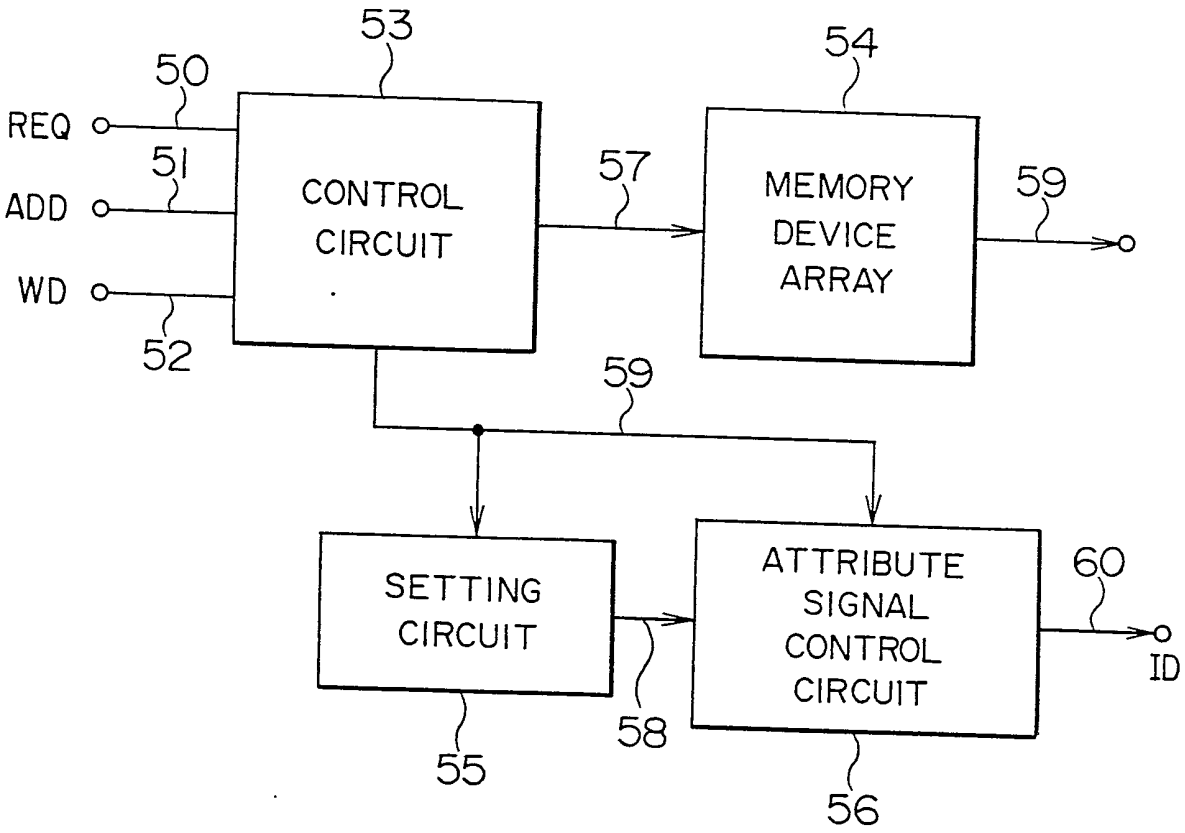


FIG. 6 PRIOR ART



IC CARD

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION:

This invention relates to an IC card having a circuit for outputting attribute information (for example; the type, capacity, and access time of the IC card memory).

DESCRIPTION OF THE RELATED ART:

Figure 4 is a block diagram showing an internal structure of conventional IC card of prior art which employs read only semiconductor memories (hereafter, ROMs). In Figure 4, 1 represents a connector, 2, a mode control circuit, and 3, an address decoder. 4 to 7 denote ROMs, and 8, an address input buffer. 9 is a data output buffer, 10, an attribute information generator circuit, and 11, an attribute output buffer.

A mode control signal 21 and a card enable signal 22 inputted via a connector 1 are provided to a mode control circuit 2. One of the outputs of the mode control circuit 2 is a memory enable signal 23. The memory enable signal 23 is inputted to an address decoder 3 and a data output buffer 9. The address decoder 3 and address input buffer 8 are provided with an address signal 26 via the connector 1. The address decoder 3 outputs a chip enable signal 25 to actuate one of ROMs 4 to 7. A post-buffer address signal 27 is

inputted from an address input buffer 8 to the ROMs 4 to 7. A data signal 28 or an output of the ROMs 4 to 7 is provided as a data signal 29 to the connector 1 via the data output buffer 9. The data signals 28 and 29, address signals 26, 26a, and 27, and chip enable signal 25 are parallel signals, which are, therefore, transmitted over a data bus, an address bus, and a signal bus, respectively.

Another output of the mode control circuit 2 is an attribute output buffer enable signal 24. This signal is inputted to an attribute output buffer 11. Pull-up and pull-down resistors 10 provided for the number of pins are connected to the attribute output buffer 11, which are used to set attribute information. An attribute data signal 30 for transmitting attribute information is outputted as a data signal 29 to the connector 1 via the attribute output buffer 11.

Next, the operations of the foregoing embodiment are explained.

A mode control circuit 2 is controlled by two inputs; that is, a mode control signal 21 and a card enable signal 22. When the card enable signal 22 is high, regardless of the level of the mode control signal 21, a memory enable signal 23 does not actuate an address decoder 3 and a data output buffer 9. Moreover, an attribute output buffer enable signal 24 does not actuate an attribute output buffer

11 (hereafter, when a certain signal does not actuate a circuit means, it is expressed as the signal is inactive. On the contrary, when a certain signal actuates a circuit means, it is expressed as the signal is active). When the card enable signal 22 is low, if the mode control signal 21 is high, the memory enable signal 23 becomes active and the attribute output buffer enable signal 24 becomes inactive. When the card enable signal 22 is low, if the mode control signal 21 is also low, the attribute output buffer enable signal 24 becomes active and the memory enable signal 23 becomes inactive.

Therefore, this kind of IC card has three output states. That is to say:

(A) Standby state

In this state, both a memory enable signal 23 and an attribute output buffer enable signal 24 are inactive. An address decoder 3, ROMs 4 to 7 connected to the address decoder 3, a data output buffer 9, and an attribute output buffer 11 are not actuated. Then, a data signal 29 is held high-impedance. To attain this state, a card enable signal 22 must be driven high.

(B) ROM read state

This is a state in which data is read out from ROMs. A memory enable signal 23 is active, and an address decoder 3 and a data output buffer 9 are actuated. However, an

attribute output buffer 11 is not actuated. At this time, any one of ROMs 4 to 7 is selected according to the upper-level address 26a of an address signal 26, then actuated by a chip enable signal 25. Then, data accessed according to the lower-level address is read out and placed on a data signal 28, then outputted as a data signal 29 to a connector 1 via the data output buffer 9. To attain this state, a card enable signal 22 must be driven low, and a mode control signal 21, high. At this time, since the attribute output buffer 11 is not actuated, the output is held high-impedance and therefore does not interrupt data read operation for the ROMs.

(C) Attribute output data read state

This is a state in which attribute information is read out. An address decoder 3 and a data output buffer 9 are not actuated, an attribute output buffer enable signal 24 is active, and an attribute output buffer 11 is actuated. At this time, all the ROMs 4 to 7 are not actuated but held high-impedance. The level set by pull-up and pull-down resistors 10 is read out as attribute output data and placed on a data signal 29.

To attain this state, a card enable signal 22 must be driven low, and a mode control signal 21 must also be driven low.

An address input buffer 8 and a data output buffer 9 are

indispensable for reducing the load across a connector 1 and thereby improving the interface characteristic of the connector 1.

Figure 5 is a circuit diagram showing the section B of Figure 4 more specifically. In Figure 5, sections C and D, and part of the functions of an address decoder form a mode control circuit 2.

Figure 6 is a block diagram showing the internal structure of other IC card disclosed in Japanese Patent Laid-Open No.63-237191. In Figure 6, an access request signal 50, an address select signal 51, and write data 52 are transferred from an upper-level unit handling a memory IC card and received at a control circuit 53. The control circuit 53 controls all components in the memory IC card, and provides a memory device array 54, an attribute signal setting circuit 55, and an attribute signal control circuit 56 with respective control signals 57 and 59. The memory device array 54 outputs read data 59. With a switching of the switchs, the attribute signal setting circuit 55 sets a signal for indicating the attribute of the memory IC card, then transmits the set signal 58 to the attribute signal control circuit 56. The attribute signal control circuit 56 controls various kinds of attribute signal. Then, the output signal 60 is transferred to the upper-level unit.

IC cards of prior art have the aforesaid configuration,

posing some problems. For example, in the first embodiment of prior art, an output buffer for reading data out of ROMs is incorporated independently of an attribute output buffer for reading out attribute output data. In the second embodiment of prior art, an output channel of a memory device array is provided separately from an output channel for an attribute signal setting circuit and an attribute signal control circuit which is thought to include an attribute output buffer. Thus, both the first and second embodiments are subject to a large number of components. This results in a complex circuit configuration of an IC card and thereby deteriorates the reliability of the IC card.

SUMMARY OF THE INVENTION

The present invention aims to solve the aforesaid problems. Specifically, the circuit configuration of an IC card is simplified by reducing the number of components, a circuit for outputting attribute information is added, and thus the reliability is improved.

A more specific object of the present invention is to provide an IC card comprising a storage means for storing data, a connector for interfacing with an external unit, a transmitting/receiving means for transferring control signals, address signals, and data with the external unit via the connector, a buffer means which is designed for the

storage means and connected on the transmitting/receiving means located between the connector and the storage means, a control means for controlling the active or inactive state of each of the storage means and the buffer means based on the control signals sent from the external unit, and an attribute information setting means which is connected to the transmitting/receiving means located between the storage means and the buffer means, and contains the attribute information of the IC card. When the storage means is inactivated while the buffer means is activated under control of the control means, the attribute information contained in the attribute information setting means is outputted to the external unit via the buffer circuit and the connector.

In the IC card according to the present invention, when the storage means is inactivated and the a buffer means designed for the storage means is activated based on control of the control means, the attribute information contained in the attribute information setting means which is connected to the transmitting/receiving means located between the storage means and the buffer means is outputted to an external unit via the transmitting/receiving means.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram showing the internal structure of an IC card according to the first embodiment of

the present invention.

Figure 2 is a schematic circuit diagram of the output section of the IC card shown in Figure 1.

Figure 3 is a schematic circuit diagram of the main section of the IC card shown in Figure 1.

Figure 4 is a block diagram showing the internal structure of conventional IC card.

Figure 5 is a schematic circuit diagram of the main section of the IC card shown in Figure 4.

Figure 6 is a block diagram showing the internal structure of other IC card of prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention is explained below.

Figure 1 is a block diagram showing the internal structure of an IC card according to an embodiment of the invention, wherein ROMs are employed as a storage means. 1 to 10 denote the same components as those for embodiments of prior art, whose explanation is, therefore, omitted.

What the embodiment of Figure 1 differs from embodiments of prior art are that an attribute output buffer 11 is omitted and that pull-up and pull-down resistors 10 or other circuit elements which form an attribute information setting circuit for setting attribute information are arranged between the data terminals of ROMs 4 to 7 and a data output

buffer circuit 9.

A mode control signal 21 and a card enable signal 22, which are inputted via a connector 1, are provided to a mode control circuit 2. One of the outputs of the mode control circuit 2 is a memory enable signal 23 which is inputted exclusively to an address decoder 3. Another output of the mode control circuit 2 is an output buffer enable signal 24a which is inputted into a data output buffer circuit 9. An address signal 26 is inputted to the address decoder 3 and an address input buffer 8 via the connector 1. 26a represents an upper-level address signal. A chip enable signal 25 is outputted from the address decoder 3, thereby one of semiconductor memory elements, such as ROMs 4 to 7, is actuated, and a post-buffer address signal 27 is inputted from the address input buffer 8 to the ROMs 4 to 7. Thus, output data is specified. A data signal 28 or an output of the ROMs 4 to 7 is outputted as a data signal 29 to the connector 1 via an attribute information setting circuit 10 including pull-up and pull-down resistors provided for the number of connector pins, and a data output buffer 9.

When a data output buffer 9 is activated by an output buffer enable signal 24a and ROMs 4 to 7 are inactivated by a memory enable signal 23, an attribute data signal containing attribute information specified by pull-up and pull-down resistors 10 is outputted as a data signal 29 from

a connector 1 to an external unit via a data output buffer 9.

An attribute information setting circuit 10 comprising a plurality of pull-up and pull-down resistors is explained in more detail. Data signals 28 and 29, which are parallel signals similarly to address signals, are transmitted over a data bus. The data bus is a bundle of multiple data lines (See Figure 3). A pull-up or pull-down resistor is connected to each data line (See Figures 2 and 3). Depending on the combination of pull-up and pull-down resistors, parallel signals which are driven low or high as intended are generated as attribute information.

In the embodiment shown in Figure 1, ROMs 4 to 7 form a storage means. The data output buffer 9 serves as a buffer means. The output mode control signal 21, the card enable signal 22, the memory enable signal 23, the output buffer enable signal 24a, the chip enable signal 25, address signals 26, 26a, and 27, data signals 28 and 29, the address decoder 3, and the address input buffer 8 constitute a transmitting/receiving means. The mode control circuit 2 operates as a control means. The attribute information setting circuit comprising a plurality of pull-up and pull-down resistors 10 acts as an attribute information setting means. A control signal represents the mode control signal 21 and card enable signal 22.

Next, the operations of the foregoing embodiment of the invention are explained.

A mode control circuit 2 is controlled by two inputs; that is, a mode control signal 21 and a card enable signal 22. When the card enable signal 22 is high, regardless of the level of the mode control signal 21, a memory enable signal 23 and an output buffer enable signal 24a become inactive. When the card enable signal 22 is low, if the mode control signal 21 is high, the memory enable signal 23 and output buffer enable signal 24a become active. When the card enable signal 22 is low, if the mode control signal 21 is low, the memory enable signal 23 becomes inactive and the output buffer enable signal 24a becomes active.

Similarly to IC cards of prior art, the IC card according to the present invention has the following three states:

(A) Standby state

In this state, a memory enable signal 23 and an output buffer enable signal 24a are inactive, an address decoder 3, ROMs 4 to 7 connected to the address decoder 3, and a data output buffer 9 are not actuated, and a data signal 29 is held high-impedance.

To attain this state, a card enable signal 22 must be driven high.

(B) ROM read state

This is a state in which ROMs are read out. An address decoder 3 and a data output buffer 9 are actuated.

To attain this state, a card enable signal 22 must be driven low, and a mode control signal 21, high. At this time, according to the upper-level address 26a of an address signal 26, any one of ROMs 4 to 7 is selected by a chip enable signal 25. In addition, data specified according to the lower-level address is read out and placed onto a data signal 28, then outputted as a data signal 29 to a connector 1 via a data output buffer 9.

At this time, the data signal 29 is driven by any one of the ROMs 4 to 7. Neither pull-up nor pull-down resistors 10 affect the aforesaid operation. This is explained using Figure 2. In the circuit diagram of Figure 2, a ROM output circuit 40 is formed as, for example, a complementary metal oxide semiconductor (CMOS). A pull-up resistor 10 is connected to a data line between a ROM data terminal and the data output buffer 9. In Figure 2, a circuit element of the output circuit 40 is formed as a CMOS, wherein a P-channel transistor and an N-channel transistor are connected in series in that order between the power supply and ground, a data signal is provided to each of the transistor gates, and a data line is connected to the joint of the transistors.

In Figure 2, when an output data signal of a ROM internal memory IC 41 is low, a P-channel transistor is

turned off, and an N-channel transistor, on. If the resistance of a pull-up resistor 10 is set so that current coming from the pull-up resistor 10 will be less than the current absorption capacity of the N-channel transistor, the N-channel transistor absorbs current flowing from the pull-up resistor 10. As a result, a low-level signal is transmitted to a data output buffer 9. When an output signal of the ROM internal memory IC 41 is high, the P-channel transistor is turned on, and the N-channel transistor, off, thereby no current flows in from the pull-up resistor 10. Consequently, a high-level signal is transmitted to the data output buffer 9. In the same manner, even when a pull-down resistor is connected, a signal sent from a ROM output circuit is transmitted to the data output buffer circuit 9 without changing the level. In this case, the resistance of the pull-down resistor should be set so that when the P-channel transistor is on, the data line is held high by the current flowing from the power supply through the P-channel transistor.

(C) Attribute output data read state

This is a state in which attribute information is read out. An address decoder 3 is inactive, while a data output buffer is active.

To attain this state, a card enable signal 22 must be driven low, and a mode control signal 21, low. At this

time, all the ROMs 4 to 7 do not operate and remain high-impedance. Therefore, a data signal 28 goes to a level specified by pull-up or pull-down resistors 10. Therefore, the information of the data signal 28 is read out as attribute information via a data output buffer 9, then outputted as a data signal 29 to a connector 1. Figure 3 is a circuit diagram showing the section A of Figure 1 more specifically. In Figure 3, part of the functions of the address decoder forms a mode control circuit 2.

In the embodiment explained so far, ROMs are incorporated in the card. SRAMs, EEPROMs, OPTROMs, or other storage means can be employed to construct the same circuit. If SRAMs or other writable storage means is used, an input-output buffer, instead of an output buffer, is connected to a data line between the SRAMs and the connector. The circuit configuration of the attribute information setting circuit comprising pull-up and pull-down resistors is identical to that of the aforesaid embodiment. Therefore, the detail explanation is omitted.

The circuit of the present invention may be formed as a hybrid IC or a monolithic IC on a semiconductor substrate.

According to the present invention, a data output buffer also operates as an attribute output buffer. This results in a reduced number of components in the IC card, thus improving the reliability.

What is claimed is:

1. An IC card having a function for outputting its own attribute information to an external unit comprising:

a storage means for storing data;

a connector for interfacing with said external unit;

a transmitting/receiving means for transferring control signals, address signals, and data with the external unit via said connector;

a buffer means which is designed for said storage means and connected on said transmitting/receiving means located between said connector and said storage means;

a control means for controlling the active or inactive state of each of said storage means and said buffer means based on said control signals sent from the external unit; and

an attribute information setting means which is connected to said transmitting/receiving means located between said storage means and said buffer means, and contains the attribute information of said IC card;

said attribute information contained in said attribute information setting means being outputted to the external unit by said transmitting/receiving means via said buffer circuit and said connector when said storage means is inactivated while said buffer means is activated under control of said control means.

2. An IC card according to claim 1 wherein said storage means has an output circuit formed as a CMOS, said transmitting/receiving means includes at least one data line connected between said output circuit of said storage means and said connector, said buffer means includes a buffer circuit inserted into said at least one data wire, and said attribute information setting means has one of a pull-up resistor and a pull-down resistor respectively connected to each of said data lines between said storage means and said buffer means.

3. An IC card according to claim 2 wherein said transmitting/receiving means includes a plurality of data lines connected between said output circuit of said storage means and said connector, said buffer means includes a buffer circuit commonly inserted into said plurality of data lines, and said attribute information setting means has one of a pull-up resistor and a pull-down resistor respectively connected to each of said plurality of data lines between said storage means and said buffer means.

4. An IC card according to claim 2 wherein one circuit element of said output circuit of said storage means, which is formed as a CMOS, is composed of a P-channel transistor and an N-channel transistor which are connected in series in that order between a power supply and ground, a data signal is provided to the gates of said transistors, and said at

least one data line is connected to a joint of said transistors,

a pull-up resistor connected to said at least one data line, which has a resistance which is less than the current absorption capacity of said N-channel transistor when said N-channel transistor is on, and a pull-down resistor connected to said at least one data line, which has a resistance that allows said at least one data line to be held high level by current coming from said P-channel transistor when said P-channel transistor is on.

5. An IC card substantially as herein described with reference to figures 1 to 3 of the accompanying drawings.

18

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number

9124027.5

Relevant Technical fields

(i) UK Cl (Edition K) G4A (AGB, AMX, AFL)

(ii) Int Cl (Edition 5) G06F 13/38

Search Examiner

S J PROBERT

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search

11 FEBRUARY 1992

Documents considered relevant following a search in respect of claims

1-5

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	US 4025906 "RIIKONEN" see whole document	1

SF2(p)

lme - c:\wp51\doc99\fil000383

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

Published 1992 at The Patent Office, Concept House, Cardiff Road, Newport, Gwent NP9 1RH. Further copies may be obtained from Sales Branch, Unit 6, Nine Mile Point, Cwmfelinfach, Cross Keys, Newport, NP1 7HZ. Printed by Multiplex techniques ltd, St Mary Cray, Kent.