(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 June 2011 (23.06.2011)

PCT

(10) International Publication Number
WO 2011/074987 A1

(51) International Patent Classification:
H01L 21/82 (2006.01) *H01L 29/786* (2006.01)
H01L 29/24 (2006.01)

(21) International Application Number:
PCT/NO2010/000467

(22) International Filing Date:
16 December 2010 (16.12.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
20093551 17 December 2009 (17.12.2009) NO
61/287,472 17 December 2009 (17.12.2009) US

(71) Applicant *(for all designated States except US)*: **UNIVERSITETSSENTERET PÅ KJELLER** [NO/NO]; P.O Box 70, N-2027 Kjeller (NO).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **NAWAZ, Muhammad** [NO/NO]; Segarudstubben 2, N-2040 Kløfta (NO).

(74) Agent: **IP.COOP (IPR SA)**; P.O. Box 27, N-1629 Gamle Fredrikstad (NO).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *with amended claims (Art. 19(1))*

(54) Title: FIELD EFFECT TRANSISTOR STRUCTURE

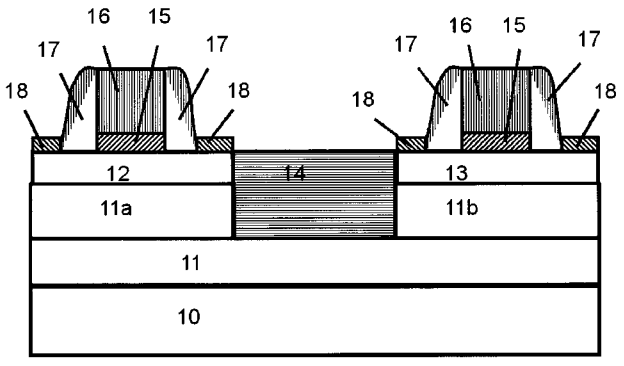

Fig. 1

(57) Abstract: A field effect transistor structure comprises a first layer (11) of undoped silicon carbide on or above the 4H-SiC substrate (10), a second layer (11a-b) of silicon carbide on or above the first layer of silicon carbide, wherein the second layer of silicon carbide has different conductivity than the first layer of silicon carbide, and a third layer (12, 13) of different material type than the first two layers of silicon carbide, preferably graphene, grown over the second layer of silicon carbide. The second layer of silicon carbide is further divided into two portions (11a-b) of different conductivities, which are separated by insulating dielectric material (14); and the third layer is further divided into two portions (12, 13) of different conductivities, which are separated by the insulating dielectric material which is in direct contact with the third and the second layer

WO 2011/074987 A1

FIELD EFFECT TRANSISTOR STRUCTURE

TECHNICAL FIELD OF THE INVENTION

The present invention generally relates to field effect transistor structures.

DESCRIPTION OF RELATED ART AND BACKGROUND OF THE INVENTION

So far, conventional silicon and silicon-on-insulator (SOI) based CMOS technologies have been the mainstream of commercial semiconductor device production, with reduction in device feature size to nanometer scale and hence providing improvements in the device performance. As the performance of a CMOS chip is generally measured by its integration density, switching speed and power dissipation, the transistor channel length and parasitic resistive-capacitive (RC) constant are the two major contributors that finally limit the circuit speed. The transistor switching delay, i.e., propagation delay, of a typical CMOS device, is a function of the device load capacitance, the drain voltage, and the saturation currents for both the n- and p-channel devices, limit the maximum operating frequency for an integrated circuit device.

Improvement of performance in conventional silicon CMOS technologies through reduction of feature size is becoming extremely difficult, if not impossible. Additionally, the electrical properties, i.e., material transport properties such as carrier mobility, of the silicon itself provide another source of performance limitation in terms of propagation delay. Note that the conventional bulk silicon and SOI based CMOS transistors, which comprise n- and p-channel MOS transistor on the same substrate, i.e., silicon substrate, suffer from imbalance due to different electron and hole mobility values. This imbalance is resulted due to higher electron mobility than hole mobility in the channel region (μ_n=1350 cm^2/V-s; μ_h =450

$cm^2/V-s$). Thus, the n-MOS transistor behaves fairly faster than the p-MOS transistor. This imbalance of electron and hole mobility in CMOS devices is further exacerbated for devices with strained silicon channels, since the strained silicon channel, i.e., process induced strain in Si and Si channel on relaxed SiGe type, does not enhance the hole mobility in the p-MOS transistor as much as it does in electron mobility in the n-MOS transistor.

Another common problem associated with conventional CMOS devices is the self heating effect. Self-heating caused by the conversion of electrical energy into thermal energy, increases the lattice temperature which influences the electron mobility, ionization and saturation velocity. The more heat generated in the active region of the device, the more influence on device performance will be. Devices operating at high drain voltage and current suffer from the reduction of carrier mobility and saturation velocity, resulting in reduction in the drain current and transconductance. Other severe problems such as increased electromigration and enhanced impact ionization because of increased device heating, affect the reliability of the devices. This problem is basically associated with difference in the thermal conductivities of Si, SiGe and SiO_2 for all standard CMOS technologies. For example, the thermal conductivity of bulk silicon is 150, compared to $Si_{0.75}Ge_{0.25}$ of 8.5, Ge of 60 and SiO_2 of 1.4 W/m.K. Note that the silicon dioxide has poor thermal conductivity value compared with silicon and $Si_{0.75}Ge_{0.25}$ (composition of 0.25 and 0.75 is typical for Ge and Si used in Si/SiGe device design). The issue of self-heating is therefore extremely important for a number of electronic device applications where the ability to remove the power which is dissipated as heat is paramount.

Yet another problem associated with conventional CMOS technologies is that the devices are operable up to a maximum of 100-120 °C with limited power handling capability. Various Si

based CMOS designs can therefore not fulfill the demand of different technological applications which require high performance, low power, and high temperature operation.

Generally speaking, low power and high performance devices need superior transport properties while high temperature and high power application demand is only fulfilled with material having high breakdown strength and wide band gap. Similarly, analog application circuitry also needs material with superior transport properties. Often, Si is used in combination with SiGe for the design of high speed CMOS.

SiC (silicon carbide) is a material of choice which overcomes all the problems mentioned earlier. Silicon carbide has gained substantial interest as a promising candidate for high power and high temperature applications. Compared to conventional silicon material used today for standard CMOS and power applications from 25 to 100 °C, silicon carbide is a wide band gap material having larger thermal conductivity values, larger breakdown field strength, and offer larger carrier saturation velocity. Because of these unique features, the SiC material is well blessed for high power devices for applications ranging from 25 up to 600 °C. Those skilled in the art know that discrete devices, i.e., MOSFETs, JFETs and BJTs, have already been tested using silicon carbide material at very high temperature. With the availability of defect free high quality 2 to 4" substrates, manufacturing of high-quality, large-area power devices are now possible. SiC exist in many forms with most common crystal polytypes such as 4H-SiC, 6H-SiC and 3C-SiC are found interesting from device application point of view. The electron and hole mobility values of 4H-SiC lie around 950 and 120 cm2/V.sec.

Graphene is a member of the class of two-dimensional materials which consists of a hexagonal array of sp^2-bonded carbon atoms, just like those found in bulk graphite. Graphene is a one-atom-

thick planar sheet of sp^2-bonded carbon atoms that are densely packed in a honeycomb crystal lattice where the carbon-carbon bond length in graphene is about 0.142 nm. Note that the intrinsic graphene is a semi-metal or zero-gap semiconductor.

Excellent transport properties of few layers graphene on oxidized silicon wafers with reported mobilities between 3000 and 270002 $cm^2/V.s$ making it an ideal choice for nanoelectronic devices. Similarly, carrier mobilities on MOS structures have found to be 4780 and 4790 $cm^2/V.s$ for electrons and holes, respectively at an effective field of 0.4 MV/cm. Compared to silicon transistors with universal mobilities of 95 and 490 $cm^2/V.s$ for holes and electrons, respectively at effective field of 0.4 MV/cm, graphene mobility values are promising for CMOS electronics. Therefore, graphene can be used to make excellent transistors. Electrons in graphene also travel ballistically over sub-micron distances. As a result, graphene-based transistors can run at higher frequencies and more efficiently that the silicon transistors used today. Electron and hole mobility values lie very close to each other, which enables balanced CMOS chip with improved switching capability. Additionally, the mobility is nearly independent of temperature between 10 K and 100K which implies that the dominant scattering mechanism is defect scattering.

Thermal conductivity of graphene is reported to be 4000-5000 W/m.K at room temperature. Combined with high thermal conductivity of SiC material, i.e., 400 W/m.K at 300K, the graphene integrated SiC based CMOS chip provides extra motivation for extended application range where thermal management is critical issue. Interesting to note that the thermal conductivity of graphene is far superior to that of conventional silicon, i.e., 150 W/m.K at 300K. Compared to silicon or other III-V materials, graphene is extremely hard and transparent over wide spectral range and therefore well-suited as passivation layer for solar cell applications as well.

A single layer or multi layer graphene growth on another material is well known in the art; see references 1-6 in the detailed description. The most common technique of graphene fabrication is exfoliation of highly oriented pyrolytic graphite (HOPG) on to a SiO_2 film, a difficult process for device fabrication on the wafer scale. Another technique is to grow graphene layers using chemical vapor deposition (CVD) using methane gas at temperature 1000-1200 °C on different substrates. Yet another technique to produce graphene is through thermal decomposition of SiC or metal carbides at high temperature in ultra-high vacuum. The face of the silicon carbide used for graphene production, the silicon-terminated or carbon-terminated, highly influences the thickness, mobility and carrier density of the graphene. From a device fabrication viewpoint, the graphene/SiC structure is favored over exfoliation, due to better reproducibility, a highly reliable interface, and commercially available high quality semi-insulating SiC wafers. Epitaxial graphene on silicon carbide can be patterned using standard microelectronics methods.

US 2009/0020764A1 presents a general concept of graphene based transistors where the graphene layer is placed over silicon carbide substrate. A manufacturing method is presented for discrete MOSFETs over silicon carbide substrate. Since silicon carbide exist in many polyforms, the type of silicon carbide substrate and its conductivity is not known since it is not disclosed. The application area of the embodiments is not targeted. Contrary to standard CMOS process, the source-drain implants are introduced before the gate oxide and gate metal process in all embodiments and inconsistency in the manufacturability also exists because of the absence of spacer layers around the gate material in the first and third embodiments. In the second embodiment, the gate stack, i.e., the gate dielectric and gate metal, and spacers are defined in the short trench region and extra angled halo implant is inserted

between the source-drain region and channel region around the gate.

In CN 101404322 (A) graphene is disclosed as being used as a conducting source drain material in a field effect transistor while the channel region is composed of small organic molecules.

SUMMARY OF THE INVENTION

A main object of the present invention is to provide preferably a high speed field effect transistor structure which is capable of not only providing an increased electron mobility in n-MOS transistors but also an increased hole mobility in p-MOS transistors using the same semiconductor material on a silicon carbide substrate.

In this respect there is a particular object of the invention to combine SiC and graphene to provide a field effect transistor structure, which addresses the aforementioned problems. Such field effect transistor structure will be well-suited both for analog and digital CMOS applications which require high performance and low power simultaneously. The manufacturability of the field effect transistor should be simple and compatible with existing standard CMOS processes.

Another object of the present invention is to find an alternate technique for CMOS devices to minimize the thermal problems, i.e., self-heating, by employing an approach based on the combined use of graphene and SiC materials.

Yet another object of the invention is to provide a field effect transistor structure which is also well-suited for high power and high temperature CMOS applications (> 100 °C).

These objects, among others, are according to the present invention, attained by field effect transistor structures as claimed in the appended claims.

According to a first aspect of the invention a field effect transistor structure is provided, which comprises a first layer of undoped silicon carbide on or above the 4H-SiC substrate, a second layer of silicon carbide on or above the first layer of silicon carbide, wherein the second layer of silicon carbide has different conductivity than the first layer of silicon carbide, and a third layer of different material type than the first two layers of silicon carbide, preferably graphene, grown over the second layer of silicon carbide. The second layer of silicon carbide is further divided into two portions of different conductivities, which are separated by insulating dielectric material, and the third layer is further divided into two portions of different conductivities, which are separated by the insulating dielectric material which is in direct contact with the third and the second layer.

By means of the present invention, a more balanced CMOS chip can be designed with improved speed performance using graphene as a channel material, which does possess approximately equal electron and hole mobilities. Silicon carbide can be used as a subchannel layer and the complete transistor structure can be designed on the undoped silicon carbide substrate.

Advantageously, the two portions of the second layer are a left portion and a right portion, the left portion being p-type doped and the right portion being n-type doped, and the dopants are provided either by an implantation technique or by in-situ epitaxial growth technique. Similarly, the two portions of the third layer may be a left portion and a right portion, and the transistor structure may further comprise a pair of left and right gate dielectric layers which are directly contacting the left and right portions of third layer, and a pair of left and right gate metal layers which are directly contacting the left and right gate dielectric layers.

Yet preferably, the transistor structure may comprise vertical LDD implants of two different dopant types wherein a first dopant type implant being of n-type is introduced in the left portions of the second and third layers in regions outside of the left gate dielectric and metal layers, and a second dopant type implant being of p-type is introduced in the right portions of the second and third layers in regions outside of the right gate dielectric and metal layers.

According to a second aspect of the invention a field effect transistor structure is provided, which comprises a first layer of undoped silicon carbide on or above a 4H-SiC substrate, a second layer of silicon carbide on the first layer of silicon carbide, wherein the second layer has a fin structure and is of different conductivity than the first layer of silicon carbide, and a third layer of different material, preferably graphene, grown over the first two layers of silicon carbide. The third layer is grown over the fin structure such that the third layer is in direct contact with the fin on each side of the fin and on top of the fin.

In one embodiment the second layer of silicon has a fin structure comprising two fins arranged side by side, and the third layer is grown over the fin structure such that the third layer is in direct contact with each of the two fins on each side of the fin and on top of the fin.

Hereby, the current handling capability of devices can be further increased. Several fins can simultaneously be etched fairly close to one another on undoped 4H-SiC substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become fully understood from the detailed description of embodiments of the present invention given herein below and the accompanying Figs. 1-5, which are

given by way of illustration only, and thus are not limitative of the present invention.

Fig. 1 displays schematically, in a cross-sectional view, a field effect transistor device according to an embodiment of the invention.

Fig. 2 displays schematically a CMOS manufacturing process flow for manufacturing the field effect transistor device of Fig. 1.

Figs. 3a-d display schematically, in cross-sectional views, and Figs. 4a-e display schematically, in perspective views, a field effect transistor device according to an embodiment of the invention during its manufacture.

Figs. 5a-b display schematically, in perspective views, a field effect transistor device according to a further embodiment of the invention during its manufacture.

DETAILED DESCRIPTION OF EMBODIMENTS

In the following description, for purposes of explanation and not limitation, specific details are set forth, such as particular techniques and applications in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced in other embodiments that depart from these specific details. In other instances, detailed descriptions of well-known techniques are omitted so as not to obscure the description of the present invention with unnecessary details.

To improve the circuit speed, it would be desirable to use similar materials in the channel region so as to have high electron and hole mobility and also comparable values to each other. For example, graphene can be used for n-MOSFET and p-MOSFET in the channel region on the same substrate. Keeping the

benefits of silicon carbide as a base material (i.e., substrate), a more balanced CMOS chip can be designed with improved speed performance using graphene as a channel material which does possess approximately equal electron and hole mobilities. SiC (silicon carbide) can be used as a subchannel layer and complete transistor structure can be designed on an undoped SiC substrate. While 6H-SiC and 3C-SiC substrate materials are possible to use in the present invention, only undoped 4H-SiC substrate will preferably be used as a substrate material. Note that the SiC material exist in many forms such as 3C-SiC, 4H-SiC and 6H-SiC where the material quality, epitaxy growth and process conditions and physical properties are different to each other.

Fig. 1 shows an exemplary embodiment of a simple CMOS structure with graphene as a channel layer 12, 13. An undoped SiC layer 11 of 1-2 μm is first grown on an undoped 4H-SiC substrate 10. A thin layer of graphene 12, 13 on SiC can be grown by many techniques such as molecular beam epitaxy, see reference 1, thermal decomposition of SiC or metal carbide at high temperature in ultra high vacuum environment. When annealed at elevated temperatures (1100-1400 °C) under vacuum, silicon carbide surfaces show a tendency towards graphitization. This process begins to appear around 1100 °C. Some of the manufacturing method to realize graphene on different substrates is given in various publications and patents, see references 1-6 below.

The layer structure 10, 11, 11a and 11b may be grown in a single growth step. Threshold voltage adjustment is provided by suitable dopants in the channel and/or subchannel layer. The dopants in the subchannel layer 11a, 11b can in fact be introduced either during the epitaxy growth step of SiC or through external threshold voltage implants. For SiC subchannel layer, nitrogen (N) and phosphorus (P) is suitable for n type dopant in the concentration range 0.1-5 $x10^{18}$ cm^{-3} while aluminum

(Al) and boron (B) is well-suited for p-type dopant in the subchannel layer in the concentration range 0.1–5 $x10^{18}$ cm^{-3}. The conductivity of the subchannel layer 11a is p-type (with dopants Al or B) and conductivity of the subchannel layer 11b is n-type (with dopants N or P). The dopants in the subchannel layer may preferably be introduced through an in-situ epitaxy step in order to keep better control of the epitaxy quality and simultaneously to avoid activation anneal process needed after implantation step. Besides in-situ doping through epitaxy growth another way to introduce dopants at the selective place is the ion-implantation technique where the dose and energy of the ion implantation is controlled to get the required concentration profile and depth of the concentration. Usually, this is the first step required on a blanket wafer to selectively introduce appropriate dopants in the epilayer over the substrate. The threshold voltage may further be adjusted by workfunction of the gate material 16 and thickness of the gate dielectric material 15.

The device manufacturing starts first by depositing a thin layer (e.g., 50-100 nm) of insulating dielectric mask (Si_3N_4) on an area where n-MOSFET and p-MOSFET devices are to be defined. This process first starts by patterning the area using lithographic technique using suitable resist as a mask. After patterning, the resist is removed while dielectric mask (Si_3N_4) still covers the area of n- and p-MOSFET device areas. The area between them is then dry etched using plasma reactive ion etching technique which isolates the two devices to make CMOS logic. The area or space 14 between the two device areas is then filled by a suitable insulator or dielectric material such as SiO_2 or Si_3N_4. This filled dielectric material may or may not be the same type of the dielectric mask material. Once filling the area 14 between the two MOSFETs, the mask material is removed and the structure is then planarized before further processing. At this stage the base structure is ready for CMOS chip.

Another suitable dielectric material 15 is then grown on the graphene surface 12, 13 which isolates the gate metal from the graphene surface. The dielectric material may be SiO_2, Si_3N_4, SiON, HfO_2, or Al_2O_3 where the properties and processing condition vary from one dielectric material to other dielectric material. The gate dielectric material may be grown by atomic layer deposition (ALD) technique, thermal or plasma oxidation, thermal or plasma nitridation, plasma vapor deposition (PVD) and/or chemical vapor deposition (CVD) techniques. It is also possible to grow same or different gate dielectric material over the graphene surface for the two types of MOSFET devices. The thickness of the gate dielectric material may be 1-20 nm and may either be the same or different over the two graphene layers 12, 13. The gate dielectric material will be in contact with the top surface of the graphene layers 12, 13. A polysilicon or metal layer 16 with required work function is then grown over the gate dielectric. Ti or TiN or Al or Ti/Al is well-suited for metal gates on 4H-SiC. One of the purposes of this material is to adjust the threshold voltage of the two MOSFET devices and may either be the same gate material or different for the two devices. The thickness of the gate material 16 may be round 100-200 nm.

An LDD (lightly doped drain) implant is then provided around the gate material. The dose and energy of the LDD implant is adjusted to get the required concentration profile on the surface area in the channel and subchannel regions. This implant further increases the conductivity of surface areas around the gate region and hence decreases the series resistance of the device. Here, the gate region (i.e. gate metal) area is first protected by a suitable mask and the vertical implant is introduced over the wafer surface. It is important to note that the LDD implant should only appear on the exposed surface of the device (exterior surface of the gate region) and dopants should not be introduced or moved laterally underneath the gate area.

Usually the dose and energy of this implant are of low to medium range in order to provide the improved conductivity in the shallow region around the gate electrode. N or P is used for n-MOSFET devices and Al or B may be used for pMOSFET devices in the LDD implants. The dopant concentration of this implant at the surface region may preferably be in the range 0.1-1 $x10^{20}$ cm^{-3}. The dopants (and their conductivity) of the LDD implant will be of opposite type with respect to that of the optional threshold voltage implant or the dopants in the channel region. For example, n type dopants (i.e. N or P) will be provided for the LDD implant while dopants in the threshold voltage implant will be of p-type (Al or B) for nMOSFET devices. The LDD implant step should follow the dopant activation anneal step which may be performed at temperature between 1200-1700 °C for 50-100 seconds.

Next step is to grow the spacer layers 17 around the gate material. The spacer layers 17 may either be of SiO_2 or Si_3N_4 material. Depending on the technology requirement, the spacer layers are laterally extended to few nanometers (50-200 nm) from the gate edge. This dielectric material in the spacer layer may be of the same type as (or different than) the material used earlier in the gate oxide layer 15. The thickness of the spacer layers 17 may be equal to the combined thickness of the gate metal and gate dielectric material. The spacer layer process is performed by deposition of conformal dielectric layer using plasma enhanced chemical vapor deposition technique (PECVD) and etched using reactive ion etching technique.

Vertical source-drain implants are then provided to make source-drain region of the device. The source-drain implant can be N (nitrogen) or P (phosphorous) for nMOSFET devices and Al (aluminum) or B (boron) for pMOSFET devices. The dose and energy of this implant is higher than dose and energy of the LDD implant used earlier so as to provide higher dopant concentration in the source-drain regions. The dopant

concentration in the source-drain region may be in the range 0.1-1 x10^{21} cm^{-3} and preferable be higher than 1 x10^{19} cm^{-3}. Note that the dopants and their conductivity will be of the same type as the LDD implant for n- and pMOSFET devices used earlier in the process flow. Note that the dopants should only be introduced at the exposed surface of the device (i.e. the area not covered by the gate metal) and should not be laterally introduced in the channel region underneath the gate. The source-drain implant step should follow the dopant activation anneal which may be performed at temperature between 1200-1700 °C for 50-100 seconds.

Finally, the source-drain metal contact layers 18 of any suitable metal are then deposited. The devices are then annealed to make source-drain contact ohmic. For example, the source-drain contact metal may be Ni/Ti, Ni/Ti/Pt, Ni/Ti/Al of total thickness 800-1000 nm and annealed at 600-1100 °C where the annealing time may vary from 10 to 60 seconds.

Fig. 2 is an overview of the CMOS manufacturing process flow.

Figs. 3a-d and 4a-e shows another embodiment of present invention where multigate structure is provided. Multigate Field effect transistors (MuGFETs) or FinFETs are devices where a double metal gate is placed around the fin sidewalls or a triple metal gate is placed around the thin fin sidewalls and top of the fin region, thus providing extra current handling capability.

The manufacturing process starts with the growth of undoped SiC layer 21 of 0.5-1.5 µm thickness over an undoped 4H-SiC substrate 20. Over this, a thin layer of doped SiC 22 is grown, which will define the current conducting area of the device. The dopants in the layer 22 may be p-type (e.g. Al or B) for n-MOSFET devices and n-type (N or P) for p-MOSFET devices. It is also possible to in-situ dope this layer using molecular beam

epitaxy or dope it externally using ion implantation technique before the start of other manufacturing steps. The dopant concentration may preferably be in the range 1 $x10^{16}$ cm^{-3} to 1 $x10^{18}$ cm^{-3} in the layer 22 and will be used to define the threshold voltage of the device.

A thin fin from the top layer 22 is first dry etched using reactive ion etching technique. The fin definition process starts by first depositing a thin dielectric layer (100nm) of SiO_2 or Si_3N_4 material. The layer is then patterned using lithography technique and the dielectric is dry etched using resist as a mask over the place other than the fin area. The resist is then removed and wafer is thoroughly cleaned. The remaining SiC material is dry etched using reactive ion etching technique with dielectric material as a mask over the fin area. Once the fin is etched, the dielectric is finally removed before further processing. A three-dimensional view of the fin structure is shown in Fig. 4a while a two-dimensional view is given in Fig. 3a. The height (h) of the fin may be 50-200 nm and thickness (w) of the fin may be 50-100 nm. Note that the fin definition process must be well controlled since the fin width and height may have an impact on the performance of the devices (e.g. variation of threshold voltage) and its geometrical non uniformity may have an impact on the yield over the wafer. A threshold voltage of the device is dependent on the fin thickness (w), fin height (h), dopants in the fin area and gate metal work function. The total width of the device is defined as 2h + w.

A thin graphene layer 23 is then grown over the fin area by anyone of the mentioned techniques above. A graphene layer 23 may only cover the fin or entire area of the undoped SiC substrate. Following fin definition and growth of the grapheme layer, a gate dielectric is grown around the fin. The gate dielectric 24 is deposited around the fin sidewalls and at top surface of the device. The gate dielectric may be of SiO_2, Si_3N_4,

HfO_2, or Al_2O_3 material. The thickness of the gate dielectric may be 1-20 nm. The gate dielectric may preferably be thermally grown around the fin. Optionally, the gate dielectric is grown by atomic layer deposition (ALD) technique or may be deposited using plasma enhanced chemical vapor deposition (PECVD) techniques. It is also possible to grow different thickness of the gate dielectric over top area of the fin and along the fin sidewalls. Those skilled in the art may also know that it is possible at this point to grow only gate oxide along the fin side walls and thus having only two conducting side gates while top surface of the fin may be non-conducting due to thick insulating oxide (i.e. 100-200 nm) sitting over it.

A polysilicon or gate metal 25 with required work function is then deposited at side walls and top surface of the fin. Since the gate is wrapping around the fin at top surface, and two sidewalls, the structure is therefore called as triple gate or multigate FET (MuGFET) or FinFET. In three-dimensional view, the gate dielectric layer 24 and gate metal 25 are visible at top surface and along one side of the fin (Fig. 4b). In fact, real device has gate dielectric and gate metal at other side of the fin (see Figs. 3c-d) as well. The gate metal may be Al or TiN or Ti/Al or Ni/Ti/Al. The thickness of the metal gate may be 100-200 nm. Although, it may be possible to deposit thicker gate metal.

Following gate metal process, an optional shallow LDD angled implant is performed around the gate region. The LDD implant also is followed by an activation anneal as well which may be performed at temperature between 1200-1700 °C for 50-100 seconds. The LDD implant may be N or P (nitrogen or phosphorus) for n-MOSFET devices and Al (aluminum) or B (boron) for p-MOSFET devices. The dopant concentration of this implant at the surface region may preferably be in the range 0.1-1 $x10^{20}$ cm^{-3}. The dopants (and their conductivity) of the LDD implant will be of opposite type with respect to that of the optional threshold

voltage implant or conductivity of the fin region. For example, n type dopants (i.e., N or P) will be provided for the LDD implant while optional threshold voltage implant will be of p-type (Al or B) for nMOSFET devices. Furthermore, the optional LDD implant may be provided vertically to the top surface of the fin or perpendicular to the fin sidewalls while covering region underneath the gate area by a suitable insulating mask. Dopants of the LDD implant should not move underneath the gate region.

A spacer layer 26 is then defined after the LDD implant. A spacer layer 26 may have lateral width of 50-200 nm and thickness should be equal to the combined thickness of the gate stack (i.e. gate metal and gate dielectric). Spacer layers (shown in Figs 4c-e) may be of SiO_2 or Si_3N_4 material system. Furthermore, the spacer layer may be of the same material like gate dielectric or of different material. The spacer layers are defined on both sides of the gate (along z-axis) and also along both sides of the fin (along x-axis). The deposition method of the spacer layer is similar to the first embodiment.

At this stage, devices are now ready for source-drain ion implantation. The source-drain implant can be N (nitrogen) or P (phosphorus) for nMOSFET devices or Al (aluminum) or B (boron) for pMOSFET devices. Principally, the source-drain implant is performed vertical to the device top surface and dopants should be of the same conductivity as the LDD implant. Simultaneously, the dose and energy of the source-drain implant should be higher than that of the LDD implant so as to provide required dopant concentration and junction depth. The dopant concentration in the source-drain region may be in the range 0.1–1 $x10^{21}$ cm^{-3} and preferable be higher than 1 $x10^{19}$ cm^{-3}. An area underneath the gate region is covered by a suitable insulating mask. Dopants of the source-drain implant should not move underneath the gate region. Immediately after the source-drain implant, dopant activation anneal is performed at temperature between 1200–1700 °C for 50–100 seconds.

Finally, the source-drain metal contact layers 27 of any suitable metal such as Al or Ti/Al or Ni/Ti/Al are deposited. The combined thickness of the metal layers is 500-1000 nm. The devices are finally annealed to make source-drain contact ohmic. For example, the source-drain contact metal may be Ti/Al annealed at 600-1100 °C where the annealing time may vary from 10 to 60 seconds. A complete three-dimensional view is given in Fig. 4e.

In another embodiment shown in Figs. 5a-b, a multi fin structure can be realized to further increase the current handling capability of the device. Here, several fins can simultaneously be etched on undoped 4H-SiC substrate. One possible example is where two fins are sitting on the undoped 4H-SiC substrate side by side and a gate dielectric along with a metal gate is placed covering the top surface and two side walls of the fins. The manufacturing steps and type of the material used during manufacturing process steps are similar to the previous embodiment of the invention.

While the present invention deals with only MuGFETs or FinFETs, several modifications are possible to realize such type of design structures. For example, FinFETs can be provided using similar manufacturing method with 3, 4, 5, 6, 7, 8, 9, 10, and even more number of fins on the same 4H-SiC substrate. These fins may be of different width, of different height and may use different gate or source-drain material. These modifications are sometimes needed to optimize the performance of the structure to particular applications. The scope of this invention therefore covers all such modifications using undoped 4H-SiC substrate along with combined SiC and graphene epitaxial materials.

It will be obvious that the invention may be varied in a plurality of ways. Such variations are not to be regarded as a departure from the scope of the invention. All such

modifications as would be obvious to one skilled in the art are intended to be included within the scope of the appended claims.

The following references are hereby incorporated by reference:

[1] Tang Jun et al 2009 Chinese Phys. Lett. 26, 088104, "Epitaxial Growth of Graphene on 6H-SiC (0001) by Thermal Annealing".

[2] Weijei Lu et al., "Growth of Graphene-Like Structures on an Oxidized SiC Surface" Journal of electronic materials, Vol. 38, No. 6, 2009.

[3] Jang Borz et al., US7071258, "Nano-scaled graphene plates".

[4] Kishi Kentaro et al., US6869581 "Hollow graphene sheet structure, electrode structure, process for the production thereof, and device thus produced".

[5] Kong Jing et al., WO2009129194, "Large-area single- and few-layer graphene on arbitrary substrates"

[6] De Heer Walt A et al., US2009236609, "Method and Apparatus for Producing Graphene Oxide Layers on an Insulating Substrate".

[7] Brebt A. Anderson et al., US2009/0020764 A1, "Graphene based transistor".

[8] Xuefeng Guo et al., CN101404322 (A), "Field effect transistor device with graphene as electrode and method for producing the same".

CLAIMS

1. A field effect transistor structure on an undoped 4H-SiC substrate, characterized in

- a first layer (11) of undoped silicon carbide on or above the 4H-SiC substrate (10);

- a second layer (11a-b) of silicon carbide on or above the first layer of silicon carbide, wherein the second layer of silicon carbide has different conductivity than the first layer of silicon carbide; and

- a third layer (12, 13) of different material type than the first two layers of silicon carbide, preferably graphene, grown over the second layer of silicon carbide, wherein

- the second layer of silicon carbide is further divided into two portions (11a-b) of different conductivities, which are separated by insulating dielectric material (14); and

- the third layer is further divided into two portions (12, 13) of different conductivities, which are separated by the insulating dielectric material which is in direct contact with the third and the second layer

2. The transistor structure according to the claim 1 wherein

- the two portions (11a-b) of the second layer are a left portion and a right portion, the left portion being p-type doped and the right portion being n-type doped, and the dopants are provided either by an implantation technique or by in-situ epitaxial growth technique; and

- the two portions (12, 13) of the third layer, which is a graphene layer, are a left portion and a right portion; and the transistor structure comprises further

- a pair of left and right gate dielectric layers (15) which are directly contacting the left and right portions of third layer; and

- a pair of left and right gate metal layers (16) which are directly contacting the left and right gate dielectric layers.

3. The transistor structure according to claim 2 further comprising vertical LDD implants of two different dopant types wherein

- a first dopant type implant being of n-type is introduced in the left portions of the second and third layers in regions outside of the left gate dielectric and metal layers; and

- a second dopant type implant being of p-type is introduced in the right portions of the second and third layers in regions outside of the right gate dielectric and metal layers.

4. The transistor structure according to claim 3 further comprising

- a first pair of spacer layers (17) of dielectric material deposited at left and right sides of the left gate metal layer wherein the dielectric material of the first pair of spacer layers is in direct contact with some portion of the third layer and vertical sides of the first pair of spacer layers are in direct contact with the vertical sides of the left gate metal layer and the left gate dielectric layer;

- a second pair of spacer layers (17) of dielectric material deposited at left and right sides of the right gate metal layer wherein the dielectric material of the second pair of spacer layers is in direct contact with some portion of the third layer and vertical sides of the second pair of spacer layers are in direct contact with the vertical sides of the right gate metal layer and the right gate dielectric layer.

5. The transistor structure according to claim 3 or 4 further comprising vertical source-drain implants of two different dopant types wherein

- a first dopant type implant being of p-type is introduced in the left portions of the second and third layers in regions outside of the left gate dielectric and metal layers;

- a second dopant type implant being of n-type is introduced in the right portions of the second and third layers in regions outside of the right gate dielectric and metal layers; and

- the source-drain implants have higher dose and energy than the LDD implants so as to get higher dopant concentration and junction depth for the source-drain implants than for the LDD implants.

6. The transistor structure according to claim 5 further comprising

- two pairs (18) of source-drain metal layers sitting over and in contact with the third layer wherein

- a first one of the two pairs of source-drain metal layers are forming ohmic contacts for the source and drain outside the left gate dielectric and metal layers; and

- a second one of the two pairs of source-drain metal layers are forming ohmic contacts for the source and drain outside the right gate dielectric and metal layers.

7. A field effect transistor structure on undoped 4H-SiC substrate comprising

- a first layer (21) of undoped silicon carbide on or above a 4H-SiC substrate (20);

- a second layer (22) of silicon carbide on the first layer of silicon carbide, wherein the second layer has a fin structure

and is of different conductivity than the first layer of silicon carbide; and

- a third layer (23) of different material, preferably graphene, grown over the first two layers (21, 22) of silicon carbide, wherein

- the third layer is grown over the fin structure such that the third layer is in direct contact with the fin on each side of the fin and on top of the fin.

8. The field effect transistor structure according to claim 7 comprising

- a gate dielectric material (24) in direct contact with the third layer and extends from one side of the fin structure, above the top of the fin structure, and to the opposite side of the fin structure;

- a gate metal (25) which is in direct contact with the gate dielectric material and extends from one side of the fin structure, above the top of the fin structure, and to the opposite side of the fin structure.

9. The field effect transistor structure according to claim 8 further comprising

- a threshold voltage adjustment implant in the second layer of silicon carbide wherein the dopant is n-type for a pMOSFET device and p-type for an nMOSFET device.

10. The field effect transistor structure according to claim 8 or 9 further comprising

- an LDD implant in the second layer of silicon carbide where the dopant is n-type for an nMOSFET device and p-type for a pMOSFET device, wherein

- the LDD implant is introduced at regions outside of the gate dielectric material and the gate metal.

11. The field effect transistor structure according to any of claims 8-10 further comprising gate spacer layers (26) of dielectric material on opposite sides of and in direct contact with the gate metal and along both sides of the sidewalls of the fin structure, wherein the gate spacer layers are of similar material as the gate dielectric material.

12. The field effect transistor structure according to claim 10 further comprising a vertical source-drain implant in the second layer of silicon carbide where the dopant is n-type for an nMOSFET device and p-type for a pMOSFET device, wherein

- the source-drain implant is introduced outside of the gate dielectric material and the gate metal; and

- the dose and energy of the source-drain implant is higher than the dose and energy of the LDD implant so as to get higher carrier concentration and junction depth for the source-drain implant than for the LDD implant.

13. The field effect transistor structure according to any of claims 7-12 further comprising a pair of metal layers (27) sitting over the top end surface of the fin and in direct contact with the third layer.

14. The field effect transistor structure according to any of claims 7-13 wherein the second layer (22a-b) of silicon has a fin structure comprising two fins arranged side by side; and the third layer (23) is grown over the fin structure such that the third layer is in direct contact with each of the two fins on each side of the fin and on top of the fin.

AMENDED CLAIMS
received by the International Bureau on 27 May 2011 (287.05.2011)

1. A field effect transistor structure on an undoped 4H-SiC substrate, characterized in

- a first layer (11) of undoped silicon carbide on or above the 4H-SiC substrate (10);

- a second layer (11a-b) of silicon carbide on or above the first layer of silicon carbide, wherein the second layer of silicon carbide has different conductivity than the first layer of silicon carbide; and

- a third layer (12, 13) of different material type than the first two layers of silicon carbide, graphene, grown over the second layer of silicon carbide, wherein

- the second layer of silicon carbide is further divided into two portions (11a-b) of different conductivities, which are separated by insulating dielectric material (14); and

- the third layer is further divided into two portions (12, 13) of different conductivities, which are separated by the insulating dielectric material which is in direct contact with the third and the second layer

2. The transistor structure according to the claim 1 wherein

- the two portions (11a-b) of the second layer are a left portion and a right portion, the left portion being p-type doped and the right portion being n-type doped, and the dopants are provided either by an implantation technique or by in-situ epitaxial growth technique; and

- the two portions (12, 13) of the third layer, which is a graphene layer, are a left portion and a right portion; and the transistor structure comprises further

- a pair of left and right gate dielectric layers (15) which are directly contacting the left and right portions of third layer; and

- a pair of left and right gate metal layers (16) which are directly contacting the left and right gate dielectric layers.

3. The transistor structure according to claim 2 further comprising vertical LDD implants of two different dopant types wherein

- a first dopant type implant being of n-type is introduced in the left portions of the second and third layers in regions outside of the left gate dielectric and metal layers; and

- a second dopant type implant being of p-type is introduced in the right portions of the second and third layers in regions outside of the right gate dielectric and metal layers.

4. The transistor structure according to claim 3 further comprising

- a first pair of spacer layers (17) of dielectric material deposited at left and right sides of the left gate metal layer wherein the dielectric material of the first pair of spacer layers is in direct contact with some portion of the third layer and vertical sides of the first pair of spacer layers are in direct contact with the vertical sides of the left gate metal layer and the left gate dielectric layer;

- a second pair of spacer layers (17) of dielectric material deposited at left and right sides of the right gate metal layer wherein the dielectric material of the second pair of spacer layers is in direct contact with some portion of the third layer and vertical sides of the second pair of spacer layers are in direct contact with the vertical sides of the right gate metal layer and the right gate dielectric layer.

5. The transistor structure according to claim 3 or 4 further comprising vertical source-drain implants of two different dopant types wherein

- a first dopant type implant being of p-type is introduced in the left portions of the second and third layers in regions outside of the left gate dielectric and metal layers;

- a second dopant type implant being of n-type is introduced in the right portions of the second and third layers in regions outside of the right gate dielectric and metal layers; and

- the source-drain implants have higher dose and energy than the LDD implants so as to get higher dopant concentration and junction depth for the source-drain implants than for the LDD implants.

6. The transistor structure according to claim 5 further comprising

- two pairs (18) of source-drain metal layers sitting over and in contact with the third layer wherein

- a first one of the two pairs of source-drain metal layers are forming ohmic contacts for the source and drain outside the left gate dielectric and metal layers; and

- a second one of the two pairs of source-drain metal layers are forming ohmic contacts for the source and drain outside the right gate dielectric and metal layers.

7. A field effect transistor structure on undoped 4H-SiC substrate comprising

- a first layer (21) of undoped silicon carbide on or above a 4H-SiC substrate (20);

- a second layer (22) of silicon carbide on the first layer of silicon carbide, wherein the second layer has a fin structure

and is of different conductivity than the first layer of silicon carbide; and

- a third layer (23) of different material, graphene, grown over the first two layers (21, 22) of silicon carbide, wherein

- the third layer is grown over the fin structure such that the third layer is in direct contact with the fin on each side of the fin and on top of the fin.

8. The field effect transistor structure according to claim 7 comprising

- a gate dielectric material (24) in direct contact with the third layer and extends from one side of the fin structure, above the top of the fin structure, and to the opposite side of the fin structure;

- a gate metal (25) which is in direct contact with the gate dielectric material and extends from one side of the fin structure, above the top of the fin structure, and to the opposite side of the fin structure.

9. The field effect transistor structure according to claim 8 further comprising

- a threshold voltage adjustment implant in the second layer of silicon carbide wherein the dopant is n-type for a pMOSFET device and p-type for an nMOSFET device.

10. The field effect transistor structure according to claim 8 or 9 further comprising

- an LDD implant in the second layer of silicon carbide where the dopant is n-type for an nMOSFET device and p-type for a pMOSFET device, wherein

- the LDD implant is introduced at regions outside of the gate dielectric material and the gate metal.

11. The field effect transistor structure according to any of claims 8-10 further comprising gate spacer layers (26) of dielectric material on opposite sides of and in direct contact with the gate metal and along both sides of the sidewalls of the fin structure, wherein the gate spacer layers are of similar material as the gate dielectric material.

12. The field effect transistor structure according to claim 10 further comprising a vertical source-drain implant in the second layer of silicon carbide where the dopant is n-type for an nMOSFET device and p-type for a pMOSFET device, wherein

- the source-drain implant is introduced outside of the gate dielectric material and the gate metal; and

- the dose and energy of the source-drain implant is higher than the dose and energy of the LDD implant so as to get higher carrier concentration and junction depth for the source-drain implant than for the LDD implant.

13. The field effect transistor structure according to any of claims 7-12 further comprising a pair of metal layers (27) sitting over the top end surface of the fin and in direct contact with the third layer.

14. The field effect transistor structure according to any of claims 7-13 wherein the second layer (22a-b) of silicon has a fin structure comprising two fins arranged side by side; and the third layer (23) is grown over the fin structure such that the third layer is in direct contact with each of the two fins on each side of the fin and on top of the fin.

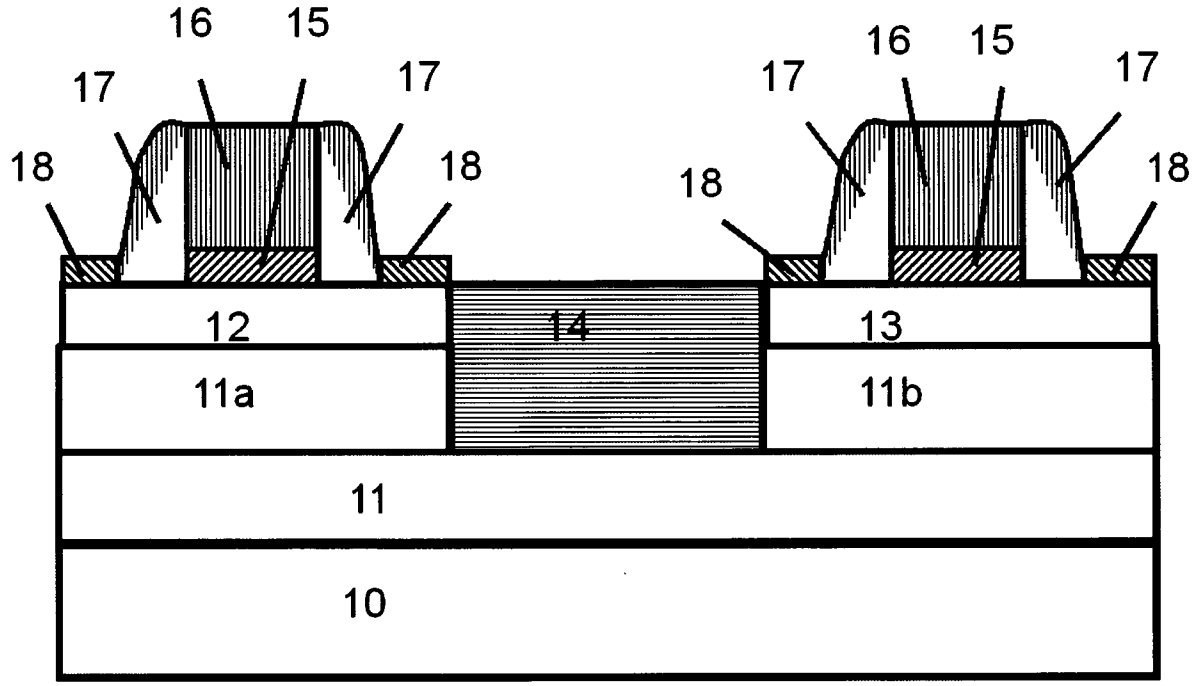

Fig. 1

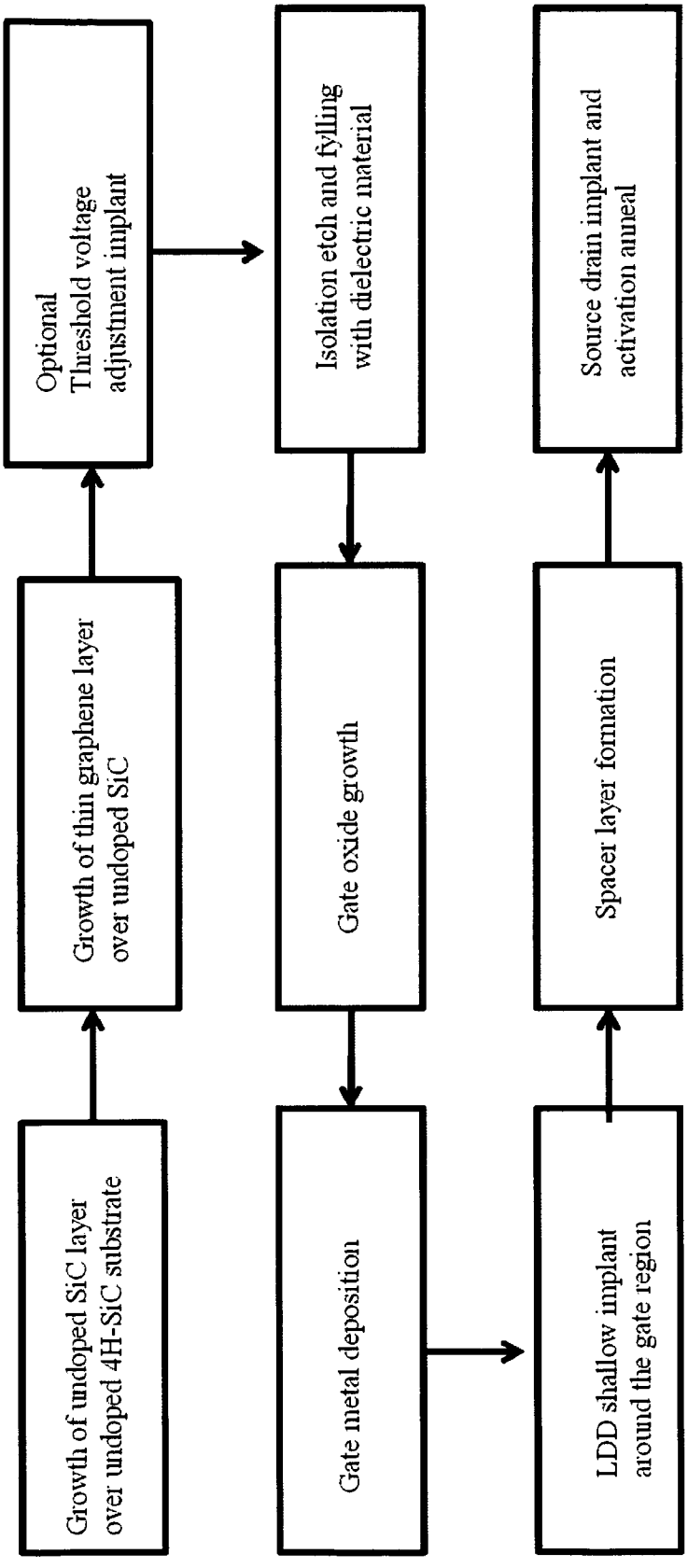
Growth of undoped SiC layer over undoped 4H-SiC substrate
Growth of thin graphene layer over undoped SiC
Optional Threshold voltage adjustment implant
Gate metal deposition
Gate oxide growth
Isolation etch and fylling with dielectric material
LDD shallow implant around the gate region
Spacer layer formation
Source drain implant and activation anneal

Fig. 2

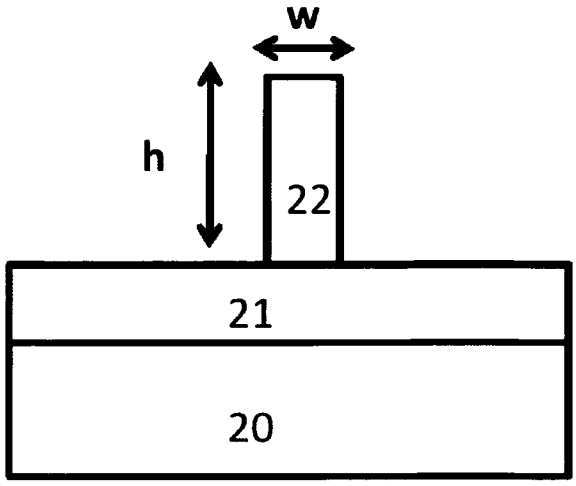

Fig. 3a

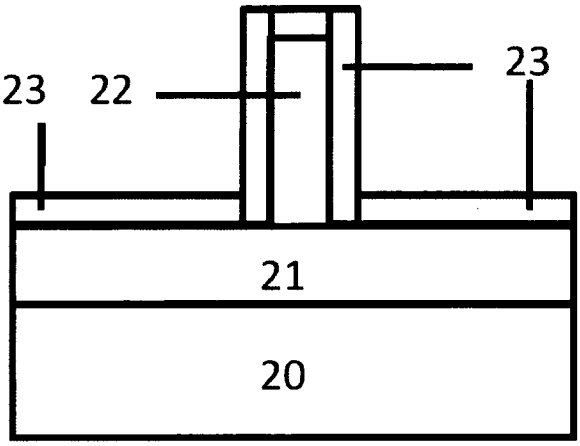

Fig. 3b

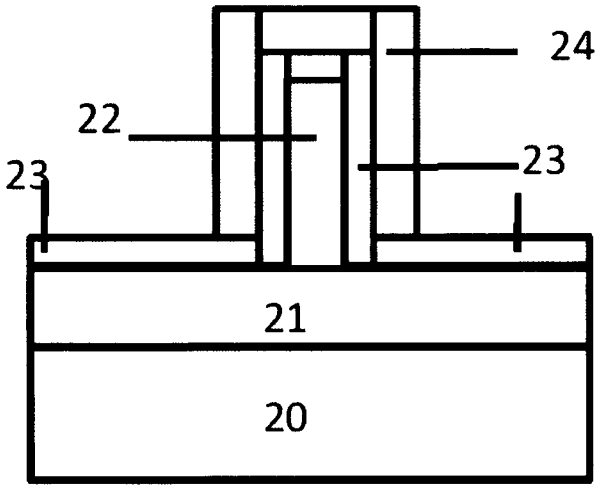

Fig. 3c

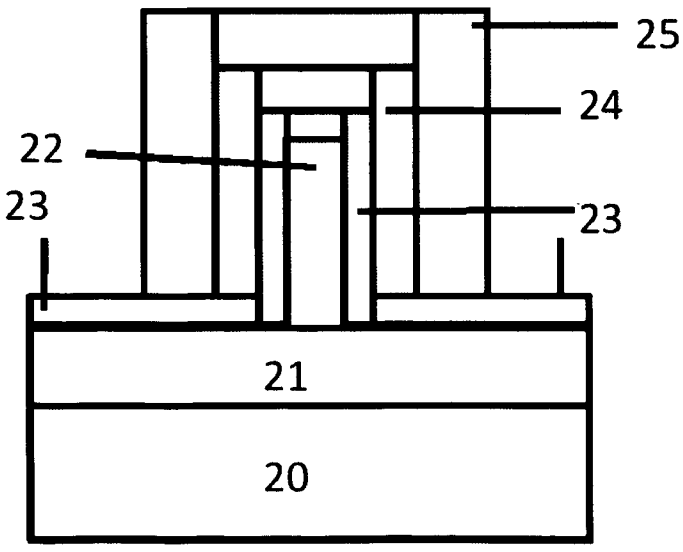

Fig. 3d

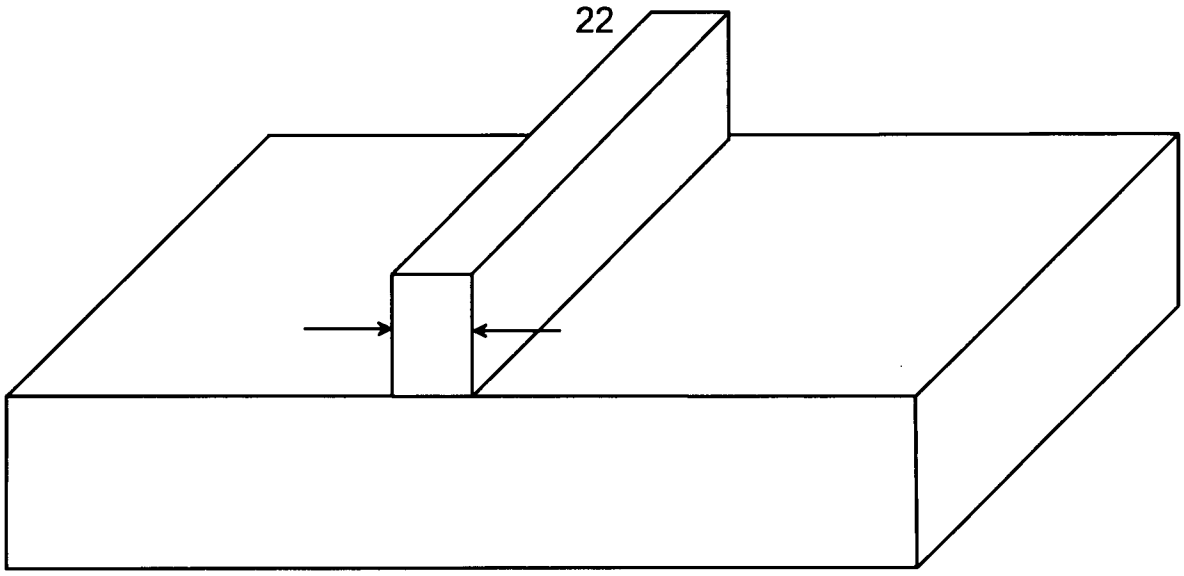

Fig. 4a

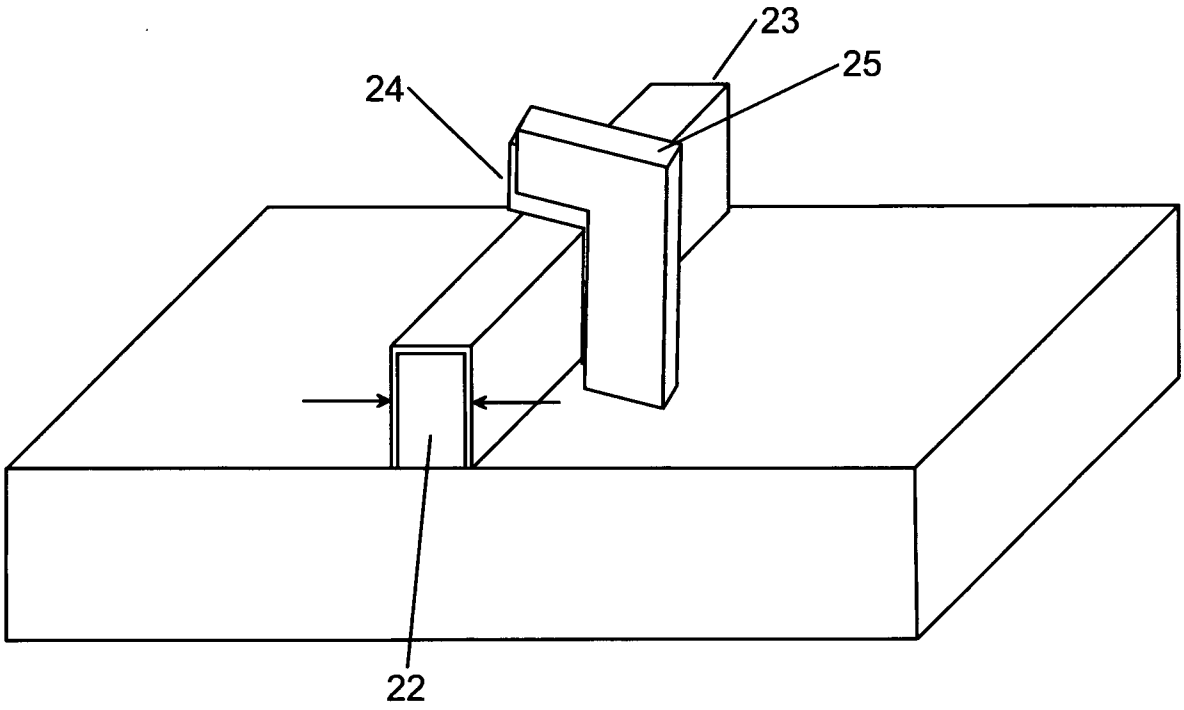

Fig. 4b

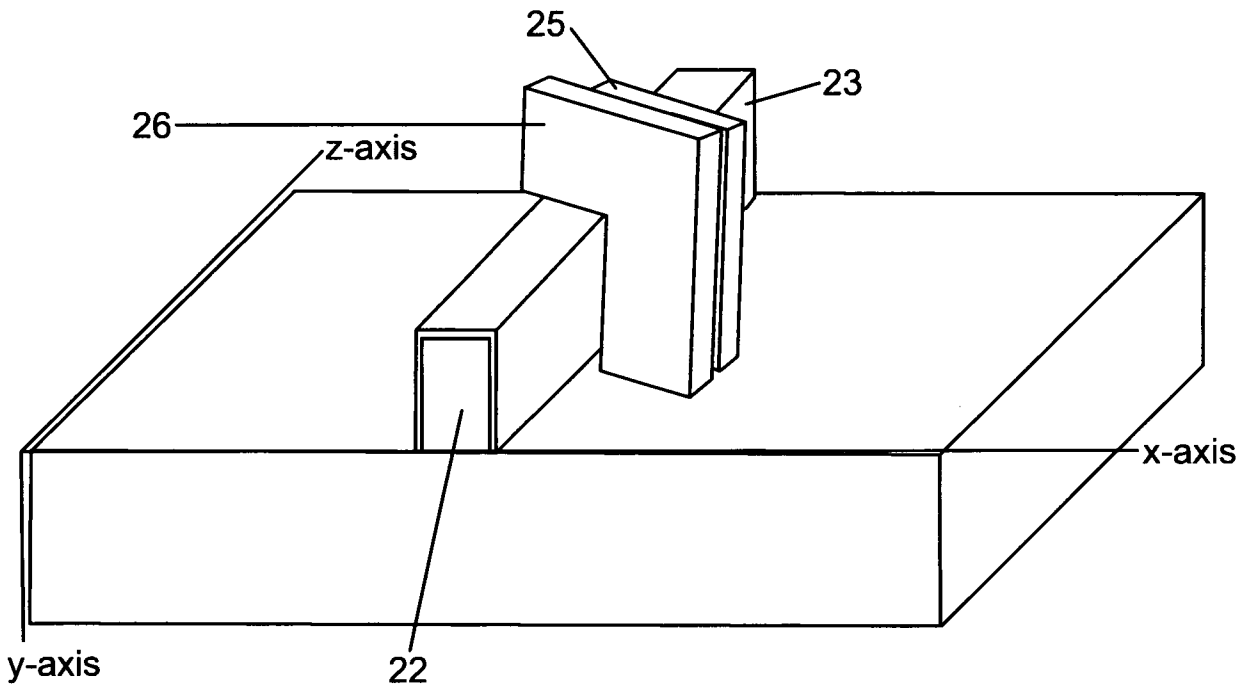

Fig. 4c

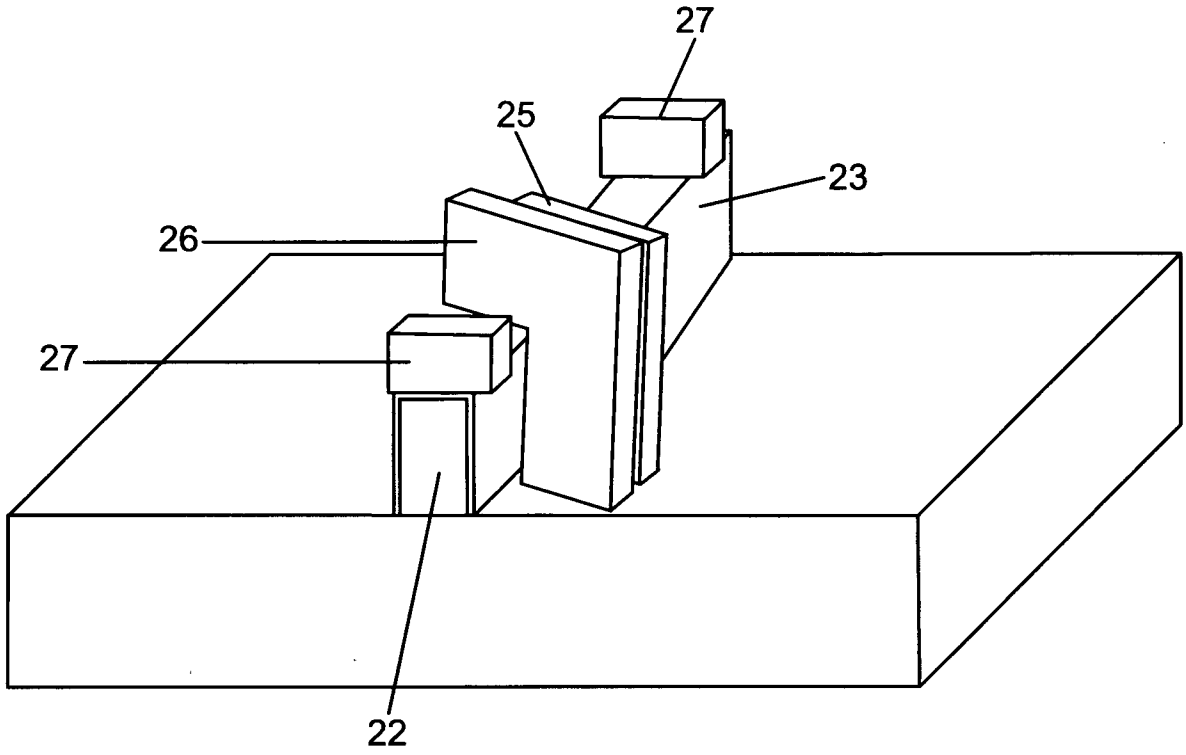

Fig. 4d

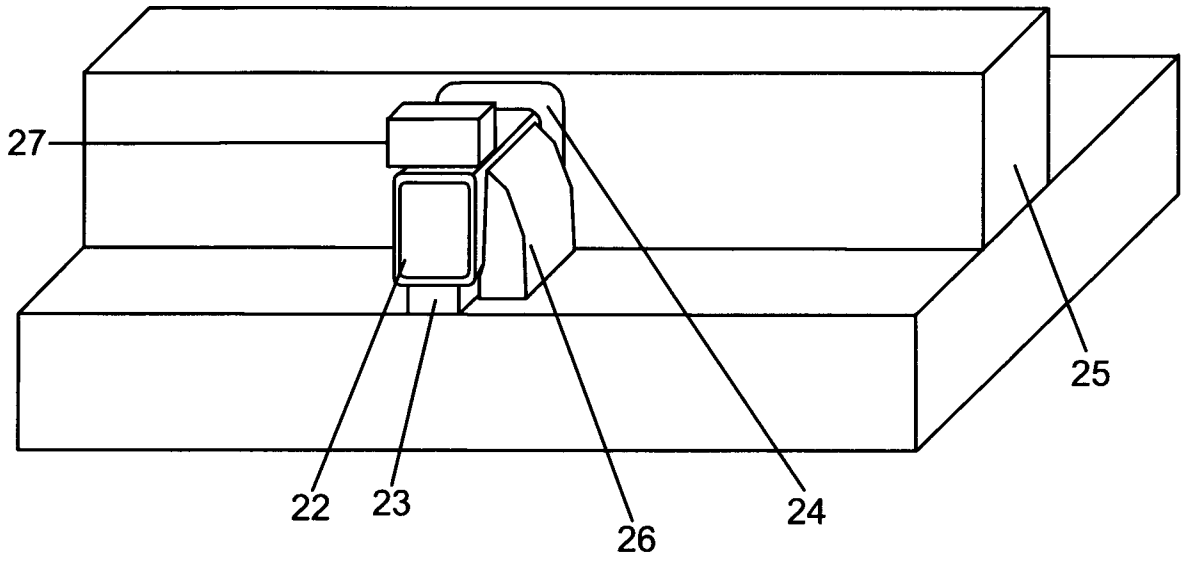

Fig. 4e

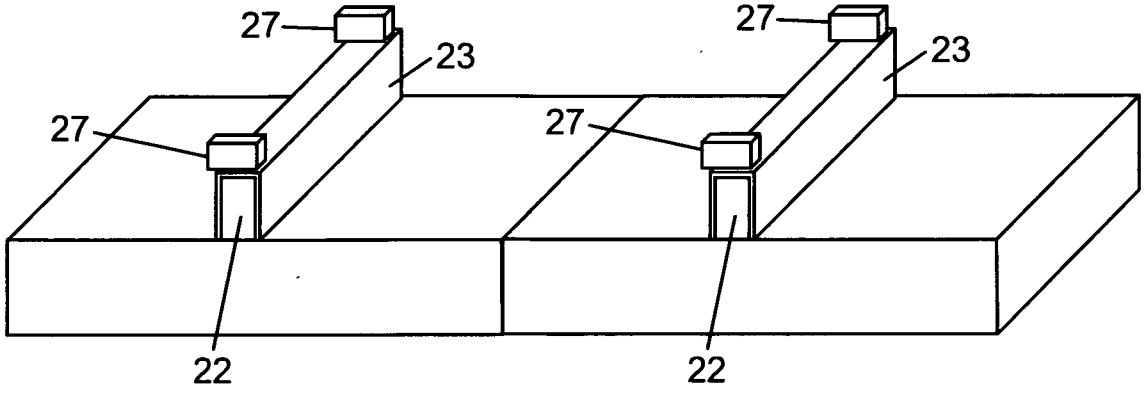

Fig. 5a

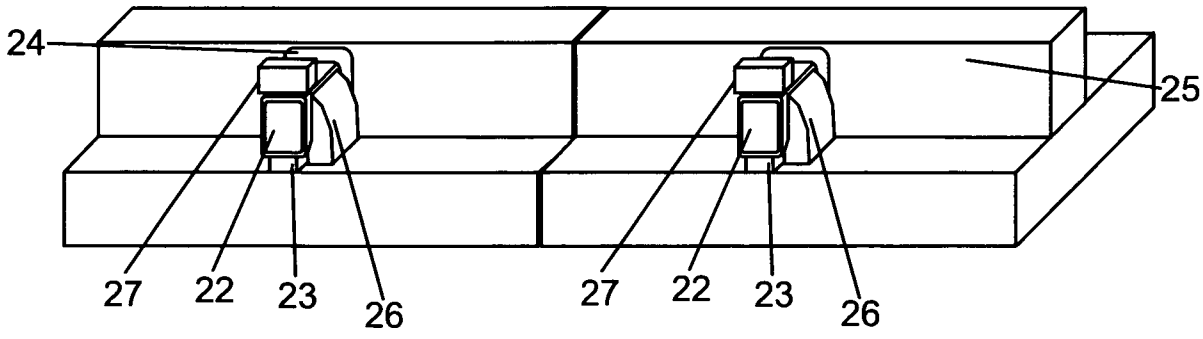

Fig. 5b

INTERNATIONAL SEARCH REPORT

International application No
PCT/NO2010/000467

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/82 H01L29/24 H01L29/786
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6 191 458 B1 (BROWN DALE MARIUS [US] ET AL) 20 February 2001 (2001-02-20) * abstract; claims; figure 7 column 2, lines 61,66 column 3, line 1 column 4, lines 1,18	1-6
Y	US 2009/020764 A1 (ANDERSON BRENT A [US] ET AL) 22 January 2009 (2009-01-22) * abstract; figures 7B,7C paragraph [0079]	7-14
Y	US 2004/253820 A1 (DEHEER WALT A [US] ET AL) 16 December 2004 (2004-12-16) * abstract; claims; figure 1I paragraphs [0012], [0026], [0028]	7-14

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 March 2011	18/04/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Wirner, Christoph

2

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/NO2010/000467

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WU Y ET AL: "Top-gated graphene field-effect-transistors formed by decomposition of SiC", APPLIED PHYSICS LETTERS, AIP, AMERICAN INSTITUTE OF PHYSICS, MELVILLE, NY, US, vol. 92, no. 9, 3 March 2008 (2008-03-03), pages 92102-92102, XP012108474, ISSN: 0003-6951, DOI: DOI:10.1063/1.2889959 * abstract; figure 2a	7-14
Y	M.YE ET AL: "Graphene Epitaxially Grown on Vicinal 4H-SiC(0001) Substrates", E-JOURNAL OF SURFACE SCIENCE AND NANOTECHNOLOGY, vol. 7, 24 January 2009 (2009-01-24), pages 29-34, XP002630463, Japan * abstract; figures	7-14
Y	JP 9 301799 A (ION KOGAKU KENKYUSHO KK; MATSUNAMI HIROYUKI; KIMOTO TSUNENOBU) 25 November 1997 (1997-11-25) * abstract; figure 5 paragraph [0071]	1-6
Y	SEI-HYUNG RYU ET AL: "Digital CMOS IC's in 6H-SiC Operating on a 5-V Power Supply", IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, vol. 45, no. 1, 1 January 1998 (1998-01-01), XP011016405, ISSN: 0018-9383 * abstract; figure 2	1-6
A	US 2006/261876 A1 (AGARWAL ANANT K [US] ET AL AGARWAL ANANT K [US] ET AL) 23 November 2006 (2006-11-23) * abstract; claims; figures	1-6
A	WO 2007/040710 A1 (CREE INC [US]; AGARWAL ANANT K [US]; KRISHNASWAMI SUMITHRA [US]; RYU S) 12 April 2007 (2007-04-12) * abstract; claims; figures	1-6

2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/NO2010/000467

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6191458 B1	20-02-2001	NONE	
US 2009020764 A1	22-01-2009	US 2010200840 A1	12-08-2010
US 2004253820 A1	16-12-2004	EP 1636829 A2	22-03-2006
		US 2006099750 A1	11-05-2006
		WO 2005001895 A2	06-01-2005
JP 9301799 A	25-11-1997	JP 3848700 B2	22-11-2006
US 2006261876 A1	23-11-2006	NONE	
WO 2007040710 A1	12-04-2007	EP 1938384 A1	02-07-2008
		JP 2009509334 T	05-03-2009
		US 2007235757 A1	11-10-2007