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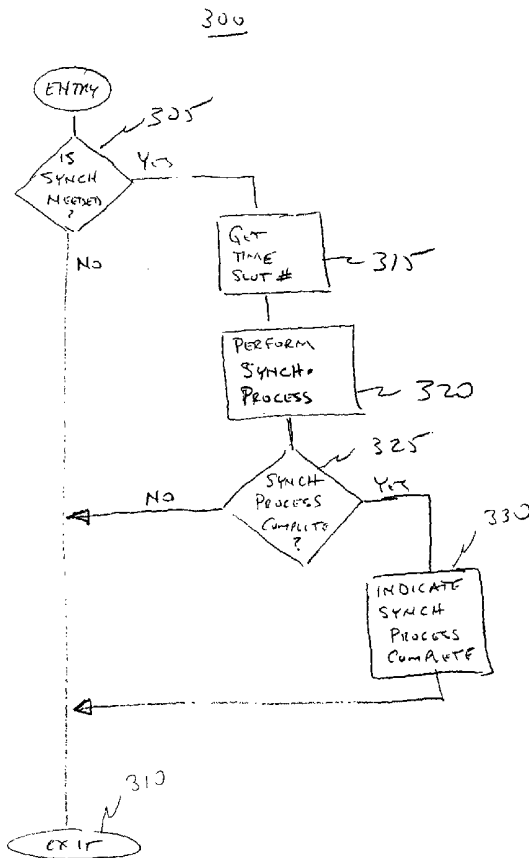
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(72) Inventors; and

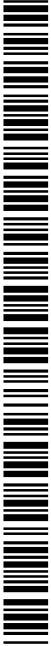
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[Continued on next page]

(54) Title: SYSTEM AND METHOD FOR DEMODULATOR STATE CONTROLLER



(57) Abstract: A method and apparatus is disclosed for performing at least one of a plurality of synchronization processes for time slot synchronization for selected time slots (315) contained in a TDM communication system, the time slots having a synchronization period of time allocated for the execution of any one of a selected one of the plurality of processes. The method comprises the steps of selecting a desired one of said plurality of synchronization processes, executing the selected synchronization process (320) in the allocated synchronization period, whereby the execution is repeatedly performed in allocated synchronization period of subsequent time slots when the execution is not completed at a termination of corresponding allocated synchronization period (325), and providing an indicator when the selected synchronization process is completed (330). In another aspect of the invention, the method is repeated for the selected time slot while time remains available during allocated synchronization period within the time slot.



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**SYSTEM AND METHOD FOR
DEMODULATOR STATE CONTROLLER**

RELATED APPLICATIONS

The present application is related to co-pending and commonly assigned U.S. Patent Applications S.N. 09/434,832, 09/434,815, 09/434,816, and 09,434,707, each entitled "SYSTEM AND METHOD FOR BROADBAND MILLIMETER WAVE DATA COMMUNICATION", the disclosures of which is hereby incorporated herein by reference. The aforementioned applications are each a divisional of commonly assigned U.S. Patent No. 6,016,313 entitled "SYSTEM AND METHOD FOR BROADBAND MILLIMETER WAVE DATA COMMUNICATION" issued 18 January 2000 and currently undergoing two re-examinations under Application S.N. 90/005,726 and Application S.N. 90/005,974.

The present application is related to and is being concurrently filed with commonly assigned U.S. Patent Application S.N. _____ entitled "SYSTEM AND METHOD FOR DYNAMIC BANDWIDTH ALLOCATION", U.S. Patent Application S.N. _____ entitled "SYSTEM AND METHOD FOR DYNAMIC BANDWIDTH ALLOCATION IN A POINT TO MULTIPOINT COMMUNICATION SYSTEM", U.S. Patent Application S.N. _____ entitled "SYSTEM AND METHOD FOR REAL TIME ADAPTIVE CAPACITY SCHEDULING", U.S. Patent Application S.N. _____ entitled "APPARATUS AND METHOD FOR MANAGING BURST PROFILE CHARACTERISTICS IN TDM SYSTEMS", and U.S. Patent Application S.N. _____ entitled "FRAME TO FRAME TIMING SYNCHRONIZATION

SYSTEM AND METHOD”, the disclosures of which is hereby incorporated herein by reference.

The present application claims the priority of co-pending U.S. Provisional Application S.N. 60/266,475 entitled “SOFTWARE PROVISIONAL APPLICATION”, the disclosure of which is hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

This application is related to wireless communication systems and more specifically to a method and apparatus for managing processes associated with time slot synchronization in TDM systems over an extended time.

As is known in the art, Time Division Multiplex (TDM) wireless communication systems increase the capacity of a single communication channel by temporally partitioning the channel into frames, which are further partitioned into time slots. Users of the system may then be allocated at least one time slot within a plurality of frames to complete the transmission or the reception of a message. In order to provide a reliable quality of service between a transmitting user and a receiving user, the receiving system must be substantially synchronized to the boundaries of the transmitting time slots. In this manner, the performance of the receiving system is maximized with regard to the transmitting information. However, changes in the environment between the transmitter and the receiver may introduce substantial delays in the received signal that consequently effect the quality of service of the received signal. For example, changes in network timing may introduce a time delay in all the data of one or more frames. Changes in symbol timing may introduce a distortion in symbols as the point of decoding symbols is altered. Similarly, changes in frequency may reduce the amplitude of the received signal

as the received signal may be shifted to an undesired portion of a filter characteristic. Hence, the wireless system provides for a periodic or dynamic execution of a plurality of processes that remove errors introduced in the time slots and synchronize the time slot to a known reference.

Synchronization processing of TDM systems is well known in the art. For example, TDM systems may be required to perform one or more processes such as AGC (Automatic Gain Control) convergence processing, symbol timing convergence processing, automatic frequency control (AFC) convergence processing, filter equalization processing and carrier recovery processing to achieve synchronization. Thus, depending upon the nature and type of error introduced, it may be necessary to perform one or more synchronization processes to achieve a desired level of synchronization.

To perform synchronization processing, a time is available is made available that is dedicated to non-data or non-payload functions. However, when one or more of the processes requires a time that exceeds the available time, the overall time slot synchronization process may not be completed. In this case, each of the synchronization processes are then repeatedly performed over an extended period until they are all successfully completed. In this case, a time slot may remain out of synchronization for an extended period of time while each of the processes is executed and completed. When the errors are significantly large, the time slot may remain continuously out of synchronization.

Hence, a method and apparatus for managing time slot synchronization over an extended period of time by retaining information regarding prior executed and successfully completed processes is needed.

BRIEF DESCRIPTION OF THE FIGURES

Figure 1 illustrates a point-to-multipoint network system;

Figure 2 illustrates a format of time slots in a TDM system;

Figure 3 illustrates a flow chart of a process for managing time slot synchronization in accordance with the principles of the invention;

Figure 4 illustrates a flow chart of a process for managing synchronization in accordance with one aspect of the process shown in Figure 3;

Figure 5 illustrates a series for achieving synchronization over a plurality of time periods in accordance with the principles of the invention; and

Figure 6 illustrates an apparatus for executing the processing depicted in Figure 3.

It is to be understood that these drawings are solely for purposes of illustrating the concepts of the invention and are not intended as a level of the limits of the invention. It will be appreciated that the same reference numerals, possibly supplemented with reference characters where appropriate, have been used throughout to identify corresponding parts.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 illustrates an exemplary wireless point-to-multipoint wireless communication system 100 for providing high speed bridging of a physical gap between a plurality of processor-based systems. In this illustrative system, process-based systems 100, 120 and 130 utilizing respective antenna elements 150, 151 and 152 communicate with centralized communication hub 101 via at least one airlink channel. Hub 101 is an omni-directional antenna array having a plurality of individual narrow beam directional antennas, each having a predetermined communication lobe that defines the antenna's spatial coverage. The antenna elements are arranged in a horizontal plane azimuthally about an axis of hub 101 to achieve an omni-directional coverage of hub 101.

Each antenna element may be operative to receive and/or transmit information or data on one or more frequency channels. In one aspect, the system may operate in a half-duplex mode, where separate frequencies are used to receive and transmit information. Alternatively, the system may operate in a full-duplex mode where a same frequency is used to receive and transmit information. Time Division Multiplex (TDM) systems increase system capability by temporally partitioning a frequency into time frames of fixed duration. Each frame is further temporally partitioned into a predetermined number of time slots. In operation, a user generally is allocated a time slot over a plurality of frames for transmission or reception of data.

Figure 2 illustrates a TDM system time 210, which is temporally partitioned into three frames 220, 230 and 240. Each time frame is further partitioned into four time slots such that frame 220 is partitioned into time slots 222, 224, 226 and 228, frame 230

is partitioned into time slots 232, 234, 236 and 238 and frame 240 is partitioned into time slots 242, 244, 246 and 248. Each of the depicted time slots is then partitioned into a period of time to transmit command/control/procedural functions and a time to transmit payload or data. One command/control/procedural function is allocated to synchronization of the time slot to a known reference. In this example, time slot 230 is shown partitioned into command time 250 and payload time 252. Time slot 234 is partitioned into command time 260 and payload time 262. Time slot 236 is partitioned into command time 270 and payload time 272. And time slot 238 is partitioned in command time 280 and payload time 282. Thus, during that time allocated for synchronization within command time 250, 260, 270, or 280, each process necessary to determine and compensate for errors that caused a lack of time slot synchronization may be performed and completed to achieve synchronization.

Figure 3 illustrates a flow chart of an exemplary process 300 for achieving time slot synchronization in accordance with the principles of the present invention. In this process, a determination is made at block 305 (is synch needed?) whether synchronization is needed. If the answer is negative, then processing ends at block 310 (exit). If, however, the answer is affirmative, then a time slot number is obtained at block 315 (get time slot #). At block 320, synchronization process is initiated (perform synch. process).

At block 325 (synch. process complete?) a determination is made whether the synchronization process for the selected time slot is completed. If the answer is in the negative, then process 300 is ended at block 310. However, if the answer is affirmative,

then an indication of synchronization process completion is made at block 330 (indicate synch process complete). Process 300 is then ended at block 310.

Figure 4 illustrates a flow chart of an exemplary synchronization processing 400 in accordance with the principles of the invention. In this process, a counter associated with a corresponding time slot is obtained at block 405 (get counter associated with T.S. #). At block 410, the counter associated with the corresponding time slot is incremented (increment counter). At block 415 (perform process associated with counter), a synchronization process associated with the time slot counter is selected and executed.

At block 420 (time remaining), a determination is made whether time remains available for the continued execution of the selected process. If the answer is negative, process 400 is ended at block 450. However, if the answer is affirmative, a determination is made at block 425 (process complete?) whether the selected process is completed. If the answer is in the negative, then the execution of the selected process is continued at block 415. If, however, the answer at block 425 is affirmative, then the time slot associated counter is saved at block 430 (save counter).

At block 435 (all process complete), a determination is made whether all processes necessary for synchronization have been completed. If the answer is negative, then the time slot counter is incremented at block 410 and a next/subsequent process is selected for execution.

If, however, the answer is affirmative, i.e., synchronization completed, then the time slot counter is reset to a nominal value at block 440 (reset counter). An indication of synchronization completion for the selected time slot is made at block 445. (indicate synch process complete).

Figure 5 illustrates an exemplary sequence 500 for achieving synchronization for each of a plurality of time slots over a plurality of time periods. In this illustrative example, counters associated with each time slot in a frame are maintained and updated to manage the level of synchronization achieved for each time slot over an extended period of time. In this example, the extended period of time is composed of four time periods, represented as 1st time 510, 2nd time 530, 3rd time 550 and 4th time 570. Furthermore, synchronization is achieved when six synchronization processes are successfully completed. It would be understood by those skilled in the art that although six synchronization processes are depicted in the illustrative example, synchronization may be achieved when any number of synchronization processes are completed, or determined not necessary to be performed.

In this example, during 1st time 510, a counter associated with time slot 512 indicates, by a value of two, that two synchronization processes have been completed. Similarly, a counter associated with time slot 514 indicates, by a value of one (1), that one synchronization process has been completed. Also, with regard to time slot 516, a counter associated with time slot 516 is set to a nominal value of zero (0), which in this example, indicates that synchronization has been completed and no further processing is necessary. Furthermore, with regard to time slot 518, an associated counter indicates, by a value of five (5), that five synchronization processes have been completed.

Referring now to 2nd time 530, time, during this time slot 512 two additional synchronization processes have been completed, as indicated by the value four (4) for the counter associated with time slot 512. Similarly for time slot 514, one additional synchronization process has been achieved, as represented by the value five (5) for the

associated counter. With regard to time slot 516, this time slot remains in synchronization as represented by the continued value of zero (0) for the corresponding counter. However, time slot 518 has achieved synchronization as indicated by the value zero (0) for its associated counter. In this embodiment of the invention, a corresponding time slot counter is reset to a nominal value of zero (0) in anticipation of subsequent synchronization processing associated with the time slot. As will be appreciated, an associated counter may be set to any other nominal value that may be appropriate for alternative counter incrementing algorithms.

Furthermore, an indicator (not shown) may be set to indicate the completion of synchronization process corresponding to the time slot 518. An indicator of synchronization completion may be contained in a location separate from an associated counter, or may be merged with an associated counter. For example, a value of "10" may be used to indicate synchronization completion for a selected time slot, wherein "1" represents an indicator of synchronization and "0" represents a counter. As will be understood by those skilled in the art, time slots may independently experience errors that require some form of synchronization processing be performed. Hence, an indication of lack of synchronization may occur independently for each time slot within a frame or may occur for synchronization of all or selected time slots in the frame. In one aspect, altering the state of the indicator associated with each time slot may indicate a lack of synchronization.

Continuing with the example of synchronization depicted in Figure 5, at the completion of 3rd time 550, time slot 512, as indicated by the value of five (5) for the associated counter has completed five synchronization processes. With regard to time

slot 514 a value of zero (0) for the associated counter indicates that synchronization is achieved. As discussed, the associated counter is set to a zero (0) value in anticipation of subsequent synchronization processing associated with time slot 514. Furthermore, an indicator (not shown) is set to indicate the completion of synchronization process corresponding to the associated time slot.

Further illustrated is that between 2nd time 530 and 3rd time 570 that with regard to time slot 516, the process illustrated in Figure 3 was executed, as indicated by the changed value of the associated counter. In this case, at the completion of 3rd time 570, five synchronization processes, as indicated by the value five (5) for the associated counter, were executed. The execution of these processes is necessary as an indication of a lack of synchronization of time slot 516 was indicated during these time periods.

With regard to time slot 518, this time slot remains in synchronization by the continued value of zero (0) for the associated counter.

With regard to 4th time 517, time slots 512 and 516 both achieve synchronization as indicated by corresponding associated counters having a zero (0) value. Furthermore, an indicator (not shown) may be set to indicate the completion of synchronization process corresponding to the associated time slot. With regard to time slots 514 and 518, these time slots remain in synchronization as indicated by the value of zero (0) for the respective associated counter.

As will be understood by those skilled in the art, in a preferred embodiment, any one of the desired synchronization processing may be selected determined and executed in contiguous time slots. In another aspect synchronization process may be selected and

determined during non-contiguous time slots. In another aspect of the invention, synchronization processing may be performed on a periodic basis, such as at a frame rate.

Although the exemplary progression of achieved levels of synchronization is shown in Figure 5 operating on each time slot within a frame independently, it would be easily understood by those skilled in the art how to alter the illustrated process to perform selected synchronization processes on all or selected time slots in all or selected time frames or frames.

Figure 6 illustrates an exemplary embodiment of an apparatus 600 that may be used for implementing the principles of the present invention. Apparatus 600 may represent a desktop, laptop or palmtop computer, a personal digital assistant (PDA), etc., as well as portions or combinations of these and other devices. Apparatus 600 may contain one or more input/output devices 602, processors 603 and memories 604, which may access one or more sources 601 that are in communication with a central station, for example. Sources 601 may alternatively be accessed over one or more network connections 610, e.g., a global computer communications network such as the Internet, a wide area network, a metropolitan area network, a local area network, a terrestrial broadcast system, a cable network, a satellite network, a wireless network, or a telephone network, as well as portions or combinations of these and other types of networks. Network connections 610 may also be representative of a PCI, ISA, microchannel communication bus, one or more internal connections of a circuit, circuit card or other apparatus, as well as portions and combinations of these and other communication media. Further, processor 603 may cause to be output over network 615 information that may be displayed or presented on display 608.

Input/output devices 602, processors 603 and memories 604 may communicate over a communication medium 606. Communication medium 606 may represent, for example, a bus, such as a DMA, ISA, PCI, etc., a communication network, one or more internal connections of a circuit, circuit card or other apparatus, as well as portions and combinations of these and other communication media. Data from sources 601 is processed in accordance with one or more software programs that may be stored in memories 604 and executed by processors 603 in order to manage synchronization processing for each time slot. As would be appreciated, processors 603 may be any means, such as general purpose or special purpose computing system, or may be a hardware configuration, such as a laptop computer, desktop computer, handheld computer, dedicated logic circuit, integrated circuit, Programmable Array Logic (PAL), Application Specific Integrated Circuit (ASIC), etc., that provides a known output in response to known inputs.

In a preferred embodiment the present invention may be implemented by computer readable code executed by processor 603. The code may be stored in the memory 604 or read/downloaded from a memory medium such as a CD-ROM, magnetic or optical disk drive or floppy disk. In other embodiments, hardware circuitry may be used in place of, or in combination with, software instructions to implement the invention. For example, the elements illustrated herein may also be implemented as discrete hardware elements.

Although the invention has been described in a preferred form with a certain degree of particularity, it is understood that the present disclosure of the preferred form has been made only by way of example, and that numerous changes in the details of

construction and combination and arrangement of parts may be made without departing from the spirit and scope of the invention as hereinafter claimed. It is intended that the patent shall cover, by suitable expression in the appended claims, those features of patentable novelty that exist in the invention disclosed. Furthermore, although the term channel is used herein with regard to frequency, it would be understood by those skilled in the art that the term channel may be readily applied to a time slot or a frequency. Thus, although the term channel is used in connection with frequency, it is not intended that the term be limited solely to frequency. Rather, it is contemplated to be within the scope of the invention that the term channel may also refer to one or more time slots on one or more frequencies.

What is claimed is:

1. A method for performing at least one of a plurality of synchronization processes for time slot synchronization for selected time slots contained in a TDM communication system, said time slots having a synchronization period of time allocated for the execution of any one of a selected one of said plurality of processes, said method comprising the steps of:
 - a. selecting a desired one of said plurality of synchronization processes;
 - b. executing said selected synchronization process in said allocated synchronization period, whereby said execution is repeatedly performed in corresponding allocated synchronization period of subsequent time slots when said execution is not completed at a termination of corresponding allocated synchronization period; and
 - c. providing an indicator when said selected synchronization process is completed.
2. The method as recited in claim 1 further comprising the step of:
 - a. repeating steps a-c while time remains available in said allocated synchronization period of time.
3. The method as recited in claim 1 wherein said subsequent time slots are contiguous.

4. The method as recited in claim 1 wherein said subsequent time slots are non-contiguous
5. The method as recited in claim 1, further comprising the step of repeating steps a-c for each of said time slots requiring synchronization.
6. The method as recited in claim 1, further comprising the step of: performing steps a-c when time slot synchronization is necessary.
7. The method as recited in claim 1, further comprising the step of: providing a second indicator when said time slot synchronization is completed.
8. The method as recited in claim 1, wherein the step of selecting one of said processes is based upon a counter associated with said selected time slot.
9. The method as recited in claim 8, wherein said counter is incremented in modulo (n) arithmetic, wherein the value of n is substantially equal to the number of said plurality of processes required for time slot synchronization of said selected time slot.
10. The method as recited in claim 1, further comprising the step of: repeating steps a-c for each of selected ones of said time slots.

11. The method as recited in claim 8, further comprising the step of:
resetting said counter when said time slot synchronization is completed.

12. An apparatus for performing at least one of a plurality of synchronization processes for time slot synchronization for selected time slots contained in a TDM communication system, said time slots having a synchronization period of time allocated for the execution of any one of a selected one of said plurality of processes, said apparatus comprising:
a memory in communication with a processor, wherein said processor is operable to execute code for:
 - a. selecting a desired one of said plurality of synchronization processes;
 - b. executing said selected synchronization process in said allocated synchronization period, whereby said execution is repeatedly performed in corresponding allocated synchronization period of subsequent time slots when said execution is not completed at a termination of corresponding allocated synchronization period; and
 - c. providing an indicator when said selected synchronization process is completed.

13. The apparatus as recited in claim 12 wherein said processor is further operable to execute code for:
 - repeating steps a-c while time remains available in said allocated synchronization period of time.
14. The apparatus as recited in claim 12 wherein said subsequent time slots are contiguous.
15. The apparatus as recited in claim 12 wherein said subsequent time slots are non-contiguous.
16. The apparatus as recited in claim 12, wherein said processor is further operable to execute code for:
 - repeating steps a-c for each of said time slots requiring synchronization.
17. The apparatus as recited in claim 12, wherein said processor is further operable to execute code for:
 - repeating steps a-c when time slot synchronization is necessary.
18. The apparatus as recited in claim 12, wherein said processor is further operable to execute code for:
 - providing a second indicator when said time slot synchronization is completed.

19. The apparatus as recited in claim 12, wherein said processor is further operable to execute code for:
 - selecting one of said processes based upon a counter associated with said selected time slot.

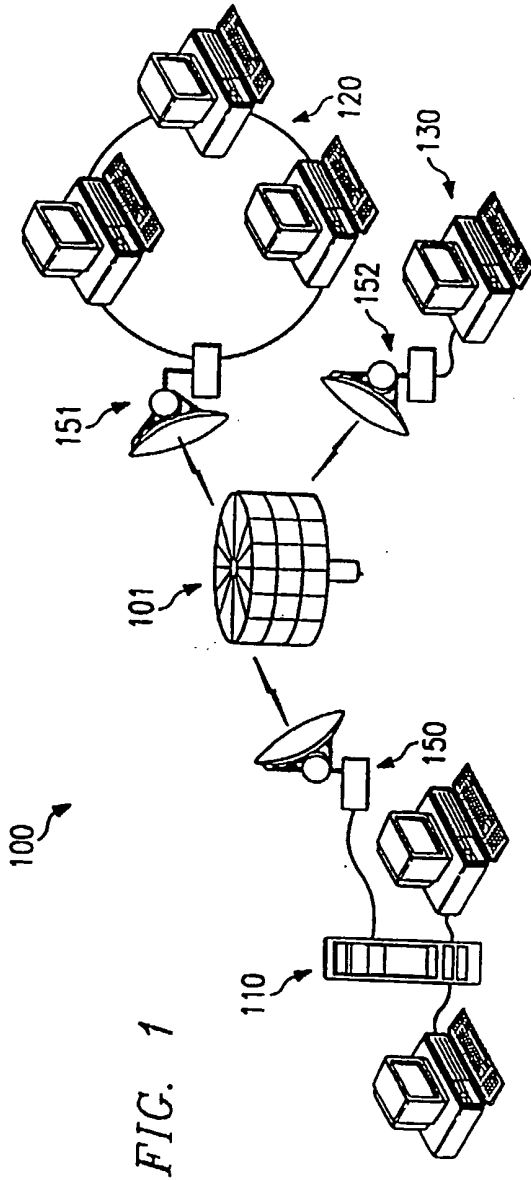
20. The apparatus as recited in claim 19, wherein said processor is further operable to execute code for:
 - incrementing said counter in modulo (n) arithmetic, wherein a value of n is substantially equal to the number of said plurality of processes required for time slot synchronization of said selected time slot.

21. The apparatus as recited in claim 12, wherein said processor is further operable to execute code for:
 - repeating steps a-c for each of selected ones of said time slots.

22. The apparatus as recited in claim 19, wherein said processor is further operable to execute code for:
 - resetting said counter when said time slot synchronization is completed.

23. The apparatus as recited in claim 12, further comprising:
 - an input/output device in communication with said processor.

24. The apparatus as recited in claim 12, further comprising:
an input/output device in communication with said memory.
25. The apparatus as recited in claim 12, wherein said code is contained in said memory.
26. The method as recited in claim 1, wherein said desired processes is selected from the group comprising: automatic gain control, symbol timing, network synchronization, equalization, carrier recovery, constellation correction.
27. The apparatus as recited in claim 12, wherein said processor is further operable to:
select said desired process from the group comprising: automatic gain control, symbol timing, network synchronization, equalization, carrier recovery, constellation correction.



Peru Act

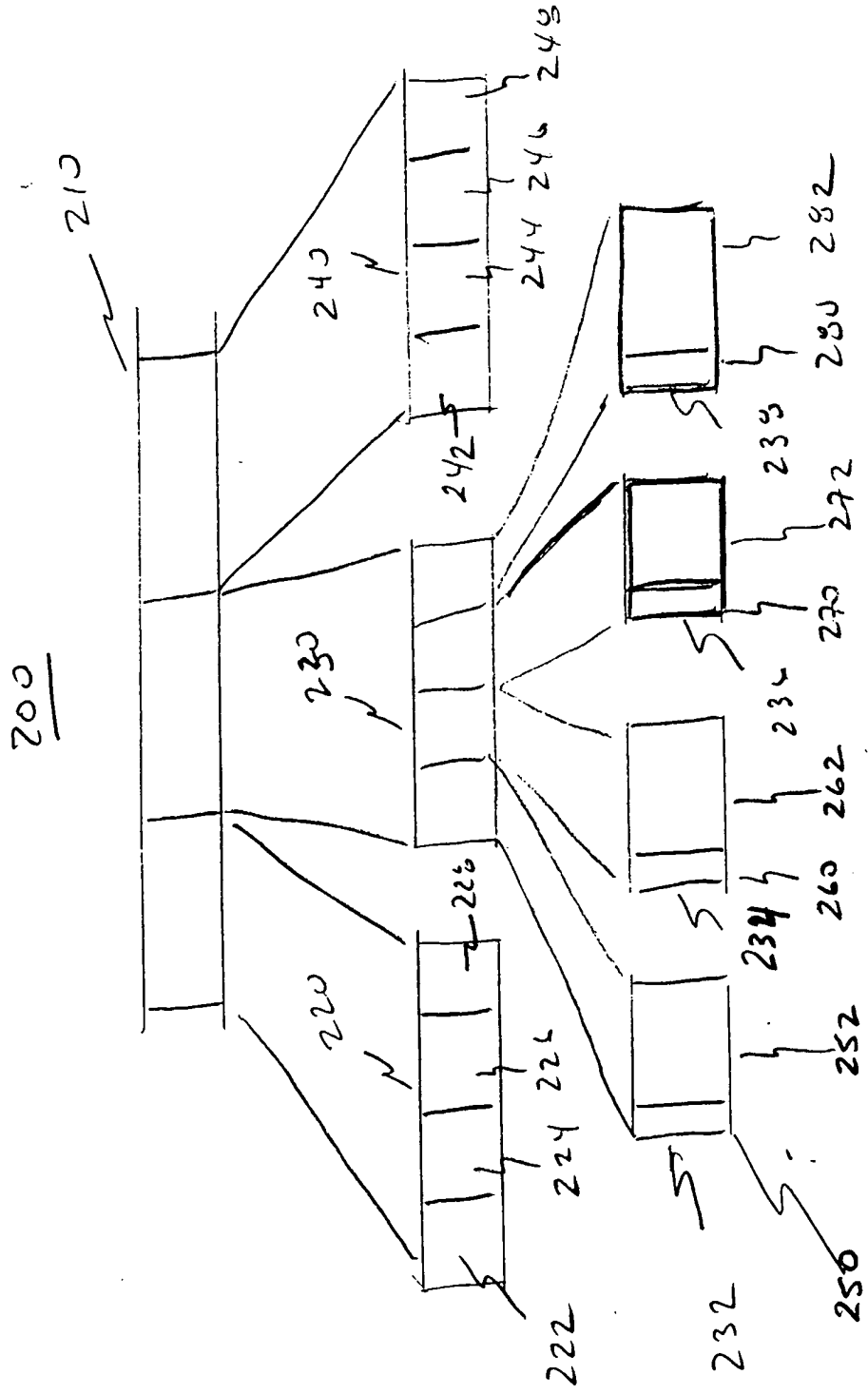


FIGURE 2

300

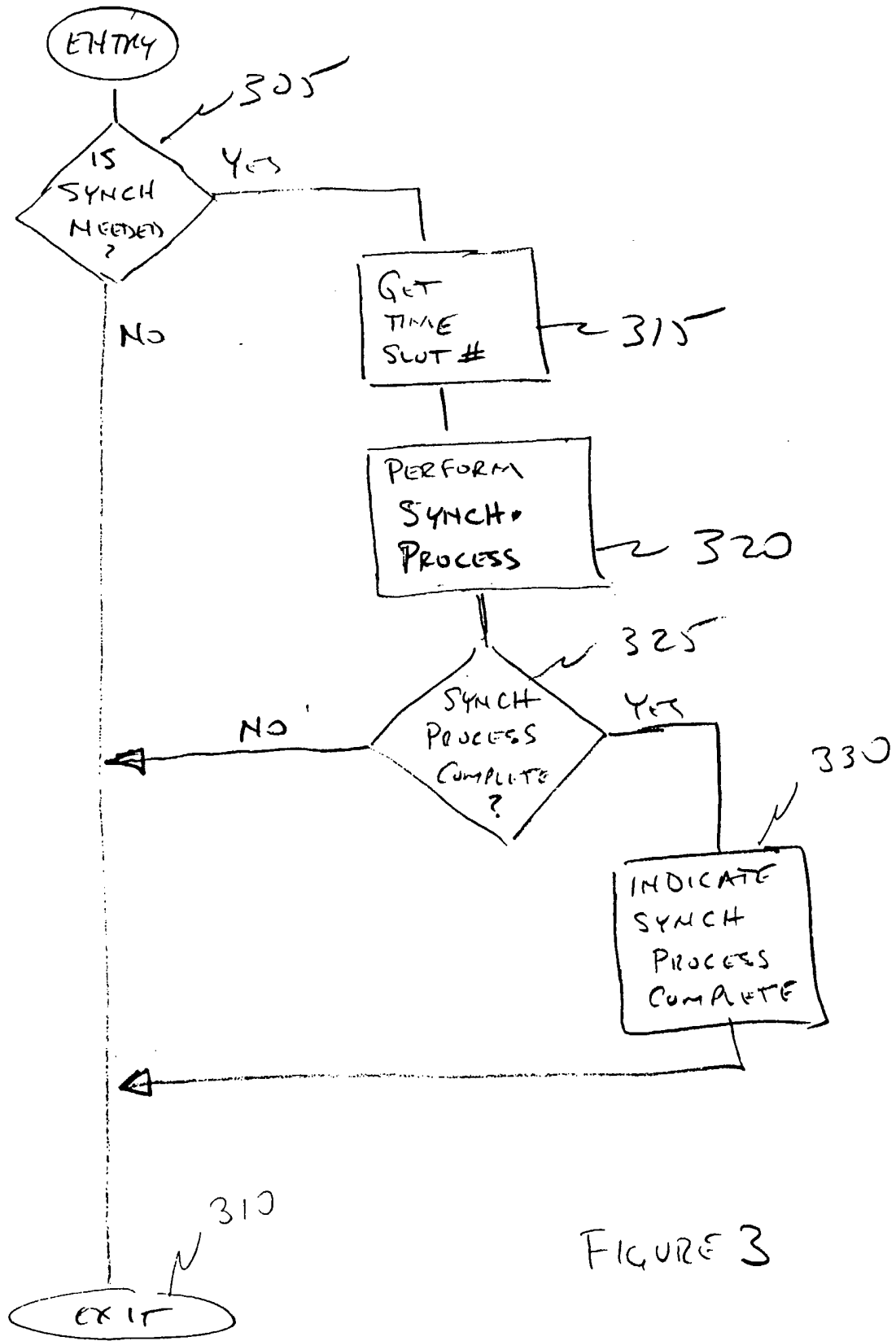


FIGURE 3

400

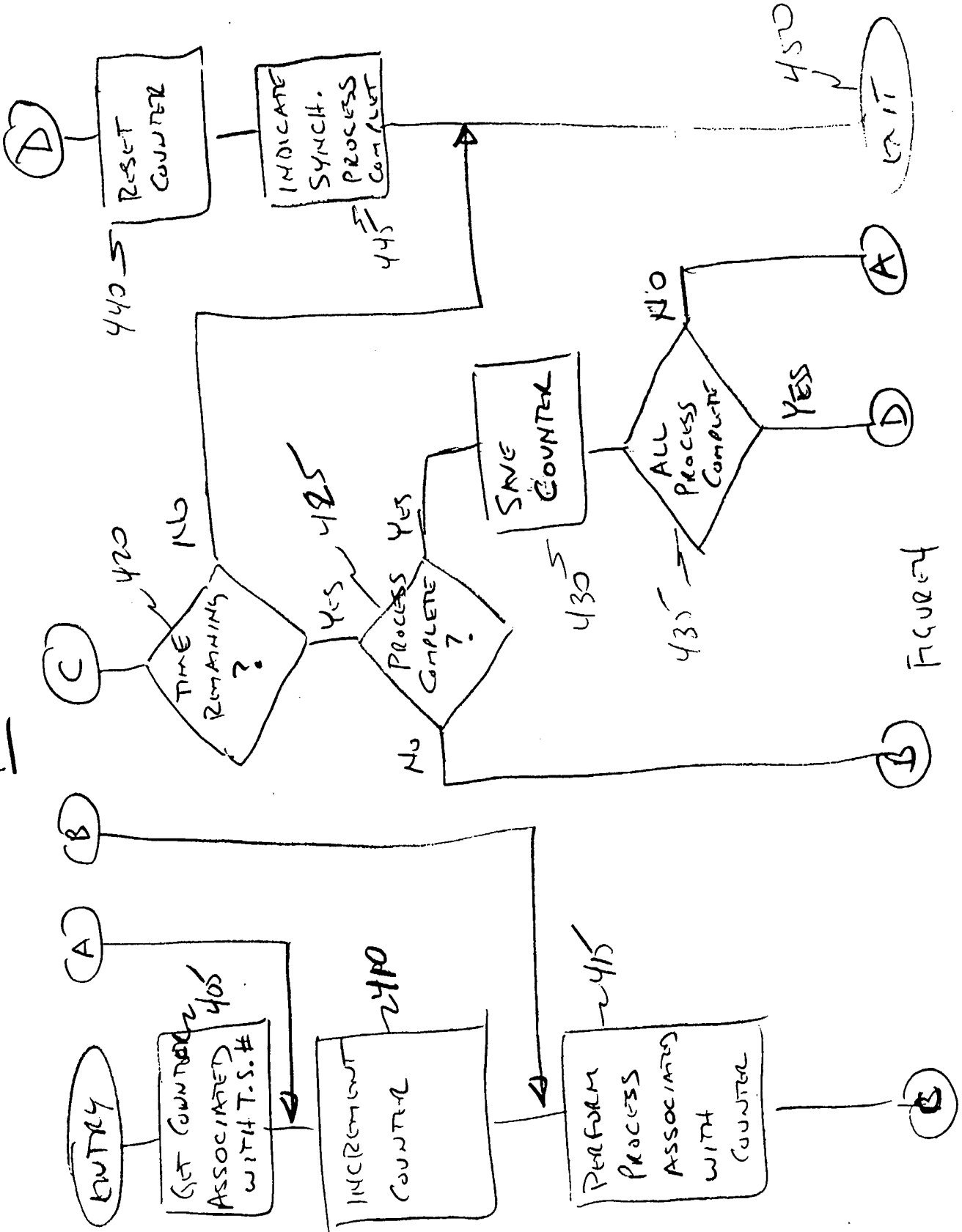


FIGURE 4

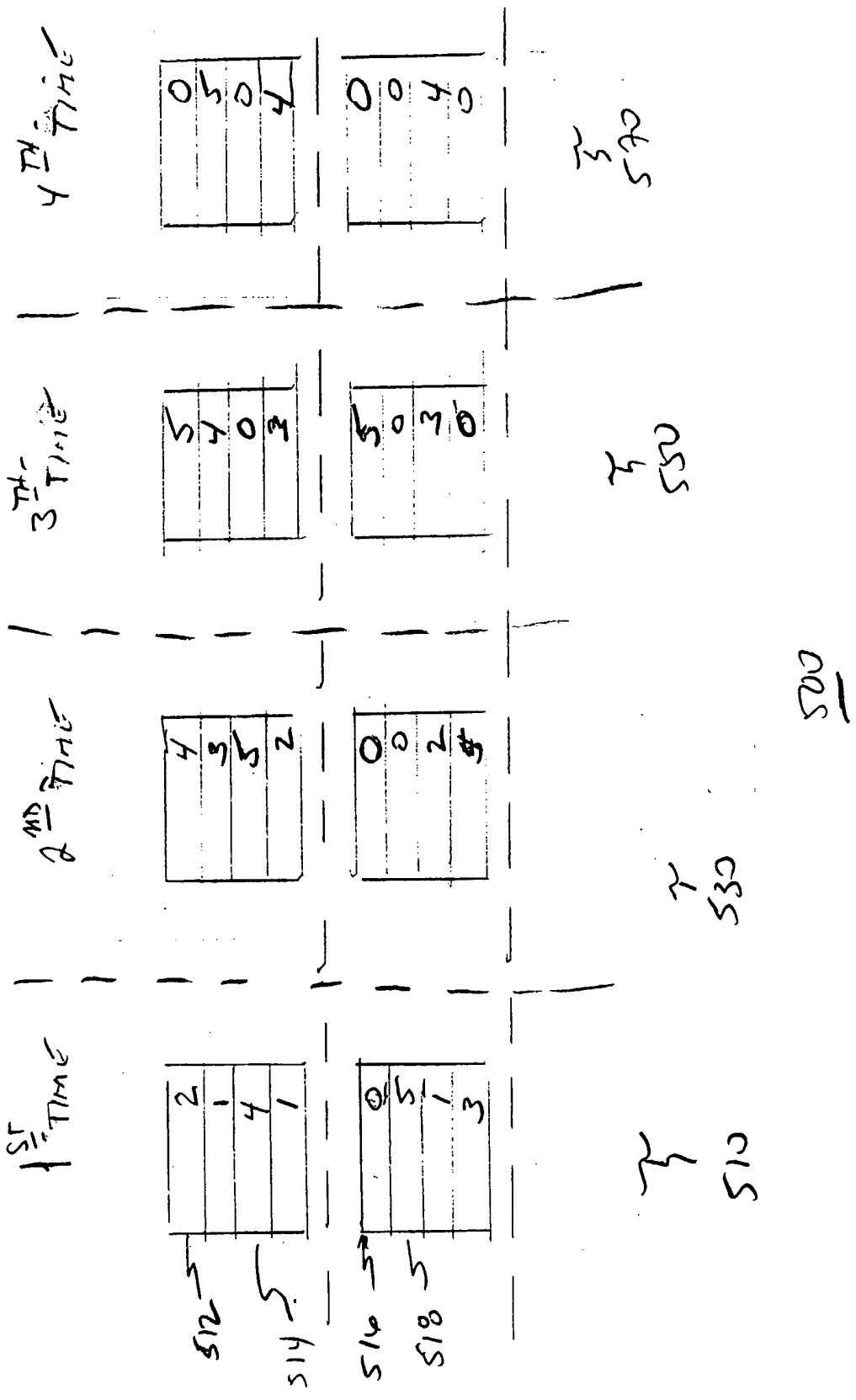


FIGURE 5

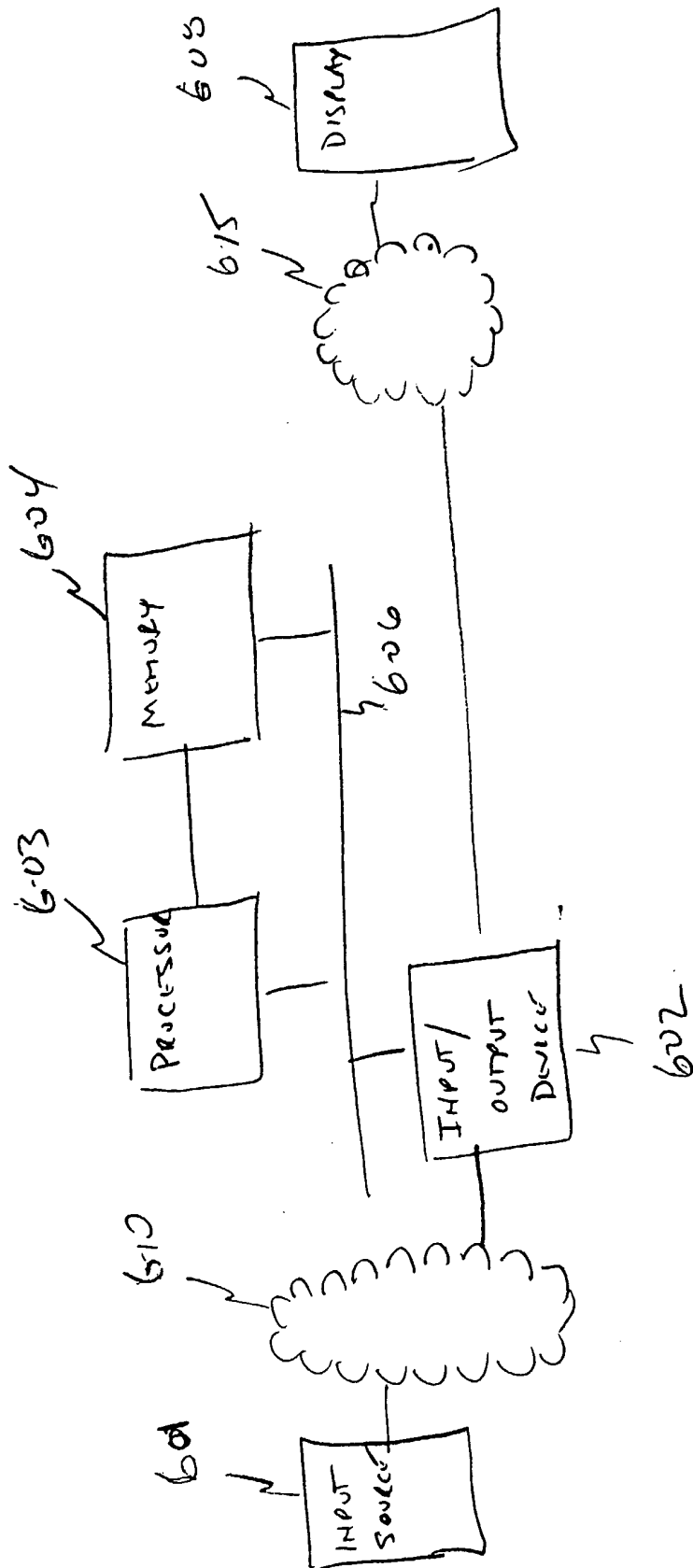


FIGURE 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/03198

A. CLASSIFICATION OF SUBJECT MATTER
 IPC(7) : H04J 3/00 3/06 3/07
 US CL : 370/498, 503-516
 According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
 Minimum documentation searched (classification system followed by classification symbols)
 U.S. : 370/498, 503-516

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
 EAST: synchronization, tdm, tdma, counter, reset modulo, demodulator, time slot, timeslot

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,809,009 A (MATSUOKA et al) 15 September 1998, ALL	1 - 3 , 5 , 6 , 12 - 14 , 16 , 17 , 21, 26, 27
Y	US 5,768,269 A (RAKIB et al) 16 June 1998, ALL	1-3,5,6,8,9 ,11-14, 16, 17, 19-22, 26, 27
Y	US 5,072,445 A (NAWATA) 10 December 1991, ALL	1,3,5,6,8,9,11-14, 16, 17, 19-22, 26, 27

Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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