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(54) **Title**: APPARATUS AND METHOD FOR CONTROLLING POWER SUPPLY START-UP IN A DEVICE

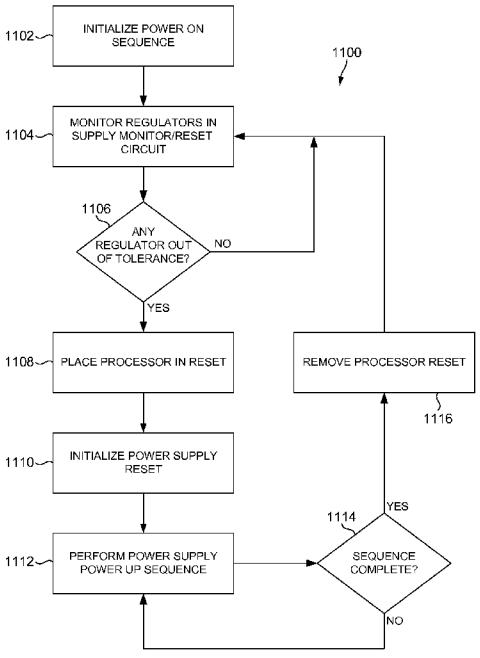

FIG. 11

(57) **Abstract**: An apparatus and method for controlling a power supply start-up in a device (400, 600) are provided herein. The present disclosure is directed at improving the operation of a device (400, 600), such as a settop box, gateway device, or the like, in the event that one or more of the power supply circuits (426) in the device (400, 600) suffers a temporary disturbance preventing proper supply voltages from being supplied to the remaining circuitry (416, 616) in the device (400, 600). The method and system of the present disclosure will detect a condition where one of a plurality of power supplies (426) providing power to critical circuitry (416, 616) of a device (400, 600) has fallen out of proper regulation, for example, due to an anomalous AC power condition, (such as an AC line power dropout) and a reset condition will be initiated just as if the user had powered up the device (400, 600) or pressed the reset button (504, 704).

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APPARATUS AND METHOD FOR CONTROLLING POWER SUPPLY START-UP IN A DEVICE

REFERENCE TO RELATED PROVISIONAL APPLICATION

This application claims priority from United States Provisional Application No. 62/062404, entitled "Apparatus and Method For Controlling Power Supply Start-Up in a Device" filed on October 10, 2014, the contents of which are hereby incorporated by reference in its entirety.

TECHNICAL FIELD

The present disclosure generally relates to operation of a power supply in a device, such as a communication device that includes circuits for receiving signals from a plurality of sources. More particularly, the present disclosure is related to an apparatus and method for controlling a power supply start-up in a device.

BACKGROUND

Any background information described herein is intended to introduce the reader to various aspects of art, which may be related to the present embodiments that are described below. This discussion is believed to be helpful in providing the reader with background information to facilitate a better understanding of the various aspects of the present disclosure. Accordingly, it should be understood that these statements are to be read in this light.

Many home entertainment devices not only include the capability to communicate with other devices in a home network but also include the ability to receive and/or process available media content from a plurality of sources, including a plurality of providers. The sources and providers may include, but are not limited to, satellite service, cable service, and free to home over the air terrestrial service. The services may operate in the same or different frequency ranges and may use the same or different transmission formats or protocols. The devices for receiving the services often include, but are not limited to, settop boxes, gateways, televisions,

home computers, and the like. Further, many of these devices may include multiple interfaces for different types of externally provided services as well as different types of home networks. These devices may also include additional features internal to the device, such as storage elements, hard drives, compact disk or digital versatile disk drives, and the like.

These home entertainment devices may include power supply circuitry used to power a number of the different circuits and functions. Very often, the circuits or functions may use more than one power supply voltage and may further require a particular arrangement or timing structure for starting up or powering up the circuit or function.

Typically, the particular arrangement or timing structure for starting or powering up the circuit may be controlled using one of two methods. First, when the unit is first powered on, a power-on reset (POR) sequence may be followed, which guarantees the supply voltages come up in the right order and are stable before the processor or other critical circuitry in the device is allowed to begin execution and function. Second, a user-initiated reset may be initiated by a user pressing a button, such as a red reset button, located on the unit. The second method is often referred to as a “red-button reset” (RBR).

However, in some cases, one or more of the power supply circuits may suffer a temporary disturbance preventing proper supply voltages from being supplied to the remaining circuitry in the home entertainment device. For example, a momentary change in the mains supply, also referred to as an alternating current (AC) line dropout, may occur. AC line dropouts may take any form of amplitude level and duration of time. Certain amplitude levels or time durations may be sufficient to cause one or more of the power supplies in the device to drop out of tolerance. Although the power supply circuits return to proper operation, a processor circuit or other circuit that is sensitive to the order in which the power supply circuit supplies power may not return to proper operation. As a result, the device may fail to continue to properly operate, or may lock up. The user may not be able to determine why the device is not operating properly. The user will be forced to first try to determine why

the device is not operating properly. The user may then choose to unplug the device from the AC mains to begin a POR or to perform an RBR. In either case, the user must initiate an action. Therefore, there is a need for a better mechanism for handling power supply disturbances in devices using power supply sensitive circuits.

SUMMARY

According to one aspect of the present disclosure, a method is provided including providing electrical power to a processing circuit, the processing circuit coupled to a plurality power supplies and requiring a start up sequence for the plurality of power supplies, determining if one of the plurality of power supplies is not properly operating while at least one other of the plurality of power supplies is properly operating, generating a first reset signal if it is determined that the one of the plurality of power supplies is not properly operating while the at least one other of the plurality of power supplies is properly operating, and providing the first reset signal to the processor circuit causing the processor circuit to enter a reset condition and to the plurality of power supplies to cause a proper start up sequence for the plurality of power supplies.

According to another aspect of the present disclosure, an apparatus is provided that includes a processing circuit coupled to a plurality power supplies, the processing circuit requiring a start up sequence for the plurality of power supplies; and a power supply monitoring circuit that determines if one of the plurality of power supplies is not properly operating while at least one other of the plurality of power supplies is properly operating, generates a first reset signal if it is determined that the one of the plurality of power supplies is not properly operating while the at least one other of the plurality of power supplies is properly operating, the power supply monitoring circuit further providing the first reset signal to the processor circuit causing the processor circuit to enter a reset condition and providing the first reset signal to the plurality of power supplies to cause a proper start up sequence for the plurality of power supplies.

BRIEF DESCRIPTION OF THE DRAWINGS

These, and other aspects, features and advantages of the present disclosure will be described or become apparent from the following detailed description of the preferred embodiments, which is to be read in connection with the accompanying drawings.

FIG. 1 is a block diagram of an exemplary signal receiving system in a home or dwelling in accordance with the present disclosure;

FIG. 2 is a block diagram of another exemplary signal receiving system including a signal receiving device in accordance with the present disclosure;

FIG. 3 is a block diagram of an exemplary network device in accordance with the present disclosure;

FIG. 4 is a block diagram of an exemplary settop box in accordance with an embodiment of the present disclosure;

FIG. 5 is a block diagram of an exemplary power supply circuit in accordance an embodiment of the present disclosure;

FIG. 6 is a block diagram of an exemplary settop box in accordance with another embodiment of the present disclosure;

FIG. 7 is a block diagram of exemplary power supply circuit in accordance with another embodiment of the present disclosure;

FIG. 8 is a schematic of a power supply circuit used in a device in accordance with an embodiment of the present disclosure;

FIGs. 9a and 9b are a schematic of a power supply circuit used in a device in accordance with another embodiment of the present disclosure;

FIGs. 10a and 10b are a schematic of a power supply circuit used in a device in accordance with another embodiment of the present disclosure;

FIG. 11 is a flow chart illustrating a process for controlling a power supply startup in a device in accordance with an embodiment of the present disclosure.

It should be understood that the drawing(s) are for purposes of illustrating the concepts of the disclosure and is not necessarily the only possible configuration for illustrating the disclosure.

DESCRPTION OF EMBODIMENTS

It also should be understood that the elements shown in the figures may be implemented in various forms of hardware, software or combinations thereof. Preferably, these elements are implemented in a combination of hardware and software on one or more appropriately programmed general-purpose devices, which may include a processor, memory and input/output interfaces. Herein, the phrase "coupled" is defined to mean directly connected to or indirectly connected with through one or more intermediate components. Such intermediate components may include both hardware and software based components.

The present description illustrates the principles of the present disclosure. It will thus be appreciated that those skilled in the art will be able to devise various arrangements that, although not explicitly described or shown herein, embody the principles of the disclosure and are included within its scope.

All examples and conditional language recited herein are intended for educational purposes to aid the reader in understanding the principles of the disclosure and the concepts contributed by the inventor to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions.

Moreover, all statements herein reciting principles, aspects, and embodiments of the disclosure, as well as specific examples thereof, are intended to encompass both structural and functional equivalents thereof. Additionally, it is intended that such equivalents include both currently known equivalents as well as equivalents developed in the future, i.e., any elements developed that perform the same function, regardless of structure.

Thus, for example, it will be appreciated by those skilled in the art that the block diagrams presented herein represent conceptual views of illustrative circuitry embodying the principles of the disclosure. Similarly, it will be appreciated that any flow charts, flow diagrams, state transition diagrams, pseudocode, and the like represent various processes which may be substantially represented in computer readable media and so executed by a computer or processor, whether or not such computer or processor is explicitly shown.

The functions of the various elements shown in the figures may be provided through the use of dedicated hardware as well as hardware capable of executing software in association with appropriate software. When provided by a processor, the functions may be provided by a single dedicated processor, by a single shared processor, or by a plurality of individual processors, some of which may be shared. Moreover, explicit use of the term “processor” or “controller” should not be construed to refer exclusively to hardware capable of executing software, and may implicitly include, without limitation, digital signal processor (DSP) hardware, read only memory (ROM) for storing software, random access memory (RAM), and nonvolatile storage.

Other hardware, conventional and/or custom, may also be included. Similarly, any switches shown in the figures are conceptual only. Their function may be carried out through the operation of program logic, through dedicated logic, through the interaction of program control and dedicated logic, or even manually, the particular technique being selectable by the implementer as more specifically understood from the context.

In the claims hereof, any element expressed as a means for performing a specified function is intended to encompass any way of performing that function including, for example, a) a combination of circuit elements that performs that function or b) software in any form, including, therefore, firmware, microcode or the like, combined with appropriate circuitry for executing that software to perform the function. The disclosure as defined by such claims resides in the fact that the functionalities provided by the various recited means are combined and brought together in the manner which the claims call for. It is thus regarded that any means that can provide those functionalities are equivalent to those shown herein.

The present disclosure is directed at improving the operation of a device, such as a settop box, gateway device, or the like, in the event that one or more of the power supply circuits in the device suffers a temporary disturbance preventing proper supply voltages from being supplied to the remaining circuitry in the device. Typically, two main mechanisms are available to assure proper recovery from a temporary disturbance, such as an AC line dropout, to the power supply circuits. The first mechanism occurs when the device is first powered on or when the device is first plugged in and is referred to as a power-on reset (POR). The second mechanism is a user initiated reset that occurs when a user presses a red reset button located on the device. The user initiated reset is referred to as a red-button reset (RBR). An RBR effectively operates as a POR. Neither of these mechanisms offers an automatic mechanism that does not require user interaction in the event that only one or some of the power supply circuits suffer a temporary disturbance. An automatic mechanism is even more important when one or more of the remaining circuits in the device are sensitive to the level or the timing of the power supply circuit operational conditions.

Described herein are mechanisms for implementing a method and system to initiate an automatic RBR when one of a plurality of power supplies supplying power to critical circuitry within a device has fallen out of proper regulation. The method and system of the present disclosure will detect a condition where one of a plurality of power supplies providing power to critical circuitry has fallen out of proper regulation, for example, due to an anomalous alternating current (AC) power condition, (such as

an AC line power dropout) and an RBR will be initiated just as if the user had powered up the device or pressed the red reset button. The automatic RBR will ensure that any necessary operational conditions for critical circuitry within a device are satisfied, and any potential damage that may be caused due to anomalous AC power condition is prevented.

Turning now to the drawings and referring initially to FIG. 1, a block diagram of an embodiment of a system 100 for providing home entertainment media content in a home, or end user, network is shown. The media content, originating from a content provider, is provided through an external network to a Multimedia over Cable Alliance (MoCA) interface 110. The media content may be provided using any one of the standard transmission protocols and standards for content delivery (e.g., Advanced Television Systems Committee (ATSC) A/53, digital video broadcast (DVB)-Cable (DVB-C), DVB-Satellite (DVB-S), or DVB-Terrestrial (DVB-T)). MoCA interface 110 is connected to external network receiving device 120, external network receiving device 130, and MoCA network device 140. Both external network receiving device 120 and external network receiving device 130 connect to local network interface 150. Local network interface 150 connects to local network device 160. Media content playback device 170 connects to MoCA network device 140. MoCA network device 140 connects to display device 180. The components shown in system 100 comprise a home network configured to provide media content to multiple locations within the home using one or more home communication networks.

A signal containing media content (e.g., audio, video, and/or data) from the external network is provided over a physical media, such as co-axial cable. The external network interfaces to MoCA interface 110. MoCA interface 110 provides a routing mechanism for the signal from the external network to devices in the home or user network (e.g., external network receiving device 120 and external network receiving device 130) in conjunction with signals that operate in the MoCA network with the home or user network. MoCa interface 110 may include active or passive circuit elements that may split or separate the input signal into different or similar output signals. MoCa interface 110 may use amplifiiers, frequency filters, and electromagnetic circuits to split or separate the signal. In one embodiment, the

external network provides a signal on a co-axial cable between the frequency range of 20 Megahertz (MHz) and 800 MHz. The MoCA network operates using signals in the frequency range from 950 MHz to 1,250 MHz. In an alternative embodiment, the external network provides a signal between the frequency range of 950 MHz and 2,150 MHz with the MoCA network operating in the frequency range of 425 MHz to 625 MHz. MoCA interface 110 provides a signal splitting for signals from the external network and a separate signal splitting for signals on the MoCA network while preventing signals from the MoCA network from being output to the external network.

External network receiving device 120 and external network receiving device 130 may each operate and function in a similar manner. External network receiving device 120 and external network receiving device 130 receive the signal from the external network through the MoCA interface 110. External network receiving device 120 and external network receiving device 130 may receive different types of media content (e.g., different channels) from either the external network or from other devices in the home network through either MoCA interface 110 or local network interface 150. External network receiving devices 120 and 130 tune, demodulate, decode, and process the received content. External network devices 120 and 130 also provide the processed content for display and use by a user in the home. External network receiving devices 120 and 130 may further provide a separation of the media content based on instructions provided with the content or over the external network. External network receiving devices 120 and 130 may also process and separate media content based on instructions received via user commands. External network receiving devices 120 and 130 may also provide storage, such as a hard drive or optical disk drive, for recording and/or storing the media content as well as providing the content for playback to other devices in a home network (e.g., MoCA network device 140 and local network device 160). The operation and function of an external network receiving device, such as discussed here, will be described in further detail below. External network receiving devices 120 and 130 may be one of a settop box, home media server, computer media station, home network gateway, multimedia player, modem, router, home network appliance, or the like.

External network receiving devices 120 and 130 provide interfaces for communicating signals on the MoCA network through MoCA interface 110 to and from other MoCA network devices (e.g., external network receiving devices 120 and 130 and MoCA network device 140). External network receiving devices 120 and 130 also provide interfaces to a local home network through local network interface 150 to local network device 160. In one embodiment, the local network is an Ethernet network. In addition, the local network may be a wireless network. Wireless communication using a wireless network may include physical interfaces to accommodate one or more wireless formats including Wi-Fi, Institute of Electrical and Electronics Engineers (IEEE) standard 802.11 or other similar wireless communications protocols.

MoCA interface 110 provides MoCA network signals between external network receiving device 120, external network receiving device 130, and MoCA network device 140. MoCA network device 140 tunes, demodulates, and decodes MoCA signals for display and use by a user. MoCA network device 140 may also transmit or communicate signals on the MoCA network for delivery to other devices (e.g., external network receiving device 120 or 130). These signals may provide control or identification information for media content to be delivered to the MoCA network device 140. The MoCA network device 140 is often referred to as a thin client MoCA device and may be, but is not limited to, a settop box, setback box, computer device, tablet, display device, television, wireless phone, personal digital assistant (PDA), gaming platform, remote control, multi-media player, or home networking appliance that includes a MoCA interface, and may further include a storage media for digital video recording. MoCA network device 140 may also include a storage device, such as a hard drive or optical disk drive, for recording and playing back audio and video content.

Local network interface 150 provides the routing and signal communication and management functions between devices communicating across the local network. In one embodiment, local network interface 150 operates as a signal router for communicating using internet protocol routing protocols as part of an Ethernet network.

Local network interface 150 provides local network signals between external network receiving device 120, external network receiving device 130, and local network device 160. Local network device 160 also may tune, demodulate, and/or decode the local network signals for display and use by a user depending on the communication protocol used. Local network device 160 may also transmit or communicate signals on the local network for delivery to other devices (e.g., external network receiving device 120 or 130). These signals may provide control or identification information for media content to be delivered to the local network device 160. The local network device 160 is often referred to a thin client device and may be, but is not limited to, a computer device, tablet, display device, television, wireless phone, personal digital assistant (PDA), gaming platform, remote control, multi-media player, or home networking appliance that includes a local network interface. Local network device 160 may further include a storage media for digital media recording.

Media content playback device 170 provides local source playback for one or more formats of media content from an internal or separate media element. Media content playback device 170 may include a compact disc (CD) drive, DVD drive, Blu-Ray drive, a hard disk drive, an electronic memory, or other storage or storage access element. Media content playback device 170 reads the media content from the media element and outputs the media content in one or more audio/video signal formats (e.g., HDMI). The audio/video signals are provided to MoCA network device 140.

Display device 180 receives and displays audio/video signals from the MoCA network device 140. The audio/video signals may either be from media content playback device 170 or may be from external network receiving devices 120 and 130 through MoCA interface 110. Display device 180 may be a conventional two-dimensional (2-D) type display or may alternatively be an advanced three-dimensional (3-D) type display.

It is important to note that external network receiving devices 120 and 130 and local network device 160 may include display capability or may be connected an

external display device, not shown. Further, external network receiving devices 120 and 130 and local network device 160 may include interfaces for connecting a media content playback device, such as media content playback device 170. It should be appreciated that other devices having display capabilities including, but not limited to, computer devices, tablets, gateways, display devices, televisions, wireless phones, PDAs, computers, gaming platforms, remote controls, multi-media players, home networking appliances or the like, may employ the teachings of the present disclosure and are considered within the scope of the present disclosure.

In operation, system 100 provides the networking and communication capability for connecting and sharing media content between devices in a user's home using either the MoCA network, or the local network, or both networks. In one embodiment, media content for a particular program is tuned by external network receiving device 120 and provided to MoCA network device 140 through MoCA interface 110 for viewing on display device 180. MoCA network device 140 may operate using a frequency range described as high MoCA. As the other devices, such as external device receiving device 120 and 130, share the network, other signals, such as single wire multiswitch (SWM) communication, Integrated Services Digital Broadcasting-Terrestrial (ISDB-T), and L-band satellite signals, may be present and must operate unimpaired by the operation of MoCA network device 140. As a result, MoCA network device 140 needs to have impedance terminations for signals in the other frequency ranges.

It should be appreciated by one skilled in the art that system 100 in FIG. 1 is described primarily as operating with a local MoCA network and a second local network, such as an Ethernet network. However, other network standards that incorporate either a wired or wireless physical interface may be used. For example, the second local network may be a wireless network using WiFi, Bluetooth, or IEEE 802.11. Other wired networks, such as phone line or power line networks, may be used in place of the MoCA network. Further, more than two networks may be used either alternatively or simultaneously together.

Turning now to FIG. 2, another exemplary signal receiving system 200 using aspects of the present disclosure is shown. System 200 primarily receives signals from one or more satellites as well as multiple television broadcast transmission sites. The signals are provided by one or more service providers and represent broadcast audio and video programs and content. System 200 is described as including components that reside both inside and outside a user's premises. It is important to note that one or more components in system 200 may be moved from inside to outside the premises. Further, one or more components may be integrated with a display device, such as a television or display monitor (not shown). In either case, several components and interconnections necessary for complete operation of system 200 are not shown in the interest of conciseness, as the components not shown are well known to those skilled in the art.

An outdoor unit (ODU) 201 receives signals from satellites and from terrestrial transmission towers through an over the air and/or near earth orbit communications link. ODU 201 is connected to settop box 202. Within settop box 202, the input is connected to filter 203. Optionally, filter 203 can be connected to splitter 204. Filter 203 is coupled to three signal processing paths. A first path includes tuner 205, link circuit 206, and transport decoder 208 connected together serially. A second path includes tuner 210, link circuit 212, and transport decoder 214 connected together serially. A third path includes MoCA circuit 234 which further connects to controller 216. The outputs of transport decoder 208 and transport decoder 214 each connect to controller 216. Controller 216 connects to security interface 218, external communication interface 220, user panel 222, remote control receiver 224, audio/video output 226, power supply 228, memory 230, and ODU control 232. External communication interface 220, remote control receiver 224, audio/video output 226, and power supply 228 provide external interfaces for the settop box 202. ODU control 232 also connects to the filter 203.

Satellite signal streams, each containing a plurality of channels, are received by ODU 201. ODU 201 includes a dish for capturing and focusing the propagated radio wave from the atmosphere onto one or more antennas contained within a structure known as a low noise block converter (LNB). ODU 201 may be configured to receive the signal streams from satellite transponders located on one or more

satellites. In a preferred embodiment, two sets of sixteen channels are received by ODU 201, and converted, using one or more LNBs to a frequency range of 950 Megahertz (MHz) to 2,150 MHz, referred to as L-band. ODU 201 also includes a terrestrial antenna for receiving over the air broadcasts. In a preferred embodiment, ODU 201 includes a multiple element antenna array for receiving ISDB-T signals in the frequency range from 170 MHz to 800 MHz.

ODU 201 provides a converted signal stream to the settop box 202 through radio frequency (RF) co-axial cable. The converted signal stream is provided to filter 203. In a preferred embodiment, filter 203 operates as a multiplex filter with up to three separate filter sections or interfaces. The frequency response properties of filter 203 may include a separate highpass filter and lowpass filter such that the frequency passbands of each do not overlap. The arrangement, often referred to as a diplexer or diplex filter, allows for a separation, through signal filtering, of the incoming satellite signal and/or MoCA signal from the terrestrial signal and/or MoCA signal. In a preferred embodiment, the low pass filter frequency response pass band ends at a frequency below 900 MHz. The low pass filter portion allows a MoCA signal in a frequency range from 475 MHz to 625 MHz as well as a terrestrial signal in the frequency range from 170 MHz to 800 MHz to pass through to subsequent blocks while attenuating, or not passing through, a satellite signal in a frequency range from 950 MHz to 2,150 MHz. The high pass filter portion operates in an opposite manner passing the MoCA signal in the frequency range around 1100 MHz, along with the satellite signal, through and attenuating cable or terrestrial broadcast signal. The high pass filter portion may also filter any electrical supply or communication signals provided to the ODU 201. An additional bandpass filter circuit may be provided to further process MoCA signals and provide the signals as an output to a home MoCA network or for processing in settop box 202. Other embodiments may be possible and some of these embodiments are described in further detail below. Filter 103 may also include surge or transient voltage protection devices.

The output signal from the high pass filter portion of filter 203 is provided to a first signal path containing a tuner 205, a link circuit 206, and a transport decoder 208 connected in a serial fashion. The output signal from the low pass filter portion of the filter 203 is provided to a second signal path. The second signal path also contains a

tuner 210, a link circuit 212, and a transport decoder 214 connected in a serial fashion. Each processing path may perform similar processing on the filtered signal streams, the processing being specific to the transmission protocol used.

Tuner 205 processes the split signal stream by selecting or tuning one of the channels provided from a satellite service provider in the highpass filtered signal stream to produce one or more baseband signals. Tuner 205 contains circuits (e.g., amplifiers, filters, mixers, and oscillators) for amplifying, filtering and frequency converting the satellite signal stream. Tuner 205 typically is controlled or adjusted by link circuit 206. Alternately, tuner 205 may be controlled by another controller, such as controller 216, which will be described later. The control commands include commands for changing the frequency of an oscillator used with a mixer in tuner 205 to perform the frequency conversion.

Tuner 210 processes the lowpass filtered signal stream by selecting or tuning one of the terrestrial or cable broadcast channels in the split signal stream to produce one or more baseband signals. Tuner 210 contains circuits (e.g., amplifiers, filters, mixers, and oscillators) for amplifying, filtering and frequency converting the signal stream. Tuner 210 may be controlled or adjusted in a manner similar to that described earlier for tuner 205.

Typically, the baseband signals at the output of tuner 205 or tuner 210 may collectively be referred to as the desired received signal and represent one satellite channel selected out of a group of channels that were received as the input signal stream. Although the signal is described as a baseband signal, this signal may actually be positioned at a frequency that is only near to baseband.

The one or more baseband signals from the satellite service provider are provided to link circuit 206 through tuner 205. Link circuit 206 typically contains the processing circuits needed to convert the one or more baseband signals into a digital signal for demodulation by the remaining circuitry of link circuit 206. In one embodiment, the digital signal may represent a digital version of the one or more baseband signals. In another embodiment, the digital signal may represent the vector form of the one or more baseband signals. Link circuit 206 also demodulates

and performs error correction on the digital signal from the satellite service provider to produce a transport signal. The transport signal may represent a data stream for one program, often referred to as a single program transport streams (SPTS), or it may represent multiple program streams multiplexed together, referred to as a multiple program transport stream (MPTS).

The one or more baseband signals from the broadcast service provider are provided to link circuit 212 through tuner 210. Link circuit 212 typically contains the processing circuits needed to convert the one or more baseband signals into a digital signal for demodulation by the remaining circuitry of link circuit 212 in a manner similar to link circuit 206 described earlier. Link circuit 212 also demodulates, performs broadcast channel equalization error correction on the digital signal from the broadcast service provider to produce a transport signal. As described earlier, the transport signal may represent a data stream for one program or it may represent multiple program streams multiplexed together.

The transport signal from link circuit 206 is provided to transport decoder 208. Transport decoder 208 typically separates the transport signal, which is provided as either a SPTS or MPTS, into individual program streams and control signals. Transport decoder 208 also decodes the program streams, and creates audio and video signals from these decoded program streams. In one embodiment, transport decoder 208 is directed by user inputs or through a controller such as controller 216 to decode only the one program stream that has been selected by a user and create only one audio and video signal corresponding to this one decoded program stream. In another embodiment, transport decoder 208 may be directed to decode all of the available program streams and then create one more audio and video signals depending on user request.

The transport signal from link circuit 212 is similarly provided to transport decoder 214. Transport decoder 214 decodes the program streams, and creates audio and video signals from these decoded program streams as directed by user inputs or a controller in a manner similar to that described earlier for transport decoder 208.

The audio and video signals, along with any necessary control signals, from both transport decoder 208 and transport decoder 214 are provided to controller 216. Controller 216 manages the routing and interfacing of the audio, video, and control signals and, further, controls various functions within settop box 202. For example, the audio and video signals from transport decoder 208 may be routed through controller 216 to an audio/video (A/V) output 226. A/V output 226 supplies the audio and video signals from settop box 202 for use by external devices (e.g., televisions, display monitors, and computers). Also, the audio and video signals from transport decoder 214 may be routed through controller 216 to memory block 230 for recording and storage.

Memory block 230 may contain several forms of memory including one or more large capacity integrated electronic memories, such as static random access memory (SRAM), dynamic RAM (DRAM), or hard storage media, such as a hard disk drive or an interchangeable optical disk storage system (e.g., compact disk drive or digital video disk drive). Memory block 230 may include a memory section for storage of instructions and data used by controller 216 as well as a memory section for audio and video signal storage. Controller 216 may also allow storage of signals in memory block 230 in an alternate form (e.g., an MPTS or SPTS from transport decoder 208 or transport decoder 214).

Controller 216 is also connected to an external communications interface 220. External communication interface 220 may provide signals for establishing billing and use of the service provider content. External communications interface 220 may include a phone modem for providing phone connection to a service provider. External communications interface 220 may also include an interface for connection to an Ethernet network and/or to home wireless communications network. The Ethernet network and/or home wireless network may be used for communication data, audio, and/or video signals and content to and from other devices connected to the Ethernet network and/or home wireless network (e.g., other media devices in a home).

Controller 216 also connects to a security interface 218 for communicating signals that manage and authorize use of the audio/video signals and for preventing

unauthorized use. Security interface 218 may include a removable security device, such as a smart card. User control is accomplished through user panel 222, for providing a direct input of user commands to control the settop box and remote control receiver 224, for receiving commands from an external remote control device. Although not shown, controller 216 may also connect to the tuners 205, 210, link circuits 206, 212, and transport decoders 208, 214 to provide initialization and set-up information in addition to passing control information between the blocks. Finally, power supply 228 typically connects to all of the blocks in settop box 202 and supplies the power to those blocks as well as providing power to any of the elements needing power externally, such as the ODU 201.

Controller 216 also controls ODU control 232. ODU control 232 provides signaling and power supply electrical power back to the ODU 201 through filter 203. ODU control 232 provides these signals and power onto the co-axial cable(s) running between ODU 201 and settop box 202. In one embodiment, the ODU control 232 receives input control signals from controller 216 and provides different direct current (DC) voltage levels to specific portions of the ODU 201 to provide a certain signal stream containing a set of programs or content to filter 203 and further to tuner 205 and tuner 210. In another embodiment, the ODU control 232 receives inputs from controller 216 and also from link circuit 206 and link circuit 212 and provides DC voltage levels and a separate tuning control signal to ODU 201 using low frequency carrier based frequency shift keying modulation or using SWM format. Controller 216 also may send control commands to disable ODU controller 230 from providing either DC voltages or control signals to ODU 201.

MoCA circuit 234 amplifies and processes the MoCA signal both for reception and transmission. As described above the MoCA interface permits communications of audio and video signals in a home network and may operate bi-directionally. MoCA circuit 234 includes a low noise amplifier for improving reception performance of a MoCA signal received by signal receiving device 200 from another network connected device. The received and amplified signal is tuned, demodulated, and decoded. The decoded signal may be provided to a number of other circuits, including audio and video outputs as well as a mass storage device (e.g., hard disk drive, optical drive, and the like), not shown. Additionally, MoCA circuit 234

generates and formats the MoCA transmit signal using audio and video content available in signal receiving device, including content received from the input (e.g., satellite signal) and content from the mass storage device. MoCA circuit 234 also includes a power amplifier for increasing the transmitted signal level of the MoCA signal sent by system 200 to another network connected device. Adjustment of the receive signal amplification as well as the transmit signal amplification in MoCA circuit 234 may be controlled by controller 216.

It should be appreciated by one skilled in the art that the blocks described inside settop box 202 have important interrelations, and some blocks may be combined and/or rearranged and still provide the same basic overall functionality. For example, transport decoder 208 and transport decoder 214 may be combined and further integrated along with some or all of the functions of controller 216 into a System on a Chip (SoC) that operates as the main controller for settop box 202. Further, control of various functions may be distributed or allocated based on specific design applications and requirements. As an example, link circuit 206 may provide control signals to ODU control 232 and no connection may exist between link circuit 212 and ODU control 232.

Further, it should be appreciated although ODU 201 includes both a dish and LNB for use with satellite signals and a terrestrial antenna, other embodiments may use separate structures. In some embodiments, the satellite dish and LNB and included in one structure and the terrestrial antenna is part of a second structure. The outputs of both satellite dish/LNB structure and terrestrial antenna are combined using a signal combining circuit and provided to settop box 202.

Although settop box 202 is described above as receiving a single converted signal stream, settop box 202 may also be configured to receive two or more separate converted signal streams supplied by ODU 201 in some modes of operation. Operation in these modes may include additional components including switches and/or further tuning and signal receiving components, not shown. Further, settop box 202 may be designed to operate only on a home network using the Ethernet or home wireless network interfaces described above. In this case, the

elements associated with operation in a MoCA network may be removed from settop box 202.

Turning now to FIG. 3, a block diagram of an exemplary network device 300 using aspects of the present disclosure is shown. Network device 300 operates in a manner similar to MoCA network device 140 described in FIG. 1. Network device 300 primarily operates on a home network. It is important to note that one or more components may be integrated with a display device, such as a television or display monitor (not shown). In either case, several components and interconnections necessary for complete operation of network device 300 are not shown in the interest of conciseness, as the components not shown are well known to those skilled in the art.

A signal from an internal or home network (e.g., MoCA network), is interfaced to network device 300 at filter 303. Filter 303 connects to MoCA front end 333. MoCA front end 333connects to MoCA transceiver 334. MoCA transceiver 334 further connects to controller 316. Controller 316 connects to security interface 318, external communication interface 320, user panel 322, remote control receiver 224, audio/video output 326, power supply 328, and memory 330. External communication interface 320, remote control receiver 324, audio/video output 326, and power supply 328 provide external interfaces for the settop box 302. Except as described below, the elements in network device 300 operate and function in a manner similar to those similarly numbered elements described for settop 202 described in FIG. 2 and will not be described further here.

The MoCA home network signal, containing audio, video, and/or data program content is received (e.g., settop box 202 described in FIG. 2 or external network receiving device 120 or 130 described in FIG. 1) through a cable (e.g., a coaxial cable) from a central distribution unit and is passed through filter 303. Filter 303 passes the MoCA signal through while attenuating other signals present on the cable. Filter 303 also filters any undesired signals transmitted from MoCA front end 333. MoCA front end 333 includes tuners and amplifiers used for receiving the MoCA signal as well as transmitting a MoCA signal from network device 300 to the home

network. The tuned input signal from RF front end 333 is provided to MoCA transceiver 334. MoCA transceiver 334 demodulates the tuned input signal and provides audio, video, and/or data program content signals to controller 316.

Controller 316 converts the signal received from the MoCA network through MoCA transceiver 334, in a serial Ethernet or reduced gigabit media independent interface (RGMII) format, and may provide the converted signal to other elements in network device 300. Similarly, controller 316 may receive and convert inputs from one or more of the elements in network device 300 and provide the signal to MoCA transceiver 334 for transmission to other devices on the MoCA home network.

As described above, two mechanisms are commonly used to generate a reset for a device, such as settop box 202 described in FIG. 1, network device 300 described in FIG. 3, or at least some of the devices described in FIG. 1. The first mechanism occurs when a device is first powered on. When a device is first powered on, a power-on reset ("POR") is initiated. The POR is configured to guarantee that the device's supply voltages are initiated and are provided to the circuitry in the device in the proper predetermined order. It is important that any critical power supplies are stable when provided to certain circuits, such as processor circuits, before those circuits are allowed to begin execution. The POR is typically only initiated when power (e.g., from the AC mains supply) has not been provided to the device for some period of time.

The other mechanism used to generate a reset in a device is often referred to as a red button reset (RBR). An RBR is a user-initiated reset caused by the user pressing a reset button, often red in color (although the reset button may be any color), located on the device. An RBR may also be initiated by via a user selections in a software application (i.e., user selected a system reset in a user interface). When the user-initiated RBR occurs, the system is required to exhibit the same characteristics as a POR. To ensure the characteristics of a POR (e.g., power has not been provided to the device for some period of time) are achieved, the RBR is configured such that all internal power supplies drop to an initial voltage level (e.g.,

below 0.2V) and then re-initialize in the proper sequence just as though the device had been re-connected to the power source.

A problem may occur when the device is subjected to AC mains supply line dropouts having varying amplitude and duration. In some cases, the dropout is sufficient to cause one or more of the power supplies to temporarily drop out of tolerance. Due to the sensitivity of certain circuitry (e.g., processor circuitry), the dropout and subsequent power supply interruption may cause an unknown operational state resulting in the device becoming inoperable or locking up. Further details related to the embodiments that address these shortcomings will be described below.

Turning to FIG. 4, a block diagram of an exemplary settop box 400 according to principles of the present disclosure is shown. It is to be appreciated that settop box 400 operates in a manner similar to settop 202 described in FIG. 2 and may also operate in a manner similar to external network receiving device 120 or external network receiving device 130 described in FIG. 1.

Settop box 400 includes, among other elements, a power supply circuit 428. Power supply circuit 428 powers the elements of settop box 400. Power supply circuit 428 includes a plurality of power supplies 426 that are provided to at least some of the other circuit elements in settop box 400. For example, the plurality of power supplies 426 may power one or more internal components of processor 416 included in settop box 400. Some of the power supplies included in the plurality of power supplies 426 are power supply 425 (3.3 V), power supply 435 (2.5 V), power supply 445 (1.5 V), power supply 455 (5 V), power supply 465 (1 V), and power supply 475 (1 V). The plurality of power supplies 426 generate power using an input power supply 402 (shown as 12 V DC IN in FIG. 4). Settop box 400 also includes a power button 401 and an RBR button 404.

As described above to operate properly, certain critical circuits, such as processor 416, must be provided power in accordance with certain operational conditions. For example, to operate properly, the plurality of power supplies 426 must provide stable power to processor 416. Additionally, when processor 416 is initialized, the plurality of power supplies must be provided to processor 416 in a certain predetermined order. For example, in settop box 400 of FIG. 4, when processor 416 is initialized power supply 475 must be the last power supply of the plurality of power supplies 426 to become operational and be provided to processor 416. To help facilitate the necessary operational conditions for processor 416 to operate properly, supply monitor/reset circuit 430 is configured to regulate and monitor the power provided to processor 416 by the plurality of power supplies 426. Furthermore, supply monitor/reset circuit 430 is configured to trigger an RBR, as will be described in greater detail below, when one of the power supplies is temporarily disabled.

Turning to FIG. 5, a block diagram of an exemplary power supply circuit 500 according to principles of the present disclosure is shown. Power supply circuit 500 may be used as part of settop box 400 described in FIG. 4, or may be used as part of any of the devices described in FIGS. 1-3. For example, in some embodiments, power supply circuit 500 may be a combination of at least power supply circuit 428, supply monitor/reset control circuit 430, power button 402, and RBR 404. As described above, to operate properly, sensitive circuitry, such as processor 416, have certain operational conditions that must be satisfied. To help meet these operational conditions, in some embodiments, power supply circuit 500 may be used to provide power to, manage, and monitor the plurality of power supplies 426 in settop box 400.

Referring to FIG. 5, power supply circuit 500 includes DC jack 502. DC jack 502 includes light emitting diode (LED) 501. Power supply circuit 500 also includes switching device 503, red button 504, or logic gate 508, voltage divider 521, supply monitor/reset 511, regulator 560, and regulator 570. Supply monitor/reset circuit 511 includes DC jack LED detector 516, RBR detector/timer 518, regulators 520, 530, 540, and current limit and short circuit (S.C.) protector 550. More specifically, DC jack 502 is coupled to switching device 503 and DC jack LED detector 516. Switching

device 503 is coupled voltage divider 521, RBR detector/timer 518, regulator 520, 530 and 540, current limit & S.C. protector 550, regulator 560 and regulator 570. Furthermore, red button 504 is coupled to OR gate 508 and OR gate 508 is coupled to RBR detector/timer 518 in supply monitor/reset circuit 511. It is to be appreciated that, in some embodiments, red button 504 may be the same as red button 404 from FIG. 4. It is also to be appreciated that switching device 503 may be a field effect transistor (FET), a relay, or similar device.

Regulators 520, 530, 540, 560, and 570 each include a voltage input (labeled VIN in FIG. 5), a voltage output (labeled VOUT in FIG. 5), an enabling pin (labeled EN in FIG. 5), and a power good pin (labeled PG in FIG. 5). More specifically, regulator 520 includes voltage input 522, voltage output 524, enabling pin 526, and power good (PG) pin 528; regulator 530 includes voltage input 532, voltage output 534, enabling pin 536, and power good pin 538; regulator 540 includes voltage input 542, voltage output 544, enabling pin 546, and power good pin 548; regulator 560 includes voltage input 562, voltage output 564, enabling pin 566, and power good pin 568; and regulator 570 includes voltage input 572, voltage output 574, enabling pin 576, and power good pin 578. Also, current limit & S.C. protector 550 includes voltage input 552, voltage output 554, enabling pin 556, and FLT 558. It is to be appreciated that FLT 558 is a fault output asserted when a predetermined current limit has been reached in current limit & S.C. protector 550.

When a POR is initiated by pressing power button 402 on settop box 400, an external power supply provides power to DC jack 502. For example, the external power supply may provide 12V to DC jack 502. The power provided to DC jack 502 is then provided to the FET switch 503. The power signal provided to DC jack 502 is also provided to DC jack LED detector 516. When DC jack LED detector 516 receives the power signal, DC jack LED detector 516 will provide a signal to LED 501 in DC jack 502. When LED 501 receives the signal, LED 501 will light up to indicate that the power is on in settop box 400. It is to be appreciated that LED 501 is configured to light up only when a predetermined threshold voltage is being provided to settop box 400. For example, LED 501 will light up if the input voltage at DC jack

502 is greater than 10.8V – the minimum voltage necessary for settop box 400 to operate properly.

The power provided to FET switch 503 is further provided to voltage inputs 522, 532, 542, 552, 562, and 572 in regulators 520, 530, 540, 560, and 570, respectively. FET switch 503 also provides power to voltage divider 521. Each regulator in power supply circuit 500 is configured to output a predetermined voltage signal upon being supplied with power from FET switch 503. It is to be appreciated the regulators shown in FIG. 5 represent at least some of the power supplies in the plurality of power supplies 426 in FIG. 4. Furthermore, it is to be appreciated that the output voltage signal from each regulator shown in FIG. 5 represents at least some of the power being provided to various components within settop box 400, such as processor 416.

For example, referring to FIG. 5, a 12 V power signal is provided to voltage inputs 522, 532, 542, 562, and 572 on regulators 520, 530, 540, 560, and 570, respectively, via an external brick power supply. When regulator 520 receives the 12 V input voltage signal, regulator 520 will output an output voltage signal 525 of 3.3 V. Similarly, when regulators 530, 540, 560, and 570 receive an input voltage signal, regulator 530 will output an output voltage signal 535 of 2.5 V, regulator 540 will output an output voltage signal 545 of 1.5 V, regulator 560 will output an output voltage signal 565 of 1 V, and regulator 570 will output an output voltage signal 575 of 1 V. It is to be appreciated that output voltage signals 525, 535, 545, 565, and 575 are provided to various components of settop box 400, such as processor 416.

It is to be appreciated that current limit & S.C. protector 550 is not powered directly through DC jack 502, instead it is powered by a separate 5V power supply derived from power through DC jack 502 that is not shown in FIG. 5. Furthermore, it is to be appreciated that, in contrast to regulators 520, 530, 540, 560, and 570, current limit & S.C. protector 538 does not alter the input voltage received to produce a different output voltage. Current limit & S.C. protector 550 receives 5V input voltage signal 551 at voltage input 552 and outputs a 5V output voltage signal 555.

The 5V output voltage signal 555 may then be provided to one of the components included in settop box 400, such as a USB port (not shown). .

Each of the enabling pins in regulators 520, 530, 540, 560, and 570 are configured to receive a voltage signal. The enabling pins in each regulator are configured such that when the voltage signal received at the enabling pin reaches a predetermined voltage, the PG pin in that regulator will assert a PG signal to indicate that the regulator is within tolerance (i.e., has reached an appropriate voltage). When the voltage signal received at one of the enabling pins falls below the predetermined threshold voltage level, the PG pin in that regulator will de-assert its PG signal to indicate that the regulator is not within tolerance (i.e., the power being provided is not good or below a predetermined threshold). It is to be appreciated that the PG signals in power supply circuit 500 are active high, therefore, in the present disclosure, when it is stated that a PG signal is being asserted it is intended to mean that the corresponding regulator is holding its PG signal high (i.e., high voltage), while when it is stated that a PG signal is being de-asserted it is intended to mean that the corresponding regulator is holding its power good signal low (i.e., ground or 0).

Also, the output voltages or the PG signals of a regulator may be coupled to the enabling pin of another regulator. Furthermore, the specific voltage threshold of each enabling pin may be chosen as desired. In this way, power circuit 500 may be configured so that during a POR certain regulators are enabled before others so as to satisfy any operational conditions present in sensitive circuitry, such as processor 416 of settop box 400. Also, power circuit 500 may be configured such that predetermined, stable voltages are provided to processor 416. If the predetermined, stable voltages stop being provided to processor 416, power circuit 500 is configured to trigger a processor reset, as will be described in greater detail below.

For example, referring to FIG. 5, when a POR is initialized, a 12V signal is provided to voltage divider 521 via DC jack 502 and FET switch 503. Then, voltage divider 521 will provide a voltage signal 523 to enabling pin 526 of regulator 520. When voltage signal 523 reaches a predetermined threshold voltage at enabling pin

526, regulator 520 will be enabled and PG pin 528 will provide PG signal 529. The voltage threshold of enabling pin 526 is set so that regulator 520 is enabled when a 10.5 V signal is provided to voltage divider 521. Voltage divider 521 provides voltage signal 523, where voltage signal 523 is compatible with the voltage range of enabling pin 526, which is 0 to 3.6V. The 3.3V voltage output signal 525 is then provided to enabling pin 536 in regulator 530, enabling pin 546 in regulator 540, and enabling pin 525 in regulator 560. When the predetermined threshold voltage is provided to enabling pin 536, regulator 530 will be enabled and PG pin 538 will provide PG signal 539. When the predetermined threshold voltage is provided to enabling pin 546, regulator 540 will be enabled and PG pin 548 will provide PG signal 549. When the predetermined threshold voltage is provided to enabling pin 566, regulator 560 will be enabled and PG pin 568 will provide PG signal 569. When the predetermined threshold voltage is provided to enabling pin 576, regulator 570 will be enabled and PG pin 578 will provide PG signal 579.

PG signals 529, 539, and 549 are configured such that when regulators 520, 530, and 540 are within tolerance (i.e., the voltage signals provided to enabling pins 526, 536, and 546 are above a predetermined threshold voltage and the output of the regulator is within +/- 5% of its nominal value), supply monitor/reset circuit 511 will provide a power good all (PGALL) signal 512. However, when regulators 520, 530, or 540 are not within tolerance (i.e., either PG signal 529, 539, or 549 is de-asserted because one or more of the voltage outputs are outside of design tolerance or the signals provided to enabling pins 526, 536, or 546 fall below the predetermined threshold voltage), the PGALL signal 512 will be de-asserted.

PGALL signal 512 is coupled to RESETB signal 514 such that, when the PGALL signal 512 is de-asserted, the RESETB signal 514 will be held low (i.e., logical 0 or ground) until the PGALL signal 512 is asserted again. It is to be appreciated that RESETB signal 514 is configured to initialize a processor reset. A processor reset resets processor 416, however, it is to be appreciated that the processor reset does not affect any other componenents in settob box 400. It is also to be appreciated that RESETB signal is an active low. Therefore, when the RESETB signal 514 is held low, the processor 416 will be held in reset. Furthermore,

all of the PG signals shown in FIG. 5 are open drain signals. In other words, the PG signals can only actively pull low when they are asserted. This allows all the PG signals to be connected together in a logical AND configuration. That is, if any PG signal is low, RESETB will be low.

When power is initially provided to regulators 520, 530, and 540 in supply monitor/reset circuit 511, the signal RESETB 514 is held low by the PGALL signal 512. Each regulator in supply monitor/reset circuit 511 will hold its corresponding PG signal low until the supply from that regulator is within tolerance. In this way, the RESETB signal 514 will be held low, thus holding the processor 416 in reset, until the last supply is up and within tolerance.

In contrast to regulators 520, 530, and 540, regulators 560 and 570 do not include a PGALL signal. Instead, PG signals 569 and 579 in regulators 560 and 570, respectively, are coupled directly to RESETB signal 514. Therefore, when either PG signal 569 or 579 is de-asserted, RESETB signal 514 will be held low and processor 416 will be held in reset.

It is to be appreciated that current limit & S.C. protector 538 does not have a power good signal because current limit & S.C. protector 538 has no function in the power sequencing of processor 416 of settop box 400. Current limit & S.C. protector 538 is configured to prevent a certain amount of current from flowing to the USB port of settop box 400 to avoid any short circuiting that can occur on the USB port. Signal 553 (USB1_PWRON) is provided to enabling pin 556 of current limit & S.C. protector 538. Voltage output 554 in current limit & S.C. protector 538 provides output voltage signal to a USB port for settop box 400 (not shown).

As described earlier, a problem may occur when settop box 400 is subjected to AC mains supply line dropouts having varying amplitude and duration. In some cases, when an AC mains supply line dropout occurs, one or more of the regulators in power supply circuit 500 may temporarily drop out of tolerance. If one or more of the regulators drop out of tolerance, the PG signal from the regulator that has

dropped out of tolerance will be de-asserted and the RESETB signal 514 will be held low, causing the processor to enter a reset. When the processor 416 comes out of its reset state, processor 416 expects to be provided the correct power supply start up sequence as if a POR had been initiated. In many instances, when an AC mains supply line dropout occurs, all the regulators in power supply circuit 500 will fall out of tolerance and when the processor 416 comes out of its operational state the proper power sequencing will take place as described above. However, an AC mains supply line dropout may occur with a certain combination of amplitude and duration that causes one or more of the regulators in power supply circuit 500 to fall out of tolerance the other regulators remain operational. If one or more of the regulators remain operational during a processor reset, it is possible that proper power sequencing will not take place. As a result, processor 416 will not be able to operate properly.

To mitigate the negative effects an AC line dropout may have on settop box 400, adjustments may be made to the voltage thresholds of enabling pins 526, 536, 546, 566, and/or 576. For example, an operational condition may exist requiring regulator 540 to become operational at a point in time after regulators 520 and 530 following initialization of a reset condition. Additionally, an operational condition may exist requiring regulator 570 to become operational at a point in time after all other regulators in power supply circuit 500. To make it more likely that a specific regulator is disabled during an AC line dropout, the voltage threshold on the enabling of the regulator may be set lower than the voltage threshold on enabling pins. Although, these adjustments may decrease the negative effects an AC line dropout may have on settop box 400, it cannot guarantee that one of the regulators will not remain operational during an AC line dropout.

To guarantee that all the regulators in power supply circuit 500 are disabled during an AC line dropout, in accordance with an embodiment of the present disclosure, power supply circuit 500 is configured such that an automatic RBR condition is created. The automatic RBR condition is configured to force an RBR even though a user has not initiated the condition.

Normally, to initiate an RBR, red button 504 (or red button 404) is pressed. When red button 504 is pressed, signal 505 is provided to OR gate 508. Alternatively, an RBR may be initiated when a user selects a system reset within the software of settop box 400. When a system reset is selected in the software of settop box 400, processor 416 will provide signal 506 (SOFT_REET) to OR gate 508. OR gate 508 is configured such that if either signal 505 or signal 506 are provided to OR gate 505, OR gate 505 will provide signal 510 to RBR detector/timer 518 in supply monitor/reset circuit 511. When RBR detector/timer 518 receives signal 510 from OR gate 508, a signal will be provided from RBR detector/timer 518 to FET switch 503. When FET switch 503 receives the signal from RBR detector/timer 518, FET switch 503 will stop providing the power FET switch 503 is receiving from DC jack 502 to voltage divider 521, regulators 520, 530, 540, 560, and 570, and current limit and S.C. protector 550. The FET switch will stop providing the power received from DC jack 502 to the rest of power supply circuit 500 for a predetermined amount of time (e.g., a time period of three seconds). In this way, the voltage in voltage divider 521, regulators 520, 530, 540, 560, 570, and current limit and S.C. protector 550 will drop to a predetermined low level (e.g., below 0.2V). After, a predetermined amount of time, the FET switch will again begin providing the power received from DC jack 502 to the rest of power supply circuit 500 and the proper power sequencing will commence as if a POR had been initiated.

To produce the automatic RBR when any regulator in supply monitor/reset circuit 511 has fallen out of tolerance, a unidirectional connection 515 is made between RESETB signal 514 and signal 505. Unidirectional connection 515 is configured such that when PGALL 512 is de-asserted, thus pulling RESETB signal 514, processor 416 will enter into a processor rest and a signal will be provided along unidirectional connection 515 to signal 505 and then to OR gate 508. The signal provided to OR gate 508 will cause an RBR to be initiated as if red button 504 had been pressed. It is to be appreciated that if unidirectional connection 515 is made with signal 506 instead of signal 505 the same effect may be achieved (i.e., an automatic RBR will be initiated when PGALL 512 is de-asserted). In this way, when any of the regulators in supply monitor/reset circuit 511 falls out of tolerance, an RBR

will automatically be initiated, and then proper power sequencing can be guaranteed; therefore, the operational conditions of processor 416 will be satisfied. It is to be appreciated that, since regulators 560 and 570 also have their PG signals (569 and 579) connected to RESETB signal 514, they will also generate the automatic RBR when PG signals 569 and/or 579 are de-asserted. Therefore, all regulators in power supply circuit 500 are monitored and any regulator pulling its PG signal low will initiate an RBR sequence as described above.

Although FIG. 5 shows one supply monitor/reset circuit including three regulators, it is to be appreciated that power supply circuit 500 may include multiple supply monitor/reset circuits, each including multiple regulators as needed to regulate and monitor any desired amount of power supplies. Furthermore, it is to be appreciated that although FIG. 5 includes values for various input and output voltages, the values included in FIG. 5 are exemplary and may be adjusted as necessary to satisfy any existing operational conditions for differing circuitry. Also, although only one current limit & S.C. protector is shown in FIG. 5, it is to be appreciated that power supply circuit 500 may include other current limit & S.C. protectors to protect other ports in settop box 400, such as an HDMI port or any other port.

Turning to FIG. 6, a block diagram of another exemplary settop box 600 according to principles of the present disclosure is shown. It is to be appreciated that settop box 600 operates in a manner similar to network device 300 described in FIG. 3, MoCA network device 140 or local network device 160 described in FIG. 1, and settop box 400 described in FIG. 4.

Settop box 600 includes, among other elements, processor 616, power button 602, red button reset 604, and power supply circuit 630. It is to be appreciated that processor 616 operates in a similar fashion to processor 416 from FIG. 4. At least some of the circuit elements in processor 616 (not shown) are powered by the output signals of a plurality of power supplies in power supply circuit 630. For example, at least some of the output signals of the plurality of power supplies in power supply

circuit 630 include 1V output signal 625, 1.5V output signal 645, 2.5V output signal 665, 3.3V output signal 635, and 5V output signal 655. The output signals of the plurality of power supplies in power supply circuit 630 are provided from power supply circuit 630 to various parts of settop box 600. It is to be appreciated that the output signals provided from power supply circuit 630 to the various part of settop box 600 shown in FIG. 6 are merely exemplary and reflect only a small number of the output signals being provided from the plurality of power supplies in power supply circuit 630. The plurality of power supplies in power supply circuit 630 are generated by external power supply unit (External PSU) 614. It is to be appreciated that External PSU 614 is coupled to power supply circuit 630.

As with processor 416 in settop box 400, for processor 616 in settop box 600 to operate properly, certain operational conditions must be met. For instance, to operate properly, the plurality of power supplies in settop box 600 must provide stable power to processor 616. Additionally, when processor 616 is initialized, the plurality of power supplies must be provided to processor 616 in a certain predetermined order. To help facilitate the necessary operational conditions for processor 616, power supply circuit 630 is used.

Turning to FIG. 7, a block diagram of another exemplary power supply circuit 700 according to principles of the present disclosure is shown. Power supply circuit 700 may be used as part of settop box 600 described in FIG. 6, or may be used as part of any of the devices described in FIGS. 1-4. It is to be appreciated that power supply circuit 700 may be included in settop box 600, for example, inside power supply circuit 630. Furthermore, although below power supply circuit 700 will be described as being used with settop box 600, it is to be appreciated that power supply circuit 700 may be configured for use with other devices as well.

Referring to FIG. 7, power supply circuit 700 includes DC jack 702. DC jack 702 includes LED 701. Power supply circuit 700 also includes FET switch 703, red button 704, voltage dividers 707, 708, 709, 710, supply monitor/reset circuit 711, and supply monitor/reset circuit 713. Supply monitor/reset circuit 711 includes DC jack

LED detector 716, RBR detector/timer 718, regulators 720, 730, 740, and current limit and S.C. protector 750. Supply monitor/reset circuit 713 includes regulators 760, 770, and current limit and S.C. protector 780. More specifically, DC jack 702 is coupled to FET switch 703 and DC jack LED detector 716. FET switch 703 is coupled to RBR detector/timer 718, voltage dividers 707, 708, 709, 710, regulators 720, 730, 740, 760, 770, and current limit & S.C. protectors 750 and 780. Furthermore, red button 704 is coupled to RBR detector/timer 718 in supply monitor/reset circuit 511. It is to be appreciated that, in some embodiments, red button 704 may be the same as red button 604 from FIG. 6.

Similar to the regulators in FIG. 4, regulators 720, 730, 740, 760, 770, and 780 each include a voltage input, a voltage output, an enabling pin, and a power good pin. Current limit & S.C. protectors 750 and 760 each include a voltage input, a voltage output, and enabling pin, and an FLT pin. It is to be appreciated that the regulators and current limit & S.C. protectors in supply monitor/reset circuits 711 and 713 function in a similar manner to the regulators and current limit & S.C. protectors in supply monitor/reset circuit 511 from FIG. 4.

When power button 602 is pressed (i.e., a POR is initiated) on settop box 600, External PSU 614 will provide a 12V power signal to DC jack 702. DC jack 702 will provide the power signal to FET switch 703 and DC jack LED detector 716. When DC jack LED detector 716 receives the power signal, DC jack LED detector 716 will transmit a signal to LED 701 in DC jack 702, causing LED 701 to light up to indicate that the power has been turned on in settop box 600. The power signal provided to FET switch 703 is further provided to the voltage inputs of regulators 720, 730, 740, 760, and 770. Furthermore, the power signal provided to FET switch 703 is also provided to voltage dividers 707, 708, 709 and 710. It is to be appreciated that current limit and S.C. protectors 750 and 760 are each provided an input voltage from a separate 5V power supply not shown in FIG. 7. It is also to be appreciated that in contrast to the other regulators in FIG. 7, the enabling pin in regulator 720 is enabled by the voltage output 765 (2.5V) of regulator 760 and regulators 730, 740, 760, and 770 are enabled by the voltage outputs of voltage dividers 707, 708, 709, and 710, respectively.

Similar to the regulators in power supply circuit 500, each of the regulators in power supply circuit 700 will output a predetermined voltage upon being supplied with power from FET switch 703. The voltage output from each regulator may power one or more of the components in settop box 600. For example, it is to be appreciated that the regulators in FIG. 7 may be the same as the plurality of power supplies in power supply circuit 630. Furthermore, in some embodiments, the voltage outputs from the regulators in supply monitor/reset circuit 711 and 713 may be used to power processor 616 and other components in settop box 600. Specifically, referring to FIG. 7, regulator 720 provides voltage output signal 725 to processor 616, where voltage output signal 725 may be the same as 1V output signal 625. Regulator 730 provides voltage output signal 735 to processor 616, where voltage output signal 735 may be the same as 3.3V output signal 635. Regulator 740 provides voltage output signal 745 to processor 616, where voltage output signal 745 may be the same as 1.5V output signal 645. Regulator 760 provides voltage output signal 765 to processor 616, where voltage output signal 765 may be the same as 2.5V output signal 665. Regulator 770 provides voltage output signal 775 (5.0V) to processor 616.

Furthermore, similar to the regulators in supply monitor/reset circuit 511 from FIG. 5, the regulators in supply monitor/reset circuit 711 in FIG. 7 will each provide a PG signal when a predetermined threshold voltage has been provided to each enabling pin in each regulator. Specifically, regulator 720 will provide PG signal 729, regulator 730 will provide PG signal 739, and regulator 740 will provide PG signal 749. In contrast, when the voltage being provided to the enabling pin of any of the regulators within supply monitor/reset circuit 711 falls below a predetermined voltage threshold, the PG signal from that regulator will be de-asserted. For example, if the voltage that is provided to the enabling pin in regulator 730 falls below a predetermined voltage threshold, PG signal 729 will be de-asserted. The predetermined voltage threshold value will depend on the regulated supply voltage level but may typically be 95 percent of the regulated supply voltage level (e.g., 4.75 volts for voltage output signal 775 (5.0V)).

As with PG signals 529, 539, and 549 if supply monitor/reset circuit 511, PG signals 729, 739, and 749 in supply monitor/reset circuit 711 are configured such that when all three PG signals are being provided PGALL signal 712 is asserted. In contrast, when any of the three PG signals in supply monitor/reset circuit 711 are de-asserted, PGALL signal 712 is also de-asserted. Furthermore, PGALL signal 712 is coupled to a RESETB signal 714 in power supply circuit 700 such that when PGALL signal 712 is de-asserted the RESETB signal 714 is held low, causing processor 616 to enter into a processor reset. It is to be appreciated that the processor reset for processor 616 is the same as the processor reset described above in relation to processor 416.

Regulators 760 and 770 in supply monitor/reset circuit 713 each also provide a PG signal when the enabling pins in regulators 769 and 770 have been provided with a predetermined threshold voltage. Specifically, regulator 760 provides PG signal 769 to logic gate 717, and regulator 770 provides PG signal 779 to logic gate 717. However, unlike PG signals 729, 739, and 749 from regulators 720, 730, and 740, the PG signals 769 and 779 provided from regulators 760 and 770 are not individually available to be provided to other parts of power supply circuit 700. For example, the PG signals from regulators 760 and 770 are not available for use to enable another regulator (similar to PG signal 539 in power supply circuit 500). Instead, PG signals 769 and 779 are both provided to logic gate 717. Logic gate 717 is configured such that when both PG signal 769 and 779 are being provided to logic gate 717, logic gate 717 will provide a PGOOD signal 719. Similar to PGALL signal 712, PGOOD signal 719 is coupled to RESETB signal 714 in settop box 600 such that when the PGOOD signal 719 is de-asserted, the PGOOD signal 719 will hold the RESETB signal 714 low, causing processor 616 to enter into a processor reset state.

It is to be appreciated that current limit & S.C. protectors 750 and 770 are not powered by DC jack 702, instead they are powered by a separate 5V power supply that are not shown in FIG. 7. Furthermore, it is to be appreciated that, in contrast to regulators 720, 730, 740, 760, and 770, current limit & S.C. protectors 750 and 770 do not alter the input voltage received to produce a different output voltage. Current limit & S.C. protectors 550 and 570 receive a 5V input voltage signal and output 5V

output voltage signals 755 and 785, respectively. The 5V output voltage signals 755 and 785 may then be provided to one of the components included in settop box 400, such as a USB or HDMI port (not shown). It is to be appreciated that output voltage signals 755 or 785 may be the same as output signal 655 in FIG. 6.

As in power supply circuit 500, power supply circuit 700 is configured such that any operational conditions necessary for processor 616 to operate properly are satisfied. Specifically, power supply circuit 700 is configured such that predetermined, stable voltages are being provided. Furthermore, power supply circuit 700 is configured such that when a POR is initiated regulators 720, 730, and 740 (i.e., the regulators providing power to processor 616) become operational (i.e., are brought within tolerance and provide output voltage signals 725, 735, and 745) in the proper order as required by processor 616. For example, a necessary operational condition for processor 616 in settop box 600 is that output voltage signal 725 (i.e., +1V0AVS in FIG. 7) is provided to processor 616 only after output voltage signals 735, 745, 775 and 765.

Although power supply circuit 700 is configured to satisfy any existing operational conditions for processor 616, as described above, problems may occur when settop box 600 is subjected to AC line dropouts of varying duration and amplitude. When settop box 600 is subject to AC line dropouts, an error may occur where power supply circuit 700 is unable to provide the proper power sequencing for processor 616. Specifically, an AC line dropout may cause one or more of the regulators in power supply circuit 700 to be disabled while regulator 720 remains operational. When this occurs, processor 616 will enter a processor reset state. As described above, during a processor reset, processor 616 expects that any power supplies that are provided to processor 616 will become operational in the proper order. If regulator 720 remains operational during a processor reset, regulator 720 will not be the last regulator to become operational; therefore, processor 616 will not be provided power in the proper order. If processor 616 is not provided power in the proper order after a reset, it may cause processor 616 to experience problems. For example, processor 616 may lock up or enter a loop.

To mitigate the effects an AC line dropout may have on settop box 600, the threshold voltage of one or more enabling pins may be adjusted in power supply circuit 700. For example, as described above, each regulator in supply monitor/reset circuit 711 and 713 has a predetermined threshold voltage that will bring the regulator within tolerance. The enabling pins in the regulators of power supply monitor/reset circuit 711 and 713 are configured such that if the enabling pin of a given regular falls below approximately 1.7V the corresponding regulator will be disabled (i.e., the regulator will fall out of tolerance and its PG signal will be de-asserted). There is approximately a 0.9V threshold variance on any given enabling pin in power supply circuit 700. That is, the guaranteed "high" input of any enabling pin is 1.8V while the guaranteed "low" input is 0.9V.

As described above, regulator 720 is enabled by voltage output signal 765. This was done to insure that when a POR is initiated regulator 720 is always brought within tolerance after the other regulators in power supply circuit 700. The threshold voltage for the enabling pin in regulator 760 may be set 0.9V lower than all the other regulators in power supply circuit 700. Therefore, when an AC line dropout occurs regulator 760 should be disabled before all other regulators. When regulator 760 is disabled, regulator 760 will no longer provide voltage output signal 765 to the enabling pin of regulator 720 and regulator 720 will fall out of tolerance and be disabled. By adjusting the threshold voltage on the enabling pin in regulator 760, regulator 720 should most likely be disabled before regulators 730 and 740 during an AC line dropout. However, as described above, it cannot be guaranteed that regulator 720 will be disabled during an AC line dropout. There may still exist a duration and amplitude of an AC line dropout that will cause regulator 730,740 or 770 in supply monitor/reset circuit 711 to be disabled while regulator 720 remains operational.

To guarantee that all the regulators in supply monitor/reset circuit 711 and 713 are disabled during an AC line dropout, in accordance with an embodiment of the present disclosure, power supply circuit 700 is configured such that an automatic RBR condition is created. The automatic RBR condition is configured to force an RBR even though a user has not initiated the condition.

Similar to power supply circuit 500, in power supply circuit 700 there are two ways for the user to initiate an RBR. The first way the user may initiate an RBR is by pressing red button 704. When red button 704 is pressed, SYS_RESET signal 705 is provided to RBR detector/timer 718. An alternative way the user may initiate an RBR is by selecting a system reset option in the settop box software (this may be done in a graphical user interface generated on a display coupled to settop box 600). When the user selects the system reset option, processor 616 will provide SOFT_RESET signal 706 to RBR detector/timer 718. RBR detector/timer 718 is configured such that if either SYS_RESET signal 705 or SOFT_RESET signal 706 are provided to RBR detector/timer 718, RBR detector/timer 718 will provide a signal to FET switch 703. When FET switch 703 is provided with a signal from RBR detector/timer 718, FET switch 703 will stop providing power to supply monitor/reset circuit 711 and supply monitor/reset circuit 713 that FET switch 703 is receiving from DC jack 702 for a predetermined amount of time (for example, in the present embodiment, it may be 3 seconds, however it is appreciated that the time may be adjusted as necessary). As described earlier, when FET switch 703 stops providing power to supply monitor/reset circuit 711 and supply monitor/reset circuit 713, the voltage levels inside regulators 720, 730, 740, 760, and 770 will drop to a predetermined voltage level (for example, in the present embodiment the voltage levels will be dropped to 0.2V).

To produce the automatic RBR when any regulator in supply monitor/reset circuit 711 and 713 has fallen out of tolerance, a unidirectional connection 715 is made between RESETB signal 714 and SYS_RESET signal 705. Unidirectional connection 715 is configured such that when PGALL 712 or PGOOD 719 is de-asserted, RESETB signal 714 will be provided along unidirectional connection 715 to SYS_RESET signal 705 and then to RBR detector/timer 718. The signal provided to RBR detector/timer 718 will cause an RBR to be initiated as if red button 704 had been pressed. It is to be appreciated that if unidirectional connection 515 is made with SOFT_RESET signal 706 instead of SYS_RESET signal 705 the same effect may be achieved (i.e., an automatic RBR will be initiated when PGALL 712 is de-asserted). In this way, when any of the regulators in supply monitor/reset circuit 711 and/or 713

fall out of tolerance, an RBR will automatically be initiated, and then proper power sequencing can be guaranteed; therefore, the operational conditions of processor 616 will be satisfied even if an AC line dropout occurs.

Although FIG. 7 shows supply monitor/reset circuit 711 including three regulators and supply monitor/reset circuit 713 including two regulators, it is to be appreciated that power supply circuit 700 may include multiple supply monitor/reset circuits, each including multiple regulators as needed to regulate and monitor any desired amount of power supplies. Furthermore, it is to be appreciated that although FIG. 7 includes values for various input and output voltages, the values included in FIG. 7 are exemplary and may be adjusted as necessary to satisfy any existing operational conditions for differing circuitry. Also, although only two current limit & S.C. protectors are shown in FIG. 7, it is to be appreciated that power supply circuit 700 may include multiple current limit & S.C. protectors to protect multiple ports in settop box 600.

Turning to FIG. 8, a schematic of a power supply circuit 800 used in a device according to principles of the present disclosure is shown. The power supply circuit 800 may be used as part of power supply 500 described in FIG. 5 in conjunction with settop box 400 described in FIG. 4. The power supply circuit 800 may be used as part of power supply 700 described in FIG. 7 in conjunction with settop box 600 described in FIG. 6. Power Supply circuit 800 may also be used in conjunction with any of the devices described in FIGS. 1-3.

Power supply circuit 800 shows the circuitry associated with the interface to the AC mains supply through a connection 801 to an external power supply converter (not shown). It is to be appreciated that connection 801 may be the same as DC jack 702 from FIG. 7. Power supply circuit 800 also shows the control circuit used in conjunction with an RBR, where elements 814-821 represent the control circuit. The control circuit includes a FET switch 817 (QP501) that is in series with the 12V DC input supply. It is to be appreciated that FET switch 817 may be the same as FET switch 703 from FIG. 7. When the red button (not shown) is pressed, FET switch 817

is “opened” for 3 seconds decoupling the 12V supply from the regulators (for example, the regulators in FIG. 7) and causing all supplies to drop below 0.2V. When FET switch 817 couples the 12V supply again at the end of 3 seconds, the unit will power up in accordance with a POR, as described above.

Below, a chart is provided lisiting the elements shown in FIG. 8 and corresponding values to each element:

Element	Type	Value
801	Power jack	12 volt
802	Capacitor	1 nanofarad
803	Capacitor	1 nanofarad
804	Capacitor	100 nanofarad
805	Resistor	0 ohm
806	Resistor	0 ohm
807	Resistor	0 ohm
808	Resistor	0 ohm
809	Capacitor	100 nanofarad
810	Zener Diode	18 volt
811	Capacitor	10 microfarad
812	Capacitor	100 microfarad
813	Capacitor	10 microfarad
814	Resistor	10 kiloohm
815	Resistor	10 kiloohm
816	Capacitor	10 microfarad
817	Transistor	DMP3056
818	Resistor	10 ohm
819	Capacitor	10 nanofarad
820	Capacitor	10 nanofarad
821	Capacitor	100 nanofarad

Turning to FIGs. 9a and 9b, a schematic of a power supply circuit 900 used in a device according to principles of the present disclosure is shown. The power supply circuit 900 may be used as part of power supply 500 described in FIG. 5 in conjunction with settop 400 described in FIG. 4. The power supply circuit 900 may be used as part of power supply 700 described in FIG. 7 in conjunction with settop 600 described in FIG. 6. Power Supply circuit 900 may also be used in conjunction with any of the devices described in FIGS. 1-3.

Power supply circuit 900 shows the circuitry associated with a set of individual power supplies used for the various circuits in a device. In particular, power supply circuit 900 shows the power supply circuitry used with critical elements in a device, such as a processor. For example, in some embodiments, power supply circuit 900 includes one or more elements of power supply circuit 700 and is used to power processor 616 from settop box 600.

Power supply circuit 900 may also interface to an input supply circuit, such as power supply circuit 800 shown in FIG. 8. Power supply circuit 900 also shows circuitry associated with power supply monitoring and internal reset conditioning. For example, power supply circuit 900 includes supply monitor/reset circuit 926. It is to be appreciated that supply monitor/reset circuit 926 may be the same as supply monitor/reset circuit 711 from FIG. 7. In addition, power supply circuit 900 includes unidirectional connection 979 to implement an automatic RBR in the event of a power supply condition due to AC line dropout. It is to be appreciated that unidirectional connection 979 may be the same as unidirectional connection 715 from FIG. 7. Although power supply circuit 900, show a diode as being used to produce unidirectional connection 979, it is to be appreciated that other components may be used to produce the required unidirectional connection to implement an automatic RBR as described in the embodiments above.

The power supply configuration in power supply circuit 900 provides a mechanism to insure that if any supply drops out, all supplies will be brought down and allowed to go through a proper power up sequence. As described above, the logical OR of the regulator power good signals already resets the processor if any supply is not good by pulling the RESETB signal low. The RBR sequence, described above, insures all the supplies are brought below 0.2V and allowed to come up in the correct sequence. By connecting the RBR signal (SYS_RST – Regulators 1, pin 5) to the RESETB signal via a diode (anode on SYS_RST, cathode on RESETB) the desired effect is achieved. If any supply goes out of tolerance it will cause RESETB to go low which, in turn, will cause the SYS_RST pin to go low initiating a RBR sequence just as if a user had pressed the reset button. There is no longer any

window of pulse duration/ AC voltage that can cause the processor to become locked due to not seeing a proper power up sequence.

Below, a chart is provided lisitng the elements shown in FIGs. 9a and 9b and corresponding values to each element:

Element	Type	Value
901	Ferrite Bead	220 ohm
902	Capacitor	10 microfarad
903	Capacitor	100 nanofarad
904	Resistor	120 kiloohm
905	Resistor	30 kiloohm
906	Resistor	120 kiloohm
907	Resistor	30 kiloohm
908	Resistor	120 kiloohm
909	Resistor	27 kiloohm
910	Capacitor	100 nanofarad
911	Inductor	2.2 microhenry
912	Resistor	0 ohm
913	Capacitor	100 picofarad
914	Resistor	27.4 kiloohm
915	Capacitor	22 microfarad
916	Capacitor	100 nanofarad
917	Resistor	4.7 kiloohm
918	Capacitor	22 microfarad
919	Capacitor	150 nanofarad
920	Capacitor	100 nanofarad
921	Resistor	120 kiloohm
922	Capacitor	100 nanofarad
923	Resistor	100 ohm
924	Resistor	40.2 kiloohm
925	Capacitor	47 nanofarad
926	Integrated Circuit	SN1202027
927	Resistor	0 ohm
928	Capacitor	4.7 nanofarad
929	Resistor	10 kiloohm
930	Capacitor	4.7 nanofarad
931	Resistor	10 kiloohm
932	Capacitor	4.7 nanofarad
933	Resistor	10 kiloohm
934	Resistor	10 kiloohm
935	Resistor	4.7 kiloohm
936	Capacitor	1 nanofarad
937	Resistor	1 kiloohm
938	Capacitor	1 nanofarad
939	Resistor	10 kiloohm
940	Resistor	0 ohm

941	Capacitor	47 nanofarad
942	Capacitor	47 nanofarad
943	Inductor	4.7 microhenry
944	Inductor	4.7 microhenry
945	Capacitor	22 microfarad
946	Resistor	10 ohm
947	Capacitor	22 microfarad
948	Capacitor	100 nanofarad
949	Ferrite Bead	220 ohm
950	Capacitor	10 microfarad
951	Resistor	41.2 kiloohm
952	Capacitor	100 picofarad
953	Resistor	9.9 kiloohm
954	Resistor	2.7 kiloohm
955	Capacitor	100 picofarad
956	Capacitor	470 microfarad
957	Resistor	10 kiloohm
958	Resistor	10 kiloohm
959	Resistor	0 ohm
960	Resistor	4.7 kiloohm
961	Capacitor	100 nanofarad
962	Capacitor	4.7 nanofarad
963	Capacitor	4.7 nanofarad
964	Capacitor	4.7 nanofarad
965	Resistor	1 kiloohm
966	Resistor	0 ohm
967	Capacitor	4.7 microfarad
968	Capacitor	4.7 microfarad
969	Resistor	0 ohm
970	Capacitor	22 microfarad
971	Capacitor	100 picofarad
972	Resistor	100 ohm
973	Resistor	41.2 kiloohm
974	Resistor	27.4 kiloohm
975	Capacitor	22 microfarad
976	Resistor	4.7 kiloohm
977	Ferrite Bead	220 ohm
978	Capacitor	22 microfarad
979	Diode	1N4148
980	Resistor	33 kiloohm
981	Capacitor	1 nanofarad
982	Resistor	470 kiloohm
983	Capacitor	1 nanofarad
984	Resistor	47 kiloohm
985	Capacitor	1 nanofarad
986	Resistor	10 kiloohm
987	Diode	1N4148
988	Capacitor	4700 picofarad

Turning to FIGs. 10a and 10b, a schematic of a power supply circuit 1000 used in a device according to principles of the present disclosure is shown. The power supply circuit 1000 may be used as part of power supply 500 described in FIG. 5 in conjunction with settop 400 described in FIG. 4. The power supply circuit 1000 may be used as part of power supply 700 described in FIG. 7 in conjunction with settop 600 described in FIG. 6. Power Supply circuit 1000 may also be used in conjunction with any of the devices described in FIGS. 1-3.

Power supply circuit 1000 shows the circuitry associated with a set of individual power supplies used for the various circuits in a device. Power supply circuit 1000 includes supply monitor/reset circuit 1020, where supply monitor/reset circuit 1020 may be the same as supply monitor/reset circuit 713 from FIG. 7. Power supply circuit 1000 may be used in conjunction with power supply 800 and power supply circuit 900 to form a complete power supply circuit for a device. It is to be appreciated that the combination of power supply circuits 800, 900, and 1000 may form power supply circuit 700 and may be used to power settop box 700.

Below, a chart is provided lisitng the elements shown in FIGs. 10a and 10b and corresponding values to each element:

Element	Type	Value
1001	Ferrite Bead	220 ohm
1002	Capacitor	10 microfarad
1003	Capacitor	100 nanofarad
1004	Resistor	120 kiloohm
1005	Resistor	30 kiloohm
1006	Resistor	120 kiloohm
1007	Resistor	30 kiloohm
1008	Capacitor	100 nanofarad
1009	Inductor	4.7 microhenry
1010	Capacitor	10 microfarad
1011	Resistor	1 kiloohm
1012	Capacitor	4.7 nanofarad
1013	Resistor	75 kiloohm
1014	Resistor	14.3 kiloohm
1015	Resistor	10 kiloohm
1016	Ferrite Bead	220 ohm
1017	Capacitor	100 nanofarad
1018	Capacitor	10 microfarad

1019	Capacitor	47 nanofarad
1020	Integrated Circuit	TPS65252
1021	Capacitor	4.7 nanofarad
1022	Resistor	10 kiloohm
1023	Diode	1N4148
1024	Resistor	10 kiloohm
1025	Resistor	10 kiloohm
1026	Resistor	10 kiloohm
1027	Resistor	75 kiloohm
1028	Resistor	75 kiloohm
1029	Resistor	232 kiloohm
1030	Resistor	511 kiloohm
1031	Capacitor	4.7 nanofarad
1032	Capacitor	4.7 nanofarad
1033	Capacitor	15 nanofarad
1034	Capacitor	15 nanofarad
1035	Capacitor	4,7 microfarad
1036	Resistor	0 ohm
1037	Capacitor	4.7 microfarad
1038	Resistor	47 kiloohm
1039	Capacitor	1 nanofarad
1040	Capacitor	100 picofarad
1041	Resistor	47 kiloohm
1042	Capacitor	1 nanofarad
1043	Capacitor	100 picofarad
1044	Capacitor	47 nanofarad
1045	Inductor	4.7 microhenry
1046	Capacitor	22 microfarad
1047	Resistor	0 ohm
1048	Resistor	41.2 kiloohm
1049	Capacitor	100 picofarad
1050	Capacitor	22 microfarad
1051	Ferrite Bead	220 ohm
1052	Capacitor	100 nanofarad
1053	Capacitor	22 microfarad
1054	Resistor	0 ohm
1055	Integrated Circuit	TLV70033
1056	Capacitor	1 microfarad
1057	Resistor	0 ohm
1058	Capacitor	1 microfarad
1059	Ferrite Bead	220 ohm
1060	Resistor	19.1 kiloohm
1061	Capacitor	100 nanofarad
1062	Resistor	10 kiloohm
1063	Resistor	0 ohm
1064	Capacitor	4.7 microfarad
1065	Integrated Circuit	TLV71210
1066	Resistor	0 ohm
1067	Capacitor	100 nanofarad
1068	Capacitor	1 microfarad
1069	Ferrite Bead	220 ohm

Turning to FIG. 11, a flow chart illustrating a process 1100 for controlling power supply startup in a processor in a device according to aspects of the present disclosure is shown. Process 1100 describes an automatic restart or automatic RBR that can be used to prevent performance issues (as described above) in a device when an AC line dropout condition occurs. It is to be appreciated that some steps in process 1100 may be removed or reordered to accommodate specific embodiments associated with the principles of the present disclosure. It is also to be appreciated that process 1100 may be applied to power supply circuit 500 as used with settop box 400 and power supply circuit 700 as used with settop box 600.

Referring to FIG. 11, in step 1102, a power on sequence is initialized for processor 416/616. A power on sequence may be initialized for processor 416/616 when settop box 400/600 is turned on (i.e., POR is initialed by pressing the power button on settop box 400/600) or a power on sequence may be initialized when an RBR is initiated (i.e., by pressing red button or choosing system reset in the software of settop box 400/600). During a power on sequence, supply monitor/reset circuit 511/711/713 will ensure all supply voltages have been provided in the proper order to processor 416/616. Supply monitor/reset circuit 511/711/713 is configured such that processor 416/616 will be held in a processor reset state (i.e., RESETB signal 514/715 will be held low) until every regulator in supply monitor/reset circuit 511/711/713 is within tolerance. When all the regulators in supply monitor/reset circuit 511/711/713 are within tolerance, supply monitor/reset circuit 511/711/713 will cause processor 416/616 to exit the processor reset state, and processor 416/616 will be able to begin normal operation within settop box 400/600.

Then, in step 1104, supply monitor/reset circuit 511/711/713 in settop box 400/600 will monitor the regulators that are providing supply voltages to 416/616 to determine if the regulators are within tolerance (i.e., proper power is being provided to processor 416/616 that is stable). In step 1106, if supply monitor/reset circuit 511/711/713 determines that the regulators are all within tolerance, in step 1104, supply monitor/reset circuit 511/711/713 will continue to monitor the regulators in

supply monitor/reset circuit 511/711/713. However, if, in step 1106, supply monitor/reset circuit 511/711/713 determines that one of the regulators have fallen out of tolerance (i.e., the PG signal for that regulator has been de-asserted), in step 1108, supply monitor/reset circuit 511/711/713 will cause processor 416/616 to enter processor reset state and, in step 1110, an RBR will automatically be initialized. Supply monitor/reset circuit 511/711/713 will hold processor 416/616 in a processor reset state until supply monitor/reset circuit 511/711 determines that the regulators providing power to processor 416/616 are within tolerance.

When the automatic RBR is initialized, power supply circuit 500/700 will cause the voltage in all the power supplies in settop box 400/600 to drop to a predetermined voltage level (for example, 0.2V, as described above). All the power supplies will be held at the voltage level for a predetermined amount of time (for example, 3 seconds, as described above). After the predetermined amount of time has passed, in step 1112, a power on sequence will be initialized where supply monitor/reset circuit 511/711/713 will ensure that all supply voltages are provided in the proper order to processor 416/616. The supply monitor/reset circuit 511/711/713 will then determine if the power up sequence is complete, in step 1114. When all the regulators in supply monitor/reset circuit 511/711/713 are within tolerance, i.e., the power up sequence is complete, supply monitor/reset circuit 511/711/713 will cause processor 416/616 to exit the processor reset state, in step 1116, and processor 416/616 will once again be able to begin normal operation within settop box 400/600.

The present embodiments provide a mechanism to insure that if any supply drops out, or fall out of regulation, all supplies will be brought down and allowed to go through a proper power up sequence. Problems with supplies are common in the presence of an AC mains line dropout. As a result of the solutions presented in the embodiment, there is no longer any window of pulse duration/ AC voltage that can cause a critical element, such as a processor, in a device to become in operable or locked due to not seeing a proper power up sequence.

Although embodiments which incorporate the teachings of the present disclosure have been shown and described in detail herein, those skilled in the art

can readily devise many other varied embodiments that still incorporate these teachings. Having described preferred embodiments (which are intended to be illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes may be made in the particular embodiments of the disclosure disclosed which are within the scope of the disclosure.

WHAT IS CLAIMED IS:

1. A method comprising:

providing electrical power to a processing circuit (416, 616), the processing circuit (416, 616) coupled to a plurality of power supplies (426) and requiring a start up sequence for the plurality of power supplies (426);

determining if one of the plurality of power supplies (426) is not properly operating while at least one other of the plurality of power supplies (426) is properly operating;

generating a first reset signal (514, 714) if it is determined that the one of the plurality of power supplies (426) is not properly operating while the at least one other of the plurality of power supplies (426) is properly operating; and

providing the first reset signal (514, 714) to the processor circuit (416, 616) causing the processor circuit (416, 616) to enter a reset condition and to the plurality of power supplies (426) to cause a proper start up sequence for the plurality of power supplies (426).

2. The method as in claim 1, wherein the first reset signal (514, 714) is coupled with a second reset signal (505, 506, 705, 706) to produce an output reset signal based on an “OR” function.

3. The method of claim 2, wherein the second reset signal (505, 506, 705, 706) is generated by at least one of a manual reset input (504, 704) and a software input.

4. The method of claim 1, wherein the first reset signal (514, 714) is provided to the plurality of power supplies (426) via a unidirectional connection (515, 715, 979).

5. The method of claim 4, wherein the unidirectional connection (515, 715, 979) includes at least one diode.

6. The method of claim 1, wherein the determining if one of the plurality of power supplies (426) is not properly operating includes determining if one of the plurality of power supplies (426) has fallen below a first voltage level.

7. The method of claim 6, wherein the providing the first reset signal (514, 714) further comprises reducing the power provided to each of the plurality of power supplies (426) to a power level below a second level before the proper start up sequence is initialized.

8. The method of claim 7, wherein the reducing further comprises maintaining the power provided to each of the plurality of power supplies (426) below the second level for a first period of time.

9. The method of claim of claim 7, wherein a switching device (503, 703, 817) provides power to each of the plurality of power supplies (426), and wherein the providing the first reset signal (514, 714) to the plurality of power supplies (426) to cause a proper start up sequence further comprises:

causing the switching device (503, 703, 817) to reduce the power provided to each of the plurality of power supplies (426) below the second level before the proper start up sequence is initialized.

10. The method of claim 9, wherein the causing the switching device (503, 703, 817) to reduce the power provided to each of the plurality of power supplies (426) further comprises maintaining the power provided to each of the plurality of power supplies (426) by the switching device (503, 703, 817) below the second level for a first period of time.

11. An apparatus comprising:

a processing circuit (416, 616) coupled to a plurality of power supplies (426), the processing circuit (416, 616) requiring a start up sequence for the plurality of power supplies (426); and

a power supply monitoring circuit (430, 630) that determines if one of the plurality of power supplies (426) is not properly operating while at least one other of the plurality of power supplies (426) is properly operating, generates a first reset signal (514, 714) if it is determined that the one of the plurality of power supplies (426) is not properly operating while the at least one other of the plurality of power supplies (426) is properly operating, the power supply monitoring circuit (430, 630) further providing the first reset signal (514, 714) to the processor circuit (416, 616) causing the processor circuit (416, 616) to enter a reset condition and providing the first reset signal (514, 714) to the plurality of power supplies (426) to cause a proper start up sequence for the plurality of power supplies (426).

12. The apparatus of claim 11, wherein the first reset signal (514, 714) is coupled with a second reset signal (505, 506, 705, 706) to produce an output reset signal based on “OR” function.

13. The apparatus of claim 12, wherein the second reset signal (505, 506, 705, 706) is generated by at least one of a manual reset input (504, 704) and a software input.

14. The apparatus of claim 11, wherein the first reset signal (514, 714) is provided to the plurality of power supplies (426) via a unidirectional connection (515, 715, 979).

15. The apparatus of claim 14, wherein the unidirectional connection (515, 715, 979) includes at least one diode.

16. The apparatus of claim 11, wherein the power supply monitoring circuit (430, 630) determines that one of the plurality of power supplies (426) is not properly

operating by determining if one of the plurality of power supplies (426) has fallen below a first voltage level.

17. The apparatus of claim 16, wherein the power supply monitoring circuit (430, 630) causes the power provided to each of the plurality of power supplies (426) to be reduced below a second level before the proper start up sequence is initialized.

18. The apparatus of claim 17, wherein the power supply monitoring circuit (430, 630) causes the power provided to each of the plurality of power supplies (426) to be maintained below the second level for a first period of time.

19. The apparatus of claim 17, further comprising a switching device (503, 703, 817) that provides power to each of the plurality of power supplies (426), wherein the power supply monitoring circuit (430, 630) causes the switching device (503, 703, 817) to reduce the power provided to each of the plurality of power supplies (426) below a second level before the proper start up sequence is initialized.

20. The apparatus of claim 19, wherein the power supply monitoring circuit (430, 630) causes the power provided to each of the plurality of power supplies (426) by the switching device (503, 703, 817) to be maintained below the second level for a first period of time.

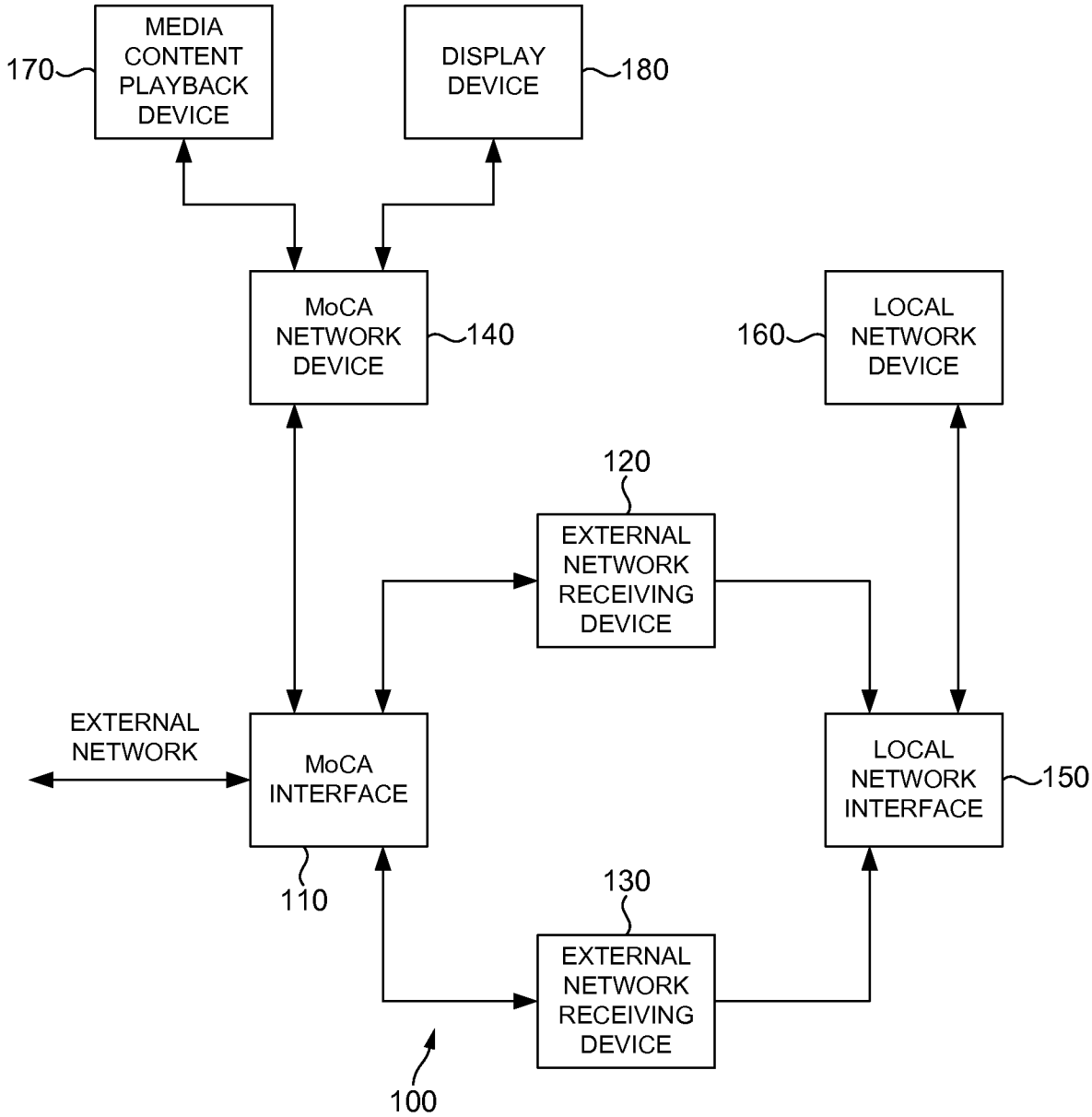
MEDIA CONTENT PLAYBACK DEVICE
170
DISPLAY DEVICE
180
MoCA NETWORK DEVICE
140
LOCAL NETWORK DEVICE
160
120
EXTERNAL NETWORK RECEIVING DEVICE
EXTERNAL NETWORK
MoCA INTERFACE
110
LOCAL NETWORK INTERFACE
150
130
EXTERNAL NETWORK RECEIVING DEVICE
100

FIG. 1

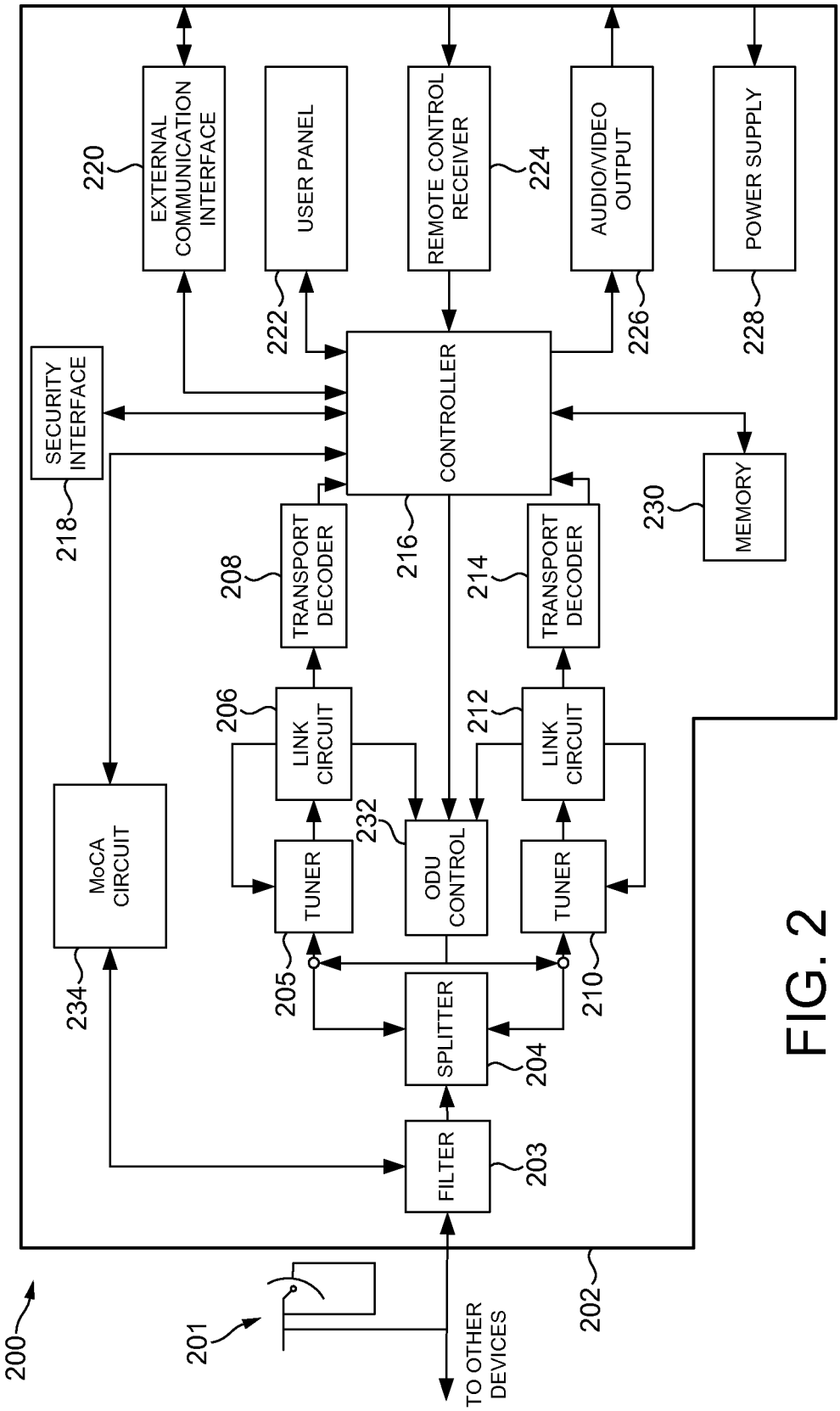
200
201
202
TO OTHER DEVICES
FILTER
203
SPLITTER
204
205
TUNER
206
LINK CIRCUIT
208
TRANSPORT DECODER
210
TUNER
212
LINK CIRCUIT
214
TRANSPORT DECODER
216
CONTROLLER
218
SECURITY INTERFACE
220
EXTERNAL COMMUNICATION INTERFACE
222
USER PANEL
224
REMOTE CONTROL RECEIVER
226
AUDIO/VIDEO OUTPUT
228
POWER SUPPLY
230
MEMORY
232
ODU CONTROL
234
MoCA CIRCUIT

FIG. 2

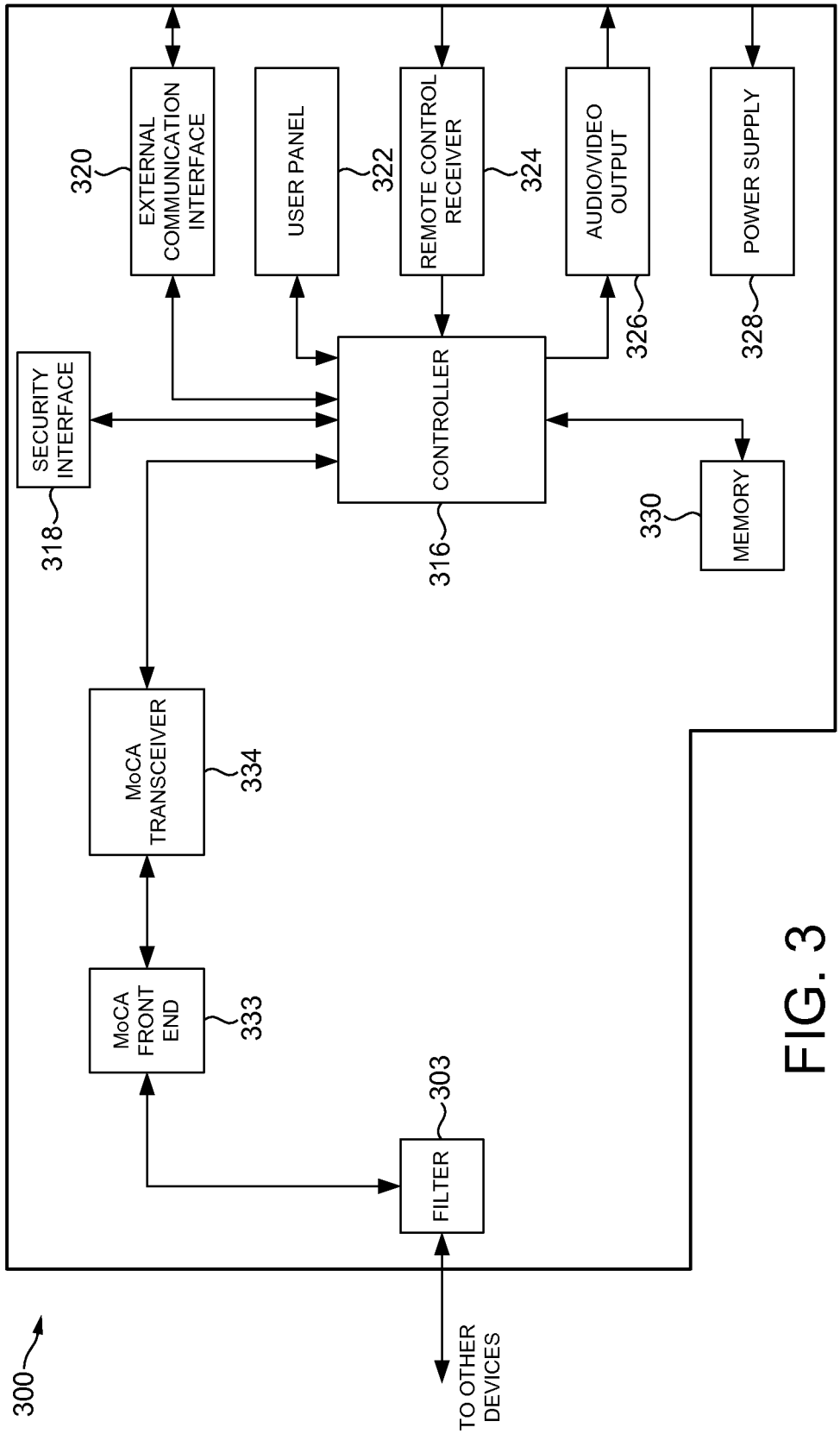
300
TO OTHER DEVICES
FILTER
303
MoCA FRONT END
333
MoCA TRANSCEIVER
334
SECURITY INTERFACE
318
CONTROLLER
316
MEMORY
330
EXTERNAL COMMUNICATION INTERFACE
320
USER PANEL
322
REMOTE CONTROL RECEIVER
324
AUDIO/VIDEO OUTPUT
326
POWER SUPPLY
328

FIG. 3

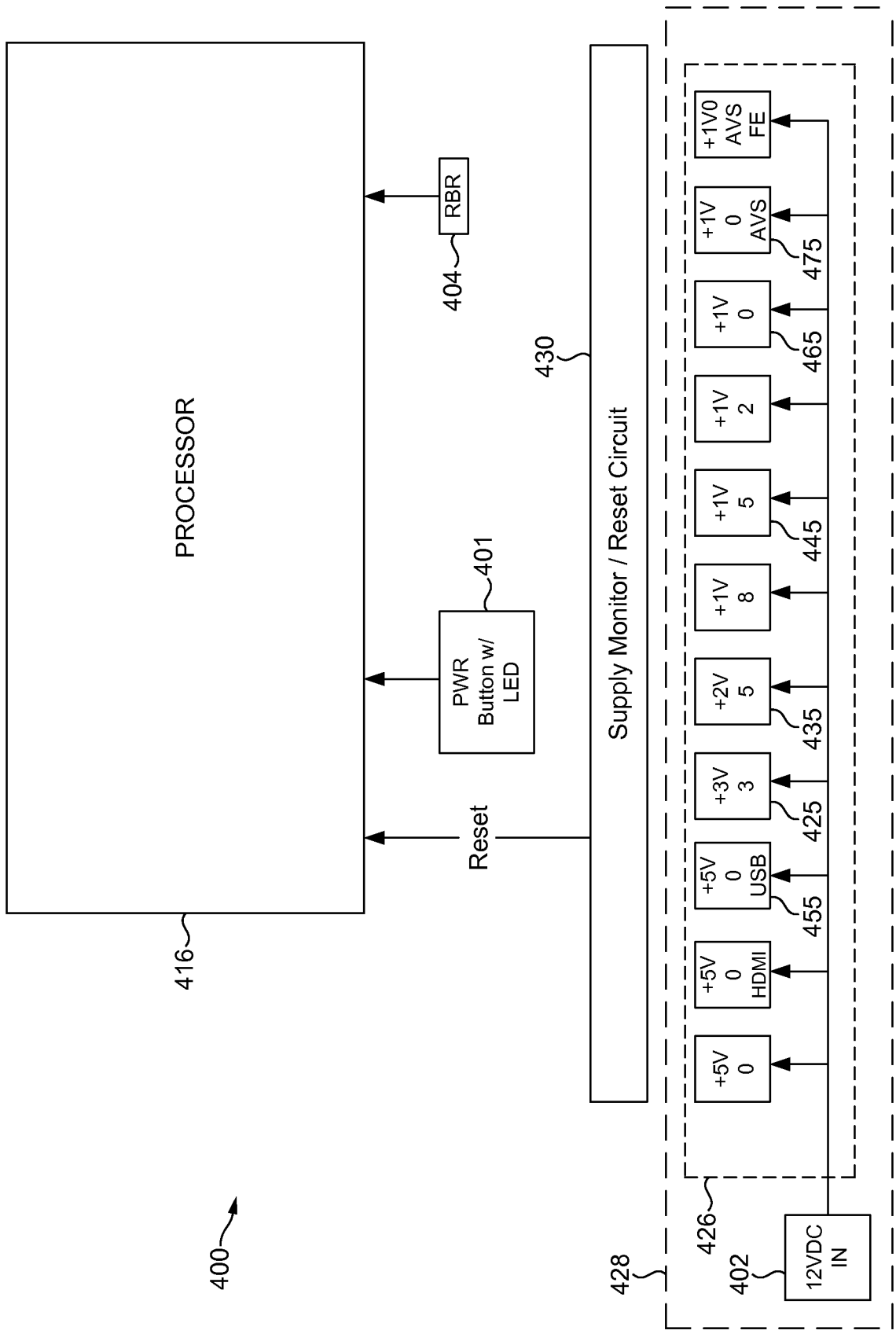
400
PROCESSOR
416
RBR
404
PWR Button w/ LED
401
Reset
430
Supply Monitor / Reset Circuit
428
426
402
12VDC IN
+5V 0
+5V 0 HDMI
+5V 0 USB
455
+3V 3
425
+2V 5
435
+1V 8
+1V 5
445
+1V 2
+1V 0
465
+1V 0 AVS
475
+1V0 AVS FE

FIG. 4

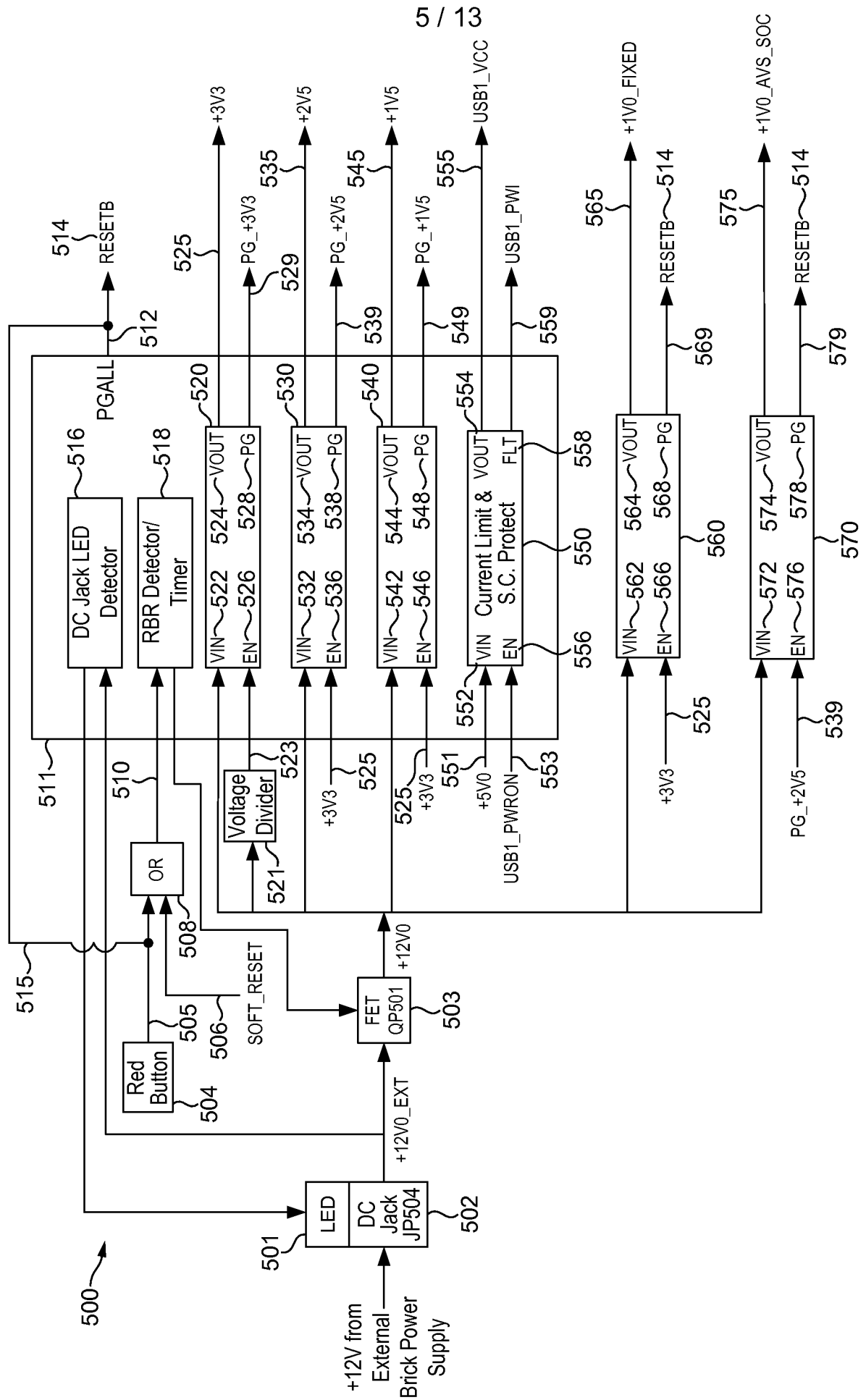
500
+12V from External Brick Power Supply
501
LED
DC Jack JP504
502
+12V0_EXT
FET QP501
503
+12V0
Red Button
504
505
506
SOFT_RESET
OR
508
510
511
515
512
PGALL
514
RESETB
516
DC Jack LED Detector
518
RBR Detector/ Timer
520
VIN
522
EN
526
VOUT
524
PG
528
525
+3V3
PG_+3V3
529
535
+2V5
PG_+2V5
539
545
+1V5
PG_+1V5
549
555
USB1_VCC
USB1_PWI
559
530
532
536
534
538
540
542
546
544
548
554
VIN
EN
VOUT
PG
Current Limit & S.C. Protect
FLT
550
556
558
552
+5V0
USB1_PWRON
551
553
Voltage Divider
521
523
565
+1V0_FIXED
562
566
564
568
560
569
575
+1V0_AVS_SOC
572
576
574
578
570
579
514
RESETB
514
RESETB
525
539
+3V3
PG_+2V5

FIG. 5

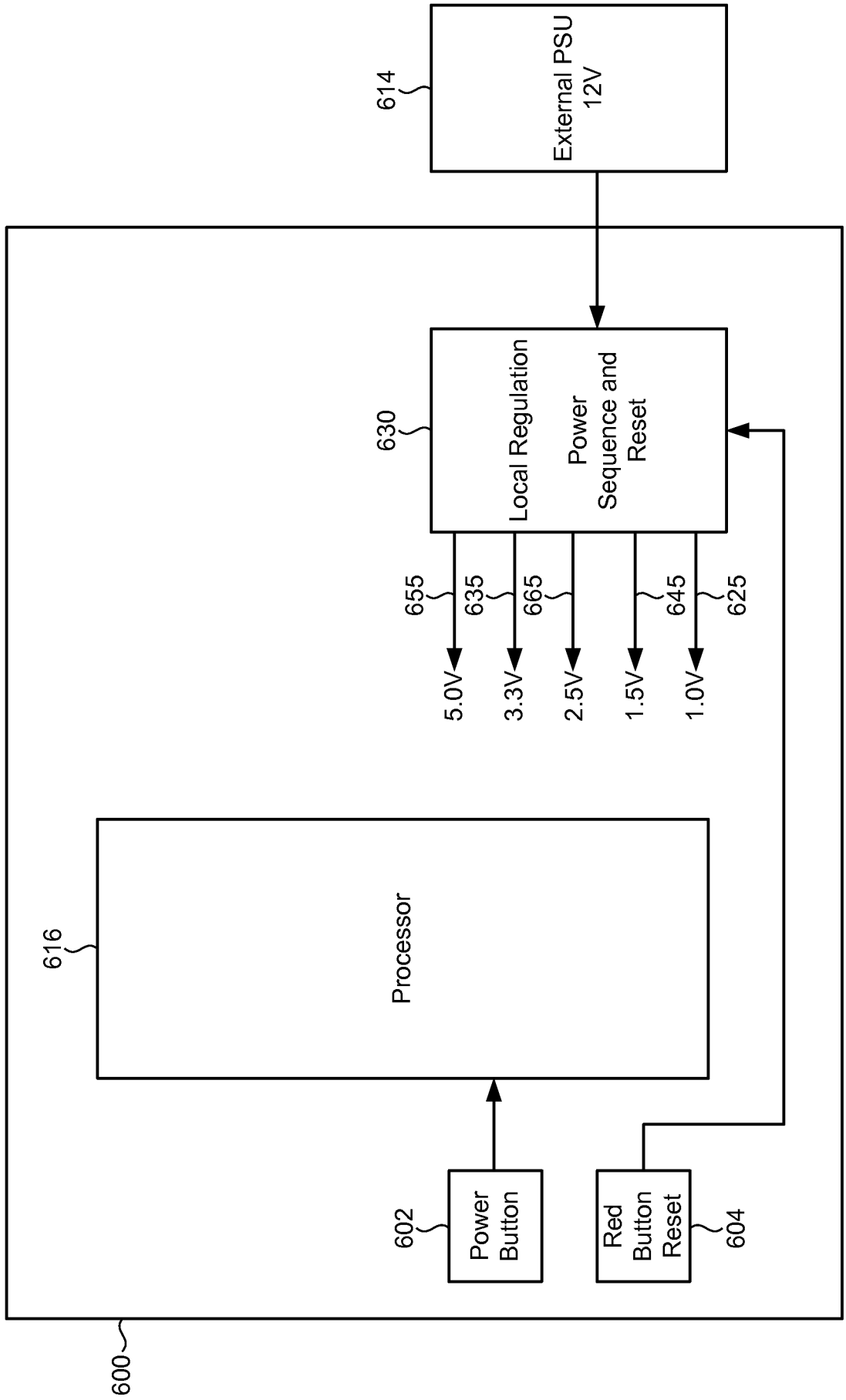
614
External PSU
12V
630
Local Regulation
Power
Sequence and
Reset
655
635
665
645
625
5.0V
3.3V
2.5V
1.5V
1.0V
616
Processor
602
Power
Button
Red
Button
Reset
604
600

FIG. 6

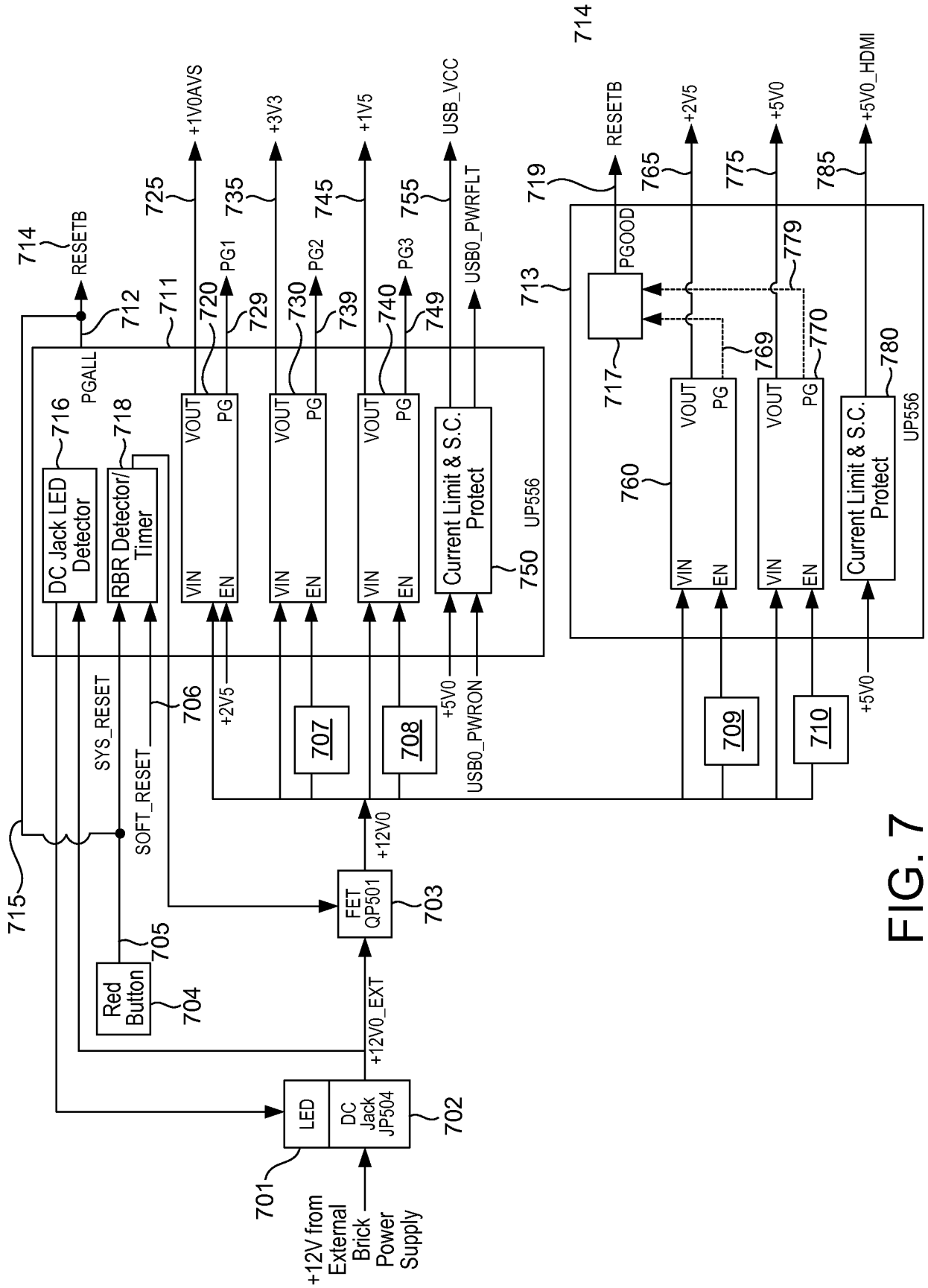
+12V from External Brick Power Supply
701
LED
DC Jack JP504
702
+12V0_EXT
Red Button
704
705
SYS_RESET
SOFT_RESET
706
715
FET QP501
703
+12V0
+2V5
+5V0
USB0_PWRON
707
708
709
710
DC Jack LED Detector
716
RBR Detector/ Timer
718
PGALL
RESETB
712
711
714
VIN
EN
VOUT
PG
720
729
PG1
725
+1V0AVS
730
739
PG2
735
+3V3
740
749
PG3
745
+1V5
USB0_PWRFLT
755
USB_VCC
Current Limit & S.C. Protect
750
UP556
713
717
PGOOD
719
RESETB
760
769
779
770
765
+2V5
775
+5V0
780
785
+5V0_HDMI
UP556

FIG. 7

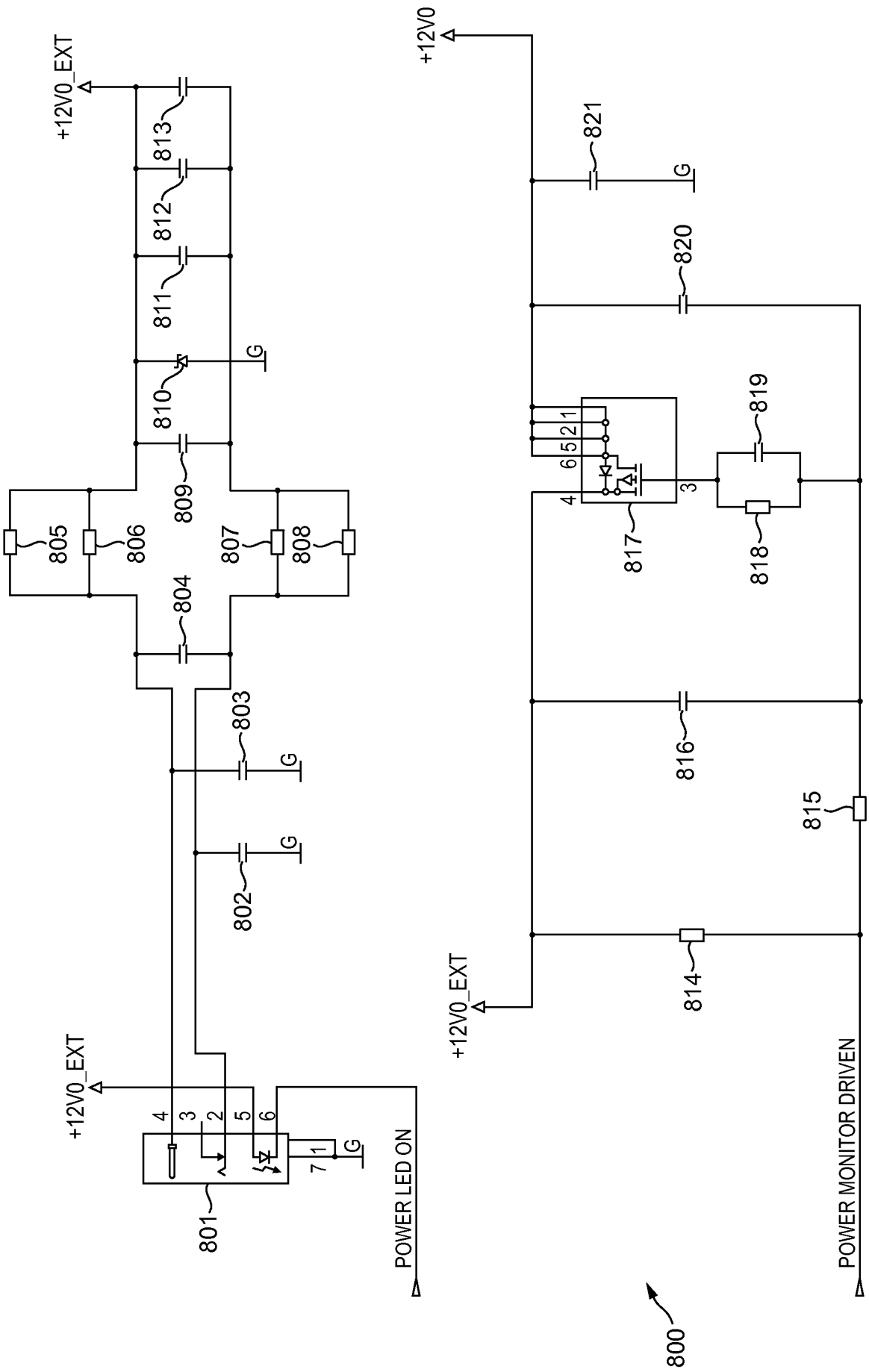
+12V0_EXT
813
812
811
810
809
805
806
807
808
804
803
802
801
+12V0_EXT
POWER LED ON
+12V0
821
820
819
817
818
816
815
814
+12V0_EXT
POWER MONITOR DRIVEN
800

FIG. 8

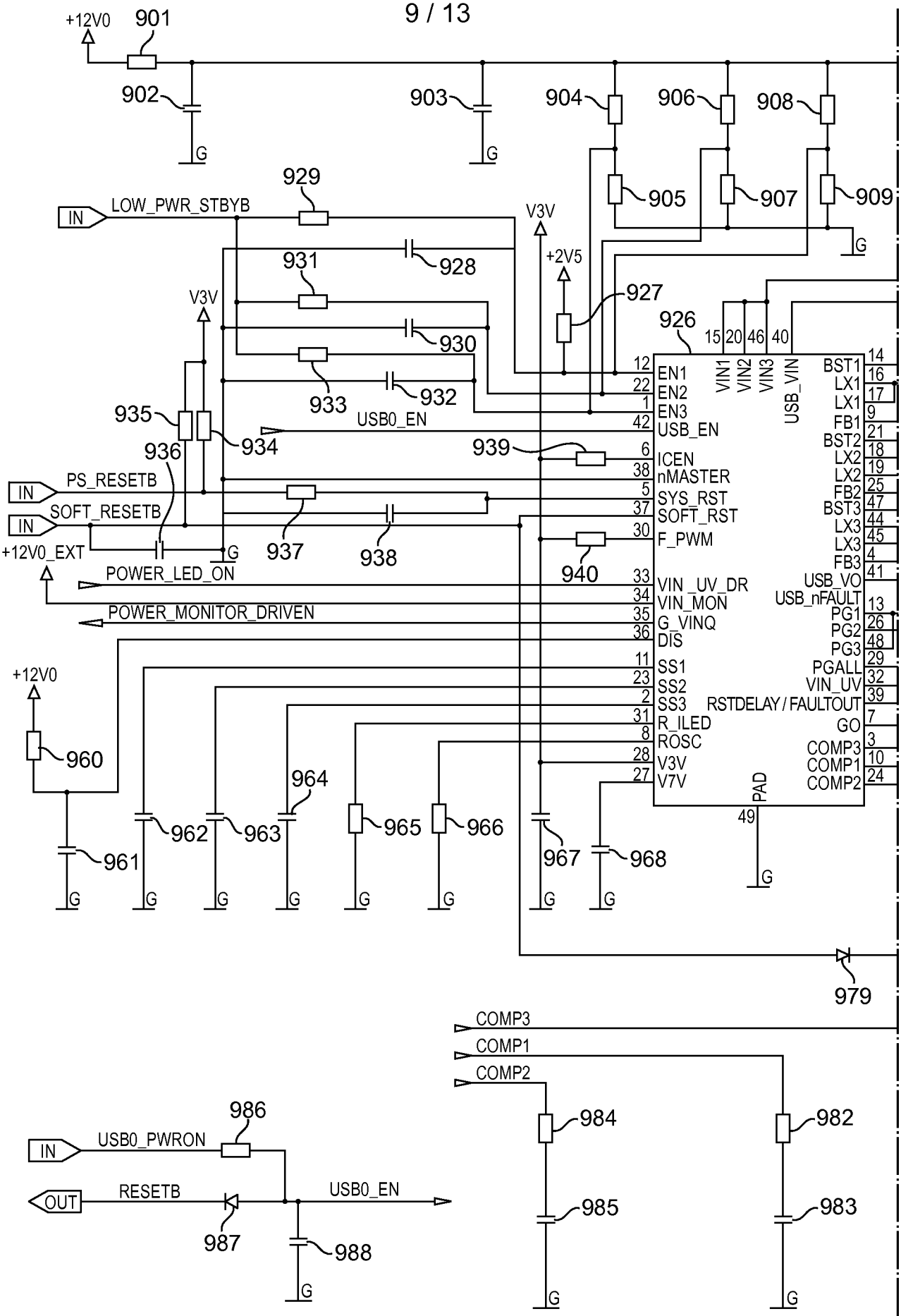
+12V0
901
902
903
904
906
908
905
907
909
929
IN
LOW_PWR_STBYB
V3V
931
928
+2V5
927
926
930
933
932
935
934
USB0_EN
936
939
PS_RESETB
SOFT_RESETB
937
938
940
+12V0_EXT
POWER_LED_ON
POWER_MONITOR_DRIVEN
960
961
962
963
964
965
966
967
968
979
EN1
EN2
EN3
USB_EN
ICEN
nMASTER
SYS_RST
SOFT_RST
F_PWM
VIN _UV_DR
VIN_MON
G_VINQ
DIS
SS1
SS2
SS3
R_ILED
ROSC
V3V
V7V
VIN1
VIN2
VIN3
USB_VIN
BST1
LX1
FB1
BST2
LX2
FB2
BST3
LX3
FB3
USB_VO
USB_nFAULT
PG1
PG2
PG3
PGALL
VIN_UV
RSTDELAY / FAULTOUT
GO
COMP3
COMP1
COMP2
PAD
COMP3
COMP1
COMP2
984
982
985
983
986
USB0_PWRON
RESETB
USB0_EN
987
988
OUT
G

FIG. 9a

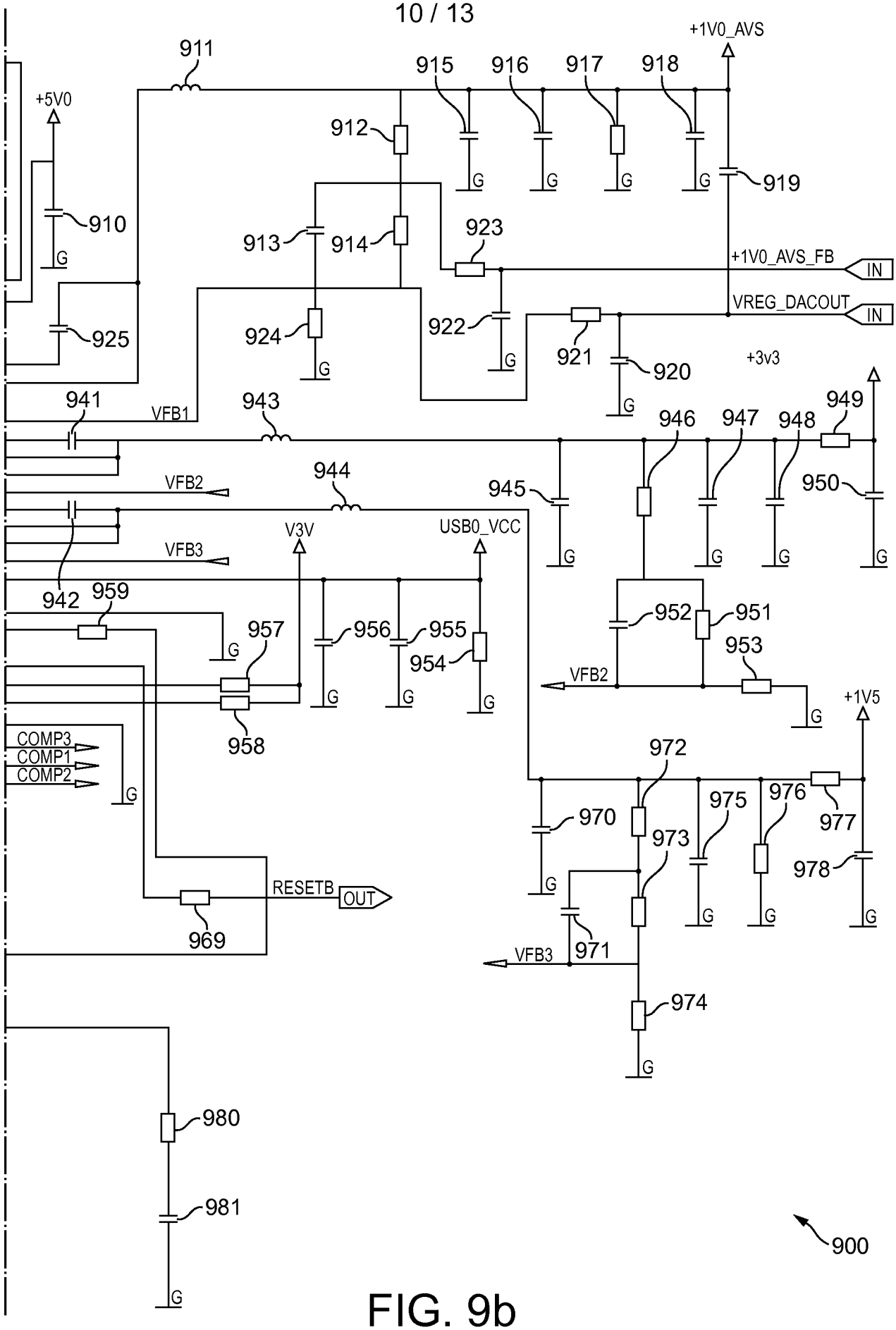
+1V0_AVS
911
915
916
917
918
+5V0
912
919
910
913
914
923
+1V0_AVS_FB
IN
VREG_DACOUT
IN
925
924
922
921
920
+3v3
941
VFB1
943
946
947
948
949
944
VFB2
945
950
V3V
USB0_VCC
VFB3
942
959
957
956
955
954
952
951
953
VFB2
+1V5
COMP3
COMP1
COMP2
958
972
970
975
976
977
973
978
RESETB
OUT
969
971
VFB3
974
980
981
900
G

FIG. 9b

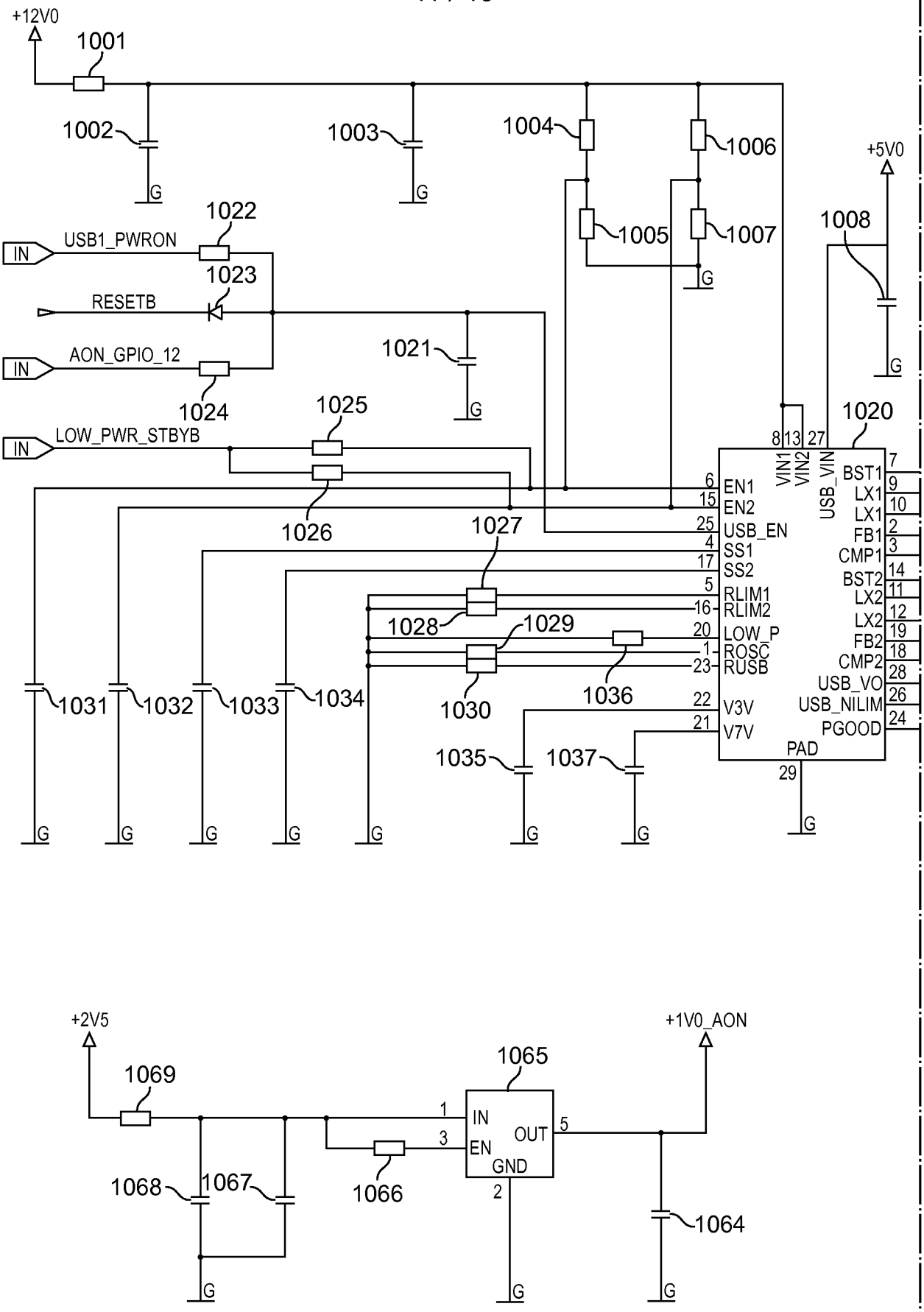
+12V0
1001
1002
1003
1004
1006
1005
1007
1008
+5V0
1022
USB1_PWRON
IN
1023
RESETB
AON_GPIO_12
1021
1024
1025
LOW_PWR_STBYB
1020
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
EN1
EN2
USB_EN
SS1
SS2
RLIM1
RLIM2
LOW_P
ROSC
RUSB
V3V
V7V
VIN1
VIN2
USB_VIN
BST1
LX1
LX1
FB1
CMP1
BST2
LX2
LX2
FB2
CMP2
USB_VO
USB_NILIM
PGOOD
PAD
G
+2V5
1069
1065
1068
1067
1066
IN
EN
OUT
GND
+1V0_AON
1064

FIG. 10a

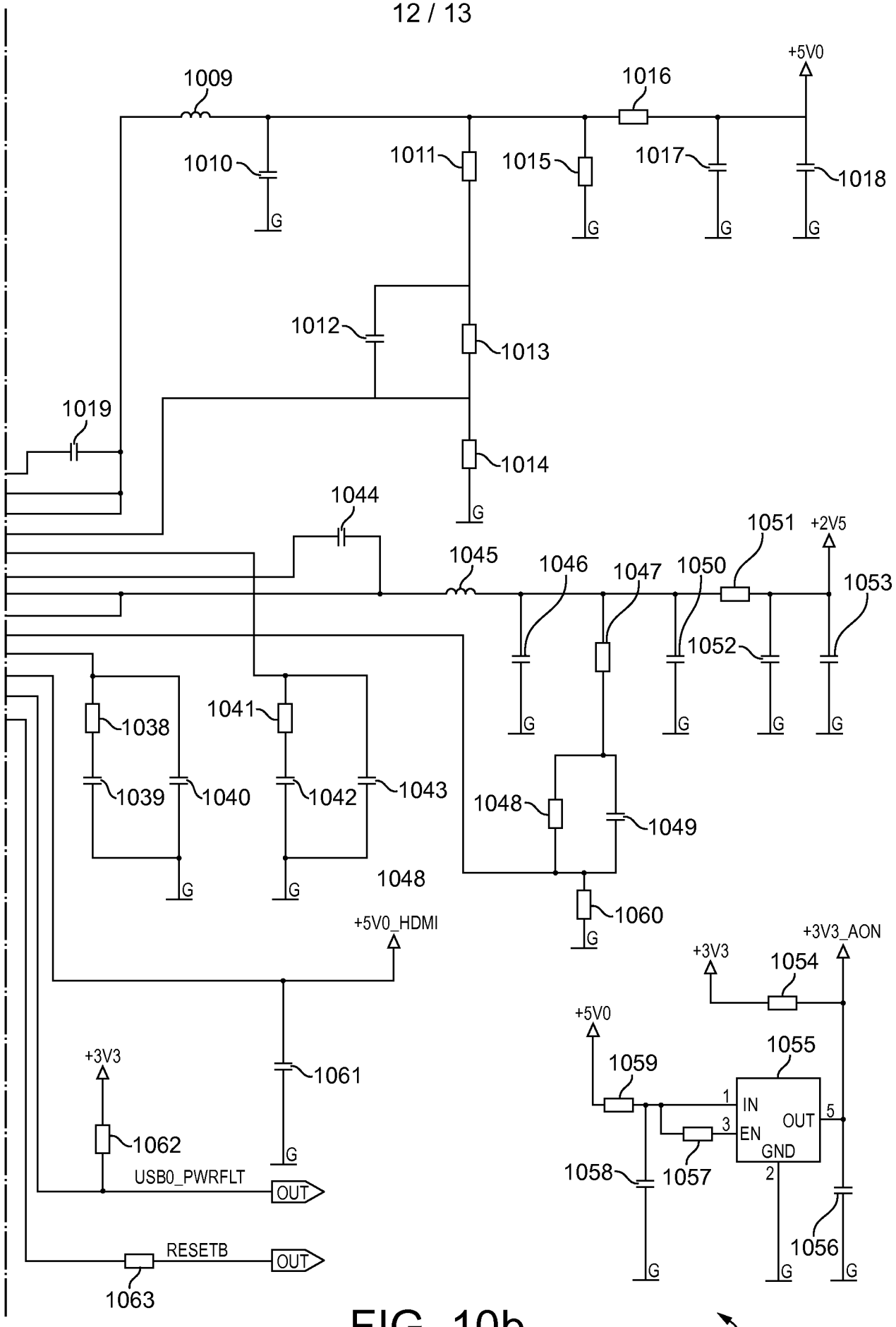
+5V0
1009
1016
1010
1011
1015
1017
1018
G
1012
1013
1019
1014
1044
1051
+2V5
1045
1046
1047
1050
1053
1052
1038
1041
1039
1040
1042
1043
1048
1049
1060
+5V0_HDMI
+3V3_AON
+3V3
1054
1061
1059
1055
1062
IN
OUT
EN
GND
1058
1057
1056
USB0_PWRFLT
OUT
RESETB
1063
1000

FIG. 10b

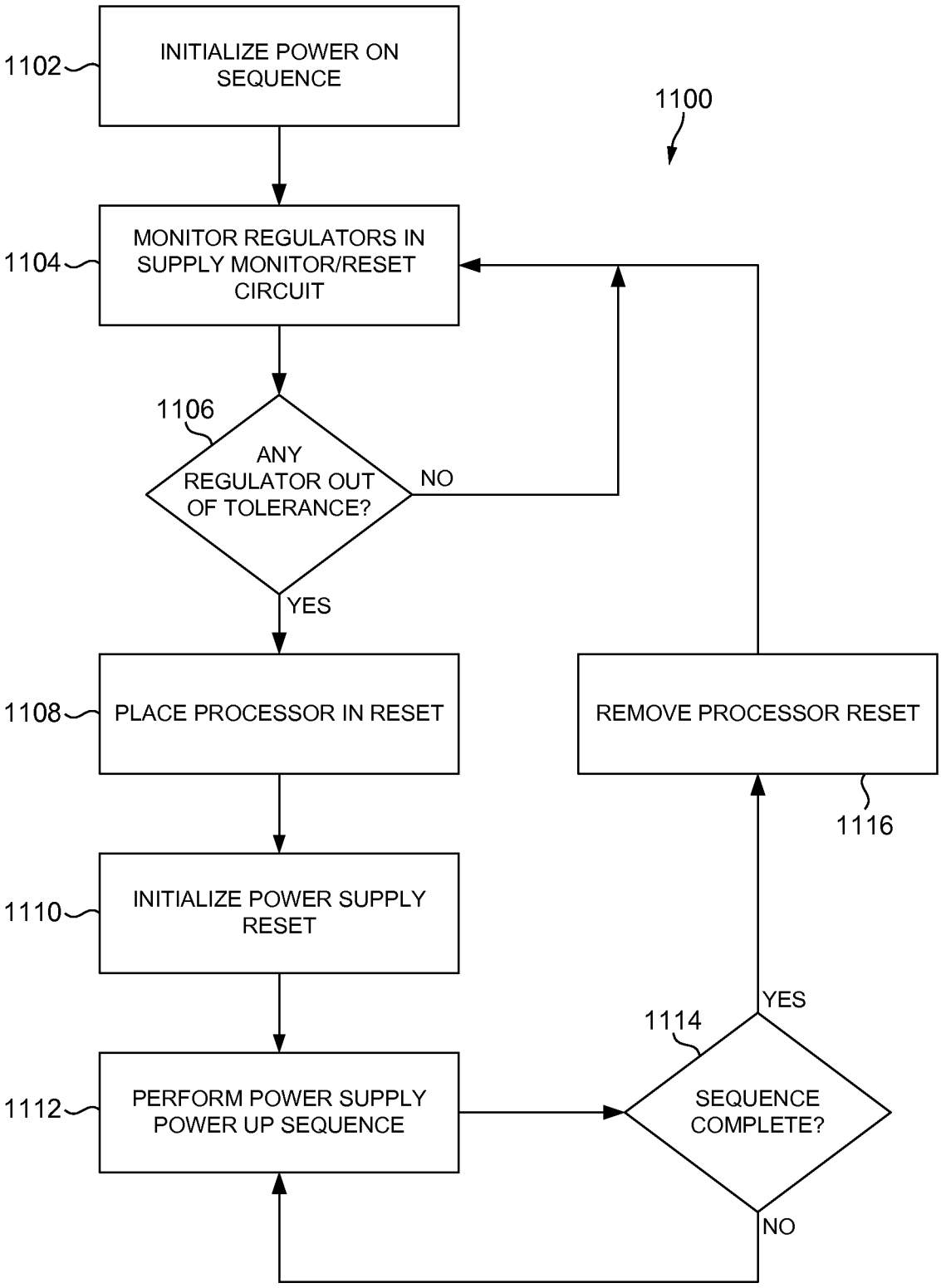
1102
INITIALIZE POWER ON SEQUENCE
1100
1104
MONITOR REGULATORS IN SUPPLY MONITOR/RESET CIRCUIT
1106
ANY REGULATOR OUT OF TOLERANCE?
NO
YES
1108
PLACE PROCESSOR IN RESET
REMOVE PROCESSOR RESET
1116
1110
INITIALIZE POWER SUPPLY RESET
YES
1114
1112
PERFORM POWER SUPPLY POWER UP SEQUENCE
SEQUENCE COMPLETE?
NO

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/052778

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F1/30 G06F1/28 G06F1/24 G06F11/30 G06F11/07
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 2 003 532 A2 (DENSO CORP [JP]) 17 December 2008 (2008-12-17) paragraph [0023] - paragraph [0045] paragraph [0065] - paragraph [0066] paragraph [0082] figure 1 -----	1-20
X	US 7 100 058 B1 (TOMLINSON JOCK F [US] ET AL) 29 August 2006 (2006-08-29) column 2, line 5 - column 3, line 18 column 4, line 10 - column 5, line 34 column 6, line 12 - line 30 column 11, line 54 - column 12, line 24 figures 1,2,7 -----	1-20
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 November 2015	16/11/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Knutsson, Frédéric

1

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/052778

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014/070616 A1 (SHIH TSUN-TE [TW] ET AL) 13 March 2014 (2014-03-13) paragraph [0005] - paragraph [0009] paragraph [0014] - paragraph [0018] figure 2 -----	1-20

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2015/052778

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 2003532 A2	17-12-2008	EP 2003532 A2	17-12-2008
		JP 4345845 B2	14-10-2009
		JP 2008289254 A	27-11-2008
		US 2008284389 A1	20-11-2008
US 7100058 B1	29-08-2006	US 7100058 B1	29-08-2006
		US 2002104031 A1	01-08-2002
US 2014070616 A1	13-03-2014	NONE	