(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 March 2021 (18.03.2021)

WIPO | PCT

(10) International Publication Number
WO 2021/050239 A1

(51) International Patent Classification:
H02M 1/32 (2007.01) *H02M 3/158* (2006.01)
H02M 3/156 (2006.01) *H02M 1/00* (2006.01)

(21) International Application Number:
PCT/US2020/047237

(22) International Filing Date:
20 August 2020 (20.08.2020)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/899,415 12 September 2019 (12.09.2019) US
16/916,395 30 June 2020 (30.06.2020) US

(71) Applicant: **CIRRUS LOGIC INTERNATIONAL SEMICONDUCTOR LTD.** [GB/GB]; 7B Nightingale Way, Quartermile, Edinburgh EH3 9EG (GB).

(72) Inventor; and

(71) Applicant *(for US only)*: **KING, Eric J.** [US/US]; c/o Cirrus Logic Inc., 800 West 6th Street, Austin, Texas 78701 (US).

(72) Inventors: **SHARMA, Ajit**; c/o Cirrus Logic Inc., 800 West 6th Street, Austin, Texas 78701 (US). **ZHANG, Lingli**; c/o Cirrus Logic Inc., 800 West 6th Street, Austin, Texas 78701 (US). **LARSEN, Christian**; c/o Cirrus Logic Inc., 800 West 6th Street, Austin, Texas 78701 (US). **MACKAY, Graeme G.**; c/o Cirrus Logic Inc., 800 West 6th Street, Austin, Texas 78701 (US).

(54) Title: EFFICIENT USE OF ENERGY IN A SWITCHING POWER CONVERTER

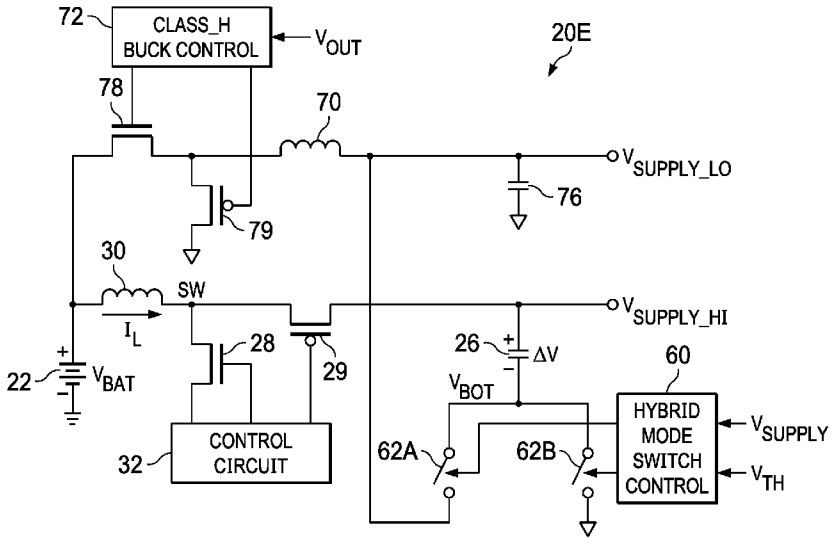

FIG. 8

(57) Abstract: A system may include a power converter having a maximum allowable input power drawn from a power source, an energy storage element coupled to an output of the power converter at a top plate of the energy storage element, wherein the energy storage element is configured to store excess energy, and control circuity configured to, when an input power of the power converter exceeds the maximum allowable input power, cause excess energy stored in the energy storage element to be consumed by circuitry coupled to the output of the power converter, and in order to maintain positive voltage headroom for the circuitry coupled to the output of the power converter, selectively couple a bottom plate of the energy storage element to the power source such that excess energy stored by the circuitry coupled to the output of the power converter is consumed from the energy storage device when the input power of the power converter exceeds the maximum allowable input power.

WO 2021/050239 A1

[Continued on next page]

(74) **Agent: PREWITT, Brian K.** et al.; JACKSON WALKER L.L.P., 100 Congress Avenue, Suite 1100, Austin, Texas 78701 (US).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

EFFICIENT USE OF ENERGY IN A SWITCHING POWER CONVERTER

FIELD OF DISCLOSURE

The present disclosure relates in general to circuits for electronic devices, including without limitation personal audio devices such as wireless telephones and media players, and more specifically, to limited average current in a peak-controlled boost converter.

BACKGROUND

Personal audio devices, including wireless telephones, such as mobile/cellular telephones, cordless telephones, mp3 players, and other consumer audio devices, are in widespread use. Such personal audio devices may include circuitry for driving a pair of headphones or one or more speakers. Such circuitry often includes a speaker driver including a power amplifier for driving an audio output signal to headphones or speakers. Oftentimes, a power converter may be used to provide a supply voltage to a power amplifier in order to amplify a signal driven to speakers, headphones, or other transducers. A switching power converter is a type of electronic circuit that converts a source of power from one direct current (DC) voltage level to another DC voltage level. Examples of such switching DC-DC converters include but are not limited to a boost converter, a buck converter, a buck-boost converter, an inverting buck-boost converter, and other types of switching DC-DC converters. Thus, using a power converter, a DC voltage such as that provided by a battery may be converted to another DC voltage used to power the power amplifier.

Often, boost converters operate as peak current-controlled boost converters, wherein a main control loop of a control system is used to determine a peak current requirement on each switching phase of the boost converter in order to generate a desired boosted output voltage of the boost converter. For boost duty cycles where a duty cycle (e.g., which may be determined by subtracting an arithmetic ratio from the number one, wherein the arithmetic ratio equals the input voltage supplied to the boost converter divided by the boost output voltage of the boost converter), slope compensation circuitry may be required to avoid sub-harmonic behavior of the boost converter. Also present in many boost converter control systems is protection circuitry to ensure that the current of a boost converter is maintained below a maximum value. The detection of the peak current in

accordance with the main control loop and detection of the maximum allowable current is often performed by two separate circuits: a first comparator comparing a measured current (e.g., measured current of a power inductor of the boost converter) with a slope-compensated target peak current signal and a second comparator comparing the measured current to the maximum current limit. The main control loop, which may also be known as a compensator, may generate a target peak current signal which may be modified by slope compensation circuitry, and such slope-compensated target peak current signal may be compared by the first comparator to the measured current in order to perform peak-current control of a boost converter. However, because slope compensation may occur in analog circuitry, an unknown amount of correction may exist at the point the first comparator toggles. Such error may be removed by the main control loop in regulating the boosted voltage output by the power converter.

However, the presence of this unknown error may result in the inability to directly control the maximum current during any specific switching cycle of the boost converter. This lack of control occurs because the second comparator allows for a measurement without slope compensation of the inductor current above a threshold. If the second comparator is used to control the current in the inductor directly, the lack of slope compensation on this measurement may result in sub-harmonic behavior. To avoid such sub-harmonic behavior while limiting the current as detected by the second comparator, the output of the second comparator may be fed back to allow control circuity to apply desired limit behavior to the slope-compensated target peak current signal. For example, an additional control loop may be present such that when operating under the current-limited condition, the slope-compensated target peak current signal is modified to obtain the desired limited current behavior.

As a result, a control system may be created that results in limiting and controlling the peak current of a power inductor of a boost converter below a maximum threshold. However, in many systems, an error between the peak inductor current and the average inductor current can be quite large and inductor variation can lead to significant challenges in determining a proper peak current limitation.

SUMMARY

In accordance with the teachings of the present disclosure, one or more disadvantages and problems associated with existing approaches to operating a power converter may be reduced or eliminated.

In accordance with embodiments of the present disclosure, a system may include a power converter having a maximum allowable input power drawn from a power source, an energy storage element coupled to an output of the power converter at a top plate of the energy storage element, wherein the energy storage element is configured to store excess energy, and control circuity configured to, when an input power of the power converter exceeds the maximum allowable input power, cause excess energy stored in the energy storage element to be consumed by circuitry coupled to the output of the power converter, and in order to maintain positive voltage headroom for the circuitry coupled to the output of the power converter, selectively couple a bottom plate of the energy storage element to the power source such that excess energy stored by the circuitry coupled to the output of the power converter is consumed from the energy storage device when the input power of the power converter exceeds the maximum allowable input power.

In accordance with these and other embodiments of the present disclosure, a system may include a power converter configured to generate a first supply voltage at a first supply output and a second supply output configured to generate a second supply voltage lower than the first supply voltage, wherein the second supply voltage tracks an envelope of an output signal generated by an amplifier coupled to the power supply.

In accordance with these and other embodiments of the present disclosure, a system may include a power supply comprising a power converter configured to generate a first supply voltage at a first supply output of the power supply and a second supply output configured to generate a second supply voltage lower than the first supply voltage. The system may also include an amplifier coupled to the power supply and configured to select between the first supply voltage and the second supply voltage as a supply voltage to the amplifier.

In accordance with these and other embodiments of the present disclosure, a system may include a power converter configured to generate a first supply voltage at a first supply output of the power supply, the power converter having a maximum allowable input power drawn from a power source, an energy storage element coupled to an output of the power

converter at a top plate of the energy storage element, wherein the energy storage element is configured to store excess energy, and a second supply output configured to generate a second supply voltage lower than the first supply voltage. The second supply voltage may track an envelope of an output signal generated by an amplifier coupled to the power supply when the amplifier consumes power from the second supply output and the second supply voltage may regulate a voltage at a bottom plate of the energy storage element when the amplifier consumes power from the first supply output.

In accordance with these and other embodiments of the present disclosure, a method may include, in a system having a power converter having a maximum allowable input power drawn from a power source and an energy storage element coupled to an output of the power converter at a top plate of the energy storage element, wherein the energy storage element is configured to store excess energy: when an input power of the power converter exceeds the maximum allowable input power, causing excess energy stored in the energy storage element to be consumed by circuitry coupled to the output of the power converter, and in order to maintain positive voltage headroom for the circuitry coupled to the output of the power converter, selectively coupling a bottom plate of the energy storage element to the power source such that excess energy stored by the circuitry coupled to the output of the power converter is consumed from the energy storage device when the input power of the power converter exceeds the maximum allowable input power.

In accordance with these and other embodiments of the present disclosure, a method may include generating a first supply voltage at a first supply output with a power converter and generating a second supply voltage lower than the first supply voltage with a second supply output, wherein the second supply voltage tracks an envelope of an output signal generated by an amplifier coupled to the power supply.

In accordance with these and other embodiments of the present disclosure, a method may include generating a first supply voltage of a power supply at a first supply output with a power converter, generating a second supply voltage of the power supply lower than the first supply voltage with a second supply output, and selecting, by an amplifier coupled to the power supply, between the first supply voltage and the second supply voltage as a supply voltage to the amplifier.

In accordance with these and other embodiments of the present disclosure, a method may be provided for use in a system having a power converter configured to generate a first

supply voltage at a first supply output of the power supply, the power converter having a maximum allowable input power drawn from a power source, an energy storage element coupled to an output of the power converter at a top plate of the energy storage element, wherein the energy storage element is configured to store excess energy, and a second supply output configured to generate a second supply voltage lower than the first supply voltage. The method may include tracking, with the second supply voltage, an envelope of an output signal generated by an amplifier coupled to the power supply when the amplifier consumes power from the second supply output and regulating, with the second supply voltage, a voltage at a bottom plate of the energy storage element when the amplifier consumes power from the first supply output.

Technical advantages of the present disclosure may be readily apparent to one skilled in the art from the figures, description and claims included herein. The objects and advantages of the embodiments will be realized and achieved at least by the elements, features, and combinations particularly pointed out in the claims.

It is to be understood that both the foregoing general description and the following detailed description are examples and explanatory and are not restrictive of the claims set forth in this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present embodiments and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

FIGURE 1 illustrates an example personal audio device, in accordance with embodiments of the present disclosure;

FIGURE 2 illustrates a block diagram of selected components of an example integrated circuit of a personal audio device, in accordance with embodiments of the present disclosure;

FIGURE 3 illustrates a block diagram of selected components of an example hybrid peak-current control boost converter with average current limit control which may be used to implement the power supply shown in FIGURE 2, in accordance with embodiments of the present disclosure;

FIGURE 4 illustrates graphs depicting example waveforms for actual inductor current and target average inductor current versus time and for a mathematical integral of a difference of the quantity of the target average inductor current and the actual inductor current target, in accordance with embodiments of the present disclosure;

FIGURE 5 illustrates graphs depicting example waveforms for selected voltages within the example hybrid peak-current control boost converter shown in FIGURE 3, in accordance with embodiments of the present disclosure;

FIGURE 6 illustrates a block diagram of selected components of another example integrated circuit of a personal audio device, in accordance with embodiments of the present disclosure;

FIGURE 7A illustrates a block diagram of selected components of an example power converter which may be used to implement the power supply shown in FIGURE 6, in accordance with embodiments of the present disclosure;

FIGURE 7B illustrates a block diagram of selected components of another example power converter which may be used to implement the power supply shown in FIGURE 6, in accordance with embodiments of the present disclosure;

FIGURE 7C illustrates a block diagram of selected components of yet another example power converter which may be used to implement the power supply shown in FIGURE 6, in accordance with embodiments of the present disclosure;

FIGURE 8 illustrates a block diagram of selected components of another example hybrid power converter which may be used to implement the power supply shown in FIGURE 6, in accordance with embodiments of the present disclosure;

FIGURE 9 illustrates graphs depicting example waveforms for selected voltages within the example hybrid power converter shown in FIGURE 8, in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

FIGURE 1 illustrates an example personal audio device 1, in accordance with embodiments of the present disclosure. FIGURE 1 depicts personal audio device 1 coupled to a headset 3 in the form of a pair of earbud speakers 8A and 8B. Headset 3 depicted in FIGURE 1 is merely an example, and it is understood that personal audio device 1 may be used in connection with a variety of audio transducers, including without limitation,

headphones, earbuds, in-ear earphones, and external speakers. A plug 4 may provide for connection of headset 3 to an electrical terminal of personal audio device 1. Personal audio device 1 may provide a display to a user and receive user input using a touch screen 2, or alternatively, a standard liquid crystal display (LCD) may be combined with various buttons, sliders, and/or dials disposed on the face and/or sides of personal audio device 1. As also shown in FIGURE 1, personal audio device 1 may include an audio integrated circuit (IC) 9 for generating an analog audio signal for transmission to headset 3 and/or another audio transducer.

FIGURE 2 illustrates a block diagram of selected components of an example IC 9A of a personal audio device, in accordance with embodiments of the present disclosure. In some embodiments, example IC 9A shown in FIGURE 2 may be used to implement IC 9 of FIGURE 1. As shown in FIGURE 2, a microcontroller core 18 may supply a digital input signal DIG_IN to a digital-to-analog converter (DAC) 14, which may convert the digital input signal to an analog signal V_{IN}. DAC 14 may supply analog signal V_{IN} to an amplifier 16 which may amplify or attenuate input signal V_{IN} to provide a differential output signal V_{OUT}, which may operate a speaker, a headphone transducer, a line level signal output, and/or other suitable output. In some embodiments, DAC 14 may be an integral component of amplifier 16. A power supply 10A may provide the power supply rail inputs of amplifier 16. In some embodiments, power supply 10A may comprise a switched-mode power converter, as described in greater detail below. Although FIGURES 1 and 2 contemplate that IC 9A resides in a personal audio device, systems and methods described herein may also be applied to electrical and electronic systems and devices other than a personal audio device, including systems for use in a computing device larger than a personal audio device, such as an automobile, a building, or other structure. Further, systems and methods described herein may also be applied to electrical and electronic systems and devices other than audio devices and audio transducers, such as vibro-haptic transducers, piezoelectric transducers, or other transducers.

FIGURE 3 illustrates a block diagram of selected components of an example hybrid peak-current control boost converter 20A with average current limit control which may be used to implement power supply 10A shown in FIGURE 2, in accordance with embodiments of the present disclosure. As shown in FIGURE 3, boost converter 20A may include a battery 22, a power inductor 30, a switch 28 implemented as an n-type metal-

oxide-semiconductor field-effect transistor (NFET), a switch 29 implemented as a p-type metal-oxide-semiconductor field-effect transistor (PFET), and a control circuit 32. FIGURE 4 illustrates graphs depicting example waveforms for actual inductor current I_L and target average inductor current I_{AVG_LIM} versus time and for a mathematical integral of a difference of the quantity of target average inductor current I_{AVG_LIM} and actual inductor current I_L, in accordance with embodiments of the present disclosure.

In a first phase (labeled as "Phase A" in FIGURE 4) of a switching cycle of boost converter 20A, control circuit 32 may cause switch 28 to be activated (e.g., closed, turned on, enabled) and switch 29 to be deactivated (e.g., opened, turned off, disabled). Thus, during the first phase, a switch node (labeled as "SW" in FIGURE 3) may be effectively shorted to a ground potential, such that battery 22 applies its voltage V_{BAT} across terminals of power inductor 30. As a result, an inductor current I_L flowing in power inductor 30 may increase during the first phase. As described in greater detail below, control circuit 32 may cause inductor current I_L to increase until such point that inductor current I_L reaches a slope-compensated peak current limit I_{PK}', at which the first phase may end.

In a second phase (labeled as "Phase B" in FIGURE 4) of the switching cycle of boost converter 20A, control circuit 32 may cause switch 28 to be deactivated and switch 29 to be activated. As a result, inductor current I_L may decrease during the second phase as power inductor 30 discharges into boost capacitor 26, boosting the supply voltage V_{SUPPLY} to a voltage higher than battery voltage V_{BAT}. In continuous conduction mode (CCM), the second phase (Phase B) may continue until the end of the switching cycle, after which the first phase (Phase A) again occurs, as shown in FIGURE 4. In discontinuous conduction mode (DCM), the second phase (Phase B) may continue until inductor current I_L reaches zero, at which point a third phase (not shown in FIGURE 4) of the switching cycle may begin. In the third phase, if it exists, control circuit 32 may cause both of switches 28 and 29 to be deactivated, and inductor current I_L may remain at zero until the beginning of the next switching cycle, in which the first phase (Phase A) again occurs. In some embodiments, control circuit 32 may deactivate switch 29 during the second phase (Phase B), such that a body diode of the PFET implementing switch 29 conducts inductor current I_L until it reaches zero.

As its name suggests, hybrid peak-current control boost converter 20A may operate in one of at least two modes. In a first mode, switch 62B may be activated (e.g., on, closed,

enabled) and switch 62A may be deactivated (e.g., off, open, disabled) such that a bottom plate of boost capacitor 26 corresponding to the negative terminal of supply voltage V_{SUPPLY} is coupled to ground voltage. In a second mode, switch 62A may be activated and switch 62B may be deactivated such that a bottom plate of boost capacitor 26 (e.g., opposite of the top plate of boost capacitor 26 at which supply voltage V_{SUPPLY} is present) is coupled to battery voltage V_{BAT}. Switching between the first mode and the second mode may be controlled by a hybrid mode switch controller 60. Hybrid mode switch controller 60 may be configured to transition from operation in the first mode to operation in the second mode when voltage ΔV across boost capacitor 26 drops below a predetermined threshold voltage V_{TH}. In addition, hybrid mode switch controller 60 may be configured to transition from operation in the second mode to operation in the first mode when voltage ΔV across boost capacitor 26 rises above a predetermined threshold voltage V_{TH}. The calculation of voltage ΔV may be either a direct measurement or may be calculated from supply voltage V_{SUPPLY}, the knowledge of switch states of switches 62A and 62B, the variable voltage provided by low-dropout regulator 58, and/or battery voltage V_{BAT}.

In some embodiments, control circuit 32 may be configured to selectively enable and disable coupling of the bottom plate of capacitor 26 to battery 22 at a first switching frequency significantly less than a second switching frequency at which switches 28 and 29 of hybrid peak-current control boost converter 20A are switched.

In these and other embodiments, control circuit 32 may be configured to selectively enable and disable coupling of the bottom plate of capacitor 26 to battery 22 at a switching frequency related to another frequency of a signal driven to a load an amplifier (e.g., amplifier 16) powered from hybrid peak-current control boost converter 20A. In these and other embodiments, control circuit 32 may be configured to selectively enable and disable coupling of the bottom plate of capacitor 26 to battery 22 at a switching frequency related to another frequency of a signal driven to a load by an amplifier (e.g., amplifier 16) powered from hybrid peak-current control boost converter 20A.

Although not shown in FIGURE 3, in some embodiments, hybrid mode switch controller 60 may operate with hysteresis, such that a threshold voltage V_{TH} for switching from the first mode to the second mode may be lower than a threshold voltage V_{TH} for switching from the second mode to the first mode.

To further illustrate hybrid operation between the first mode and the second mode, FIGURE 5 illustrates graphs depicting example waveforms for selected voltages of example hybrid peak-current control boost converter 20A when switched between the first mode and the second mode and between the second mode and the first mode, in accordance with embodiments of the present disclosure.

As shown in FIGURE 5, as a magnitude of output signal V_{OUT} generated by amplifier 16 increases, a droop in supply voltage V_{SUPPLY} supplying amplifier 16 may occur. Such droop may occur because the current drawn by the hybrid peak-current control boost converter 20A from battery 22 may be limited by the circuitry shown in FIGURE 3. This limited current may be required to protect battery 22 and/or to avoid brownout on other devices using battery 22 as a source of energy. Such droop in supply voltage V_{SUPPLY} may be due to the load connected to the output of hybrid peak-current control boost converter 20A demanding more power than the limited operation of hybrid peak-current control boost converter 20A is able provide. As such, when such droop occurs, the stored energy on capacitor 26 may be used to provide the necessary power to the load.

If such droop were to cause supply voltage V_{SUPPLY} to drop below the magnitude of output signal V_{OUT}, clipping or other distortion may occur in output signal V_{OUT}. Accordingly, when supply voltage V_{SUPPLY} drops below threshold voltage V_{TH}, at a time labeled t_1 in FIGURE 5, hybrid mode switch controller 60 may cause transition between the first mode (in which the bottom plate of boost capacitor 26 is coupled to ground) to the second mode (in which the bottom plate of boost capacitor 26 is coupled to battery voltage V_{BAT}). As a result, a bottom plate voltage V_{BOT} at the bottom plate of boost capacitor 26 may rise from zero to battery voltage V_{BAT}. Furthermore, because a voltage ΔV across boost capacitor 26 cannot instantaneously change, the increase in bottom plate voltage V_{BOT} may cause a similar increase in supply voltage V_{SUPPLY} (e.g., $V_{SUPPLY} = V_{BOT} + \Delta V$), ensuring supply voltage V_{SUPPLY} remains above output signal V_{OUT} by allowing hybrid peak-current control boost converter 20A to transfer more energy from boost capacitor 26 to amplifier 16 than would be possible if peak-current control boost converter 20A only operated in the first mode with the bottom plate of boost capacitor 26 coupled to ground. In fact, in particular implementations, hybrid operation between the two modes described herein may allow hybrid peak-current control boost converter 20A to utilize 1.8 times more energy (or would allow utilization of the same amount of energy with a boost capacitor 1.8

times smaller) than if peak-current control boost converter 20A only operated in the first mode with the bottom plate of boost capacitor 26 coupled to ground.

As shown in FIGURE 3, hybrid peak-current control boost converter 20A may include a low-dropout regulator 58 coupled between battery 22 and switch 62A. In operation, hybrid mode switch controller 60 may, when switching hybrid operation from the first mode to the second mode and vice versa, control a voltage across low-dropout regulator 58 to allow for a controlled ramping of bottom plate voltage V_{BOT} between zero and battery voltage V_{BAT} and vice versa, in order to eliminate high-frequency switching artifacts that may occur in output signal V_{OUT} due to sudden changes in supply voltage V_{SUPPLY}.

Also as depicted in FIGURE 3, hybrid peak-current control boost converter 20A may include a current sensor circuit 56 to sense current I_{BOT} flowing through boost capacitor 26. Current sensor circuit 56 may measure current I_{BOT} using a sense resistor with resistance R_{BOT}. In some embodiments, R_{BOT} may have a resistance of approximately 10 mΩ. As described in greater detail below, measured current I_{BOT} may be used by control circuit 32.

Turning back to FIGURE 3, control circuit 32 may include a compensator 34, current average limit control block 35, a multiplexer 37, a current sensor circuit 36, a digital-to-analog converter (DAC) 38, a DAC 40, a slope generator 42, a peak current comparator 44, a clock (CLK) generator 46, a latch 48, switch block control 50, integrator 52, integrator comparator 54, and latch 56.

In operation in both CCM and DCM, the duty cycle of switch 28 (e.g., the duration of the first phase (Phase A)) may determine the magnitude of supply voltage V_{SUPPLY} relative to battery voltage V_{BAT}. For example, in CCM, the duty cycle D needed to provide a desired supply voltage V_{SUPPLY} may be given by $D = 1 - V_{BAT}/V_{SUPPLY}$. Thus, for a desired level of supply voltage V_{SUPPLY} (e.g., which may be based on an envelope of an output signal of an amplifier), control circuit 32 may implement a feedback control loop, which may be internal to compensator 34, based on measured supply voltage V_{SUPPLY} and measured inductor current I_L, which may be measured by current sensor circuit 36 (e.g., using a sense resistor with resistance R_{SENSE}; in some embodiments, R_{SENSE} may have a resistance of approximately 10 mΩ). Thus, control circuit 32 may monitor actual supply voltage V_{SUPPLY}, compare it against a desired supply voltage V_{SUPPLY}, and increase or

decrease actual supply voltage V_{SUPPLY} by increasing or decreasing the peak of inductor current I_L. In that vein, compensator 34 may generate a digital signal indicative of a desired peak current, and DAC 38 may, when multiplexer 37 is selected to output the output of compensator 34, convert such digital signal into an analog equivalent peak current signal I_{PK}. Further, as shown in FIGURE 3, measured current I_{BOT} through boost capacitor 26 may be subtracted from peak current signal I_{PK} to compensate for current from battery 22 that charges boost capacitor 26, as opposed to inductor current I_L charging boost capacitor 26.

Slope generator 42 may generate a slope compensation signal. In some embodiments, slope generator 42 may generate the slope compensation signal as a triangle or sawtooth waveform. The slope compensation signal may be combined with peak current signal I_{PK} to generate slope-compensated peak current signal I_{PK}'. Peak current comparator 44 may, during the first phase (Phase A), compare a measured inductor current I_L (e.g., measured by a current sensor circuit 36), generating a control signal responsive to the comparison. Together, the output of comparator 44, clock generator 46, and latch 48 may be arranged as shown, or arranged in another suitable manner, to generate a control signal to switch control block 50. For example, clock generator 46 may generate a clock signal indicating the beginning of a switching cycle (e.g., beginning of the first phase/Phase A) and comparator 44 may, based on a point in which measured inductor current I_L reaches peak current I_{PK}, generate a signal indicating the end of the first phase (Phase A). Based on such signals indicating timing of switch cycles and switch phases of boost converter 20A, latch 48 may generate appropriate control signal(s) to switch control block 50, which may in turn generate appropriate control signals to switches 28 and 29 to accordingly selectively activate and deactivate switches 28 and 29.

In addition, current average limit control block 35 may generate a digital signal indicative of a target average current limit, which DAC 40 may convert into an equivalent analog target average current signal I_{AVG_LIM} representative of a maximum average current to flow through power inductor 30. Such target average current signal I_{AVG_LIM} may be set based on a maximum current limit of power inductor 30, which may be among the parameters received by average limit control block 35. Other parameters received by average limit control block 35 may include battery voltage V_{BAT} and/or a parameter programmed to be indicative of maximum current as a function of battery voltage V_{BAT}.

Additional or alternative parameters may include supply voltage V_{SUPPLY}, digital audio input signal DIG_IN, and/or analog signal V_{IN}.

Average limit control block 35 may also generate its own version of peak current I_{PK} (which may be different than that generated by compensator 34) based on target average current signal I_{AVG_LIM} such that inductor current I_L does not exceed the maximum current limit based on a control loop including integrator 52, integrator comparator 54, and latch 56. As shown in FIGURE 3, a multiplexer 37 may select one of the peak current signals generated by compensator 34 and average limit control block 35 based on a control signal communicated from multiplexer select block 39.

Multiplexer select block 39 may be configured such that, if the peak current determined by compensator 34 is less than the peak current determined by average limit control block 35, multiplexer select block 39 may cause multiplexer 37 to select the peak current determined by compensator 34. On the other hand, if the peak current determined by compensator 34 is greater than the peak current determined by average limit control block 35, then multiplexer select block 39 may cause multiplexer 37 to select the peak current determined by average limit control block 35.

In some embodiments, the maximum current limit of power inductor 30 may be determined by analyzing timing information of the output of latch 48 and the output of latch 56. Because the output of compensator 34 may have a slope compensation value added to it, the actual value of the peak current of inductor current I_L may be different than that represented by the output of compensator 34. As such, when the current limiting behavior is applied (e.g., by multiplexer select block 39 causing multiplexer 37 to select the peak current determined by average limit control block 35), the value of compensator 34 at that point in time may be registered by average limit control block 35 and used as a reference to determine if compensator 34 has decreased its value below that of the controlled limited current as represented by target average current signal I_{AVG_LIM}.

Accordingly, average limit control block 35 may operate to maintain the inductor current I_L as measured over multiple switching cycles of boost converter 20A to operate at the average current limit as set by average limit control block 35 on the input to DAC 40. Accordingly, boost converter 20A may increase the value for peak current delivered to the input of DAC 38 until the average of inductor current I_L is larger than the value for peak current delivered to the input of DAC 40. Once this occurs, average limit control block 35

may operate to decrease the value for peak current delivered to the input of DAC 38 until the average of inductor current I_L is smaller than that of the value for peak current delivered to the input of DAC 40. Such operation may over time maintain the average inductor current at the current I_{AVG_LIM} value as represented by the output of DAC 40.

To further illustrate, consider the waveforms for measured current I_L and target average current signal I_{AVG_LIM} shown in FIGURE 4. Because boost converter 20A must operate with volt-second balancing, the average current during the second phase in CCM (Phase B) must be equal to average current during the first phase (Phase A) when in steady state. A simple analysis may show that during the first phase (Phase A), if the average current of power inductor 30 is equal to a desired average current $I_{avg\_desired}$, the mathematical integral of the actual inductor current I_L during the first phase (Phase A) will be equal to the mathematical integral of the desired average current during the first phase. Therefore, if the first phase has a duration of time T1, it is known that:

$$\frac{\int_0^{T1} I_L}{T1} = \frac{\int_0^{T1} I_{avg\_desired}}{T1}$$

Thus:

$$\int_0^{T1} I_L = \int_0^{T1} I_{avg\_desired}$$

and

$$\int_0^{T1} I_L - \int_0^{T1} I_{avg\_desired} = 0$$

Therefore:

$$\int_0^{T1} \left(I_L - I_{avg\_desired}\right) = 0$$

As the equations above show, if a difference between measured inductor current I_L and desired average current $I_{avg\_desired}$ is integrated over the first phase (Phase A), the result of the integration will be zero (0). The equations above show that if the value over the T1 period is integrated, then the value will be zero. Likewise, if the difference is integrated, the T1 value can be found when the result of the integral is zero (0). FIGURE 4 also shows the value of the integration of a difference between measured inductor current I_L and the

desired average current $I_{avg\_desired}$. The order of the subtraction is not critical as the critical detection point is when the integral is equal to zero.

To take advantage of the above analysis, integrator 52 may calculate a mathematical integral of the difference between actual inductor current I_L and target average current signal I_{AVG_LIM}, and integrator comparator 54 may compare the result to zero, such that latch 56 may generate an output indicative of when the integration performed by integrator 52 is zero. As a result of such output, digital compensation and current average limit control block 34 may appropriately modify target average current signal I_{AVG_LIM} and peak current I_{PK} for subsequent switching cycles of boost converter 20A.

Accordingly, to alleviate the concerns with respect to inductor variation and to completely remove the errors associated in determining the average current while controlling the peak current, an integrator circuit may be provided prior to a current averaging comparator to allow for a determination of when the average input current of the boost converter crosses a threshold circuit. Blanking circuitry (not shown) may be provided to allow the current averaging comparator to not indicate that the threshold is crossed at the initiation of the first phase (Phase A), as the integrator may be set to zero at the beginning of the first phase.

FIGURE 6 illustrates a block diagram of selected components of an example IC 9B of a personal audio device, in accordance with embodiments of the present disclosure. In some embodiments, example IC 9B shown in FIGURE 6 may be used to implement IC 9 of FIGURE 1. As shown in FIGURE 6, a microcontroller core 18 may supply a digital input signal DIG_IN to a digital-to-analog converter (DAC) 14, which may convert the digital input signal to an analog signal V_{IN}. DAC 14 may supply analog signal V_{IN} to an amplifier 16 which may amplify or attenuate input signal V_{IN} to provide a differential output signal V_{OUT}, which may operate a speaker, a headphone transducer, a line level signal output, and/or other suitable output. In some embodiments, DAC 14 may be an integral component of amplifier 16. A power supply 10B may provide a plurality of power supplies (e.g., supply voltage V_{SUPPLY_HI} and V_{SUPPLY_LO}) to amplifier 16. In some embodiments, power supply 10B may comprise a switched-mode power converter, as described in greater detail below. Although FIGURE 6 contemplates that IC 9B resides in a personal audio device, systems and methods described herein may also be applied to electrical and electronic systems and devices other than a personal audio device, including

systems for use in a computing device larger than a personal audio device, such as an automobile, a building, or other structure. Further, systems and methods described herein may also be applied to electrical and electronic systems and devices other than audio devices and audio transducers, such as vibro-haptic transducers, piezeoelectric transducers, or other transducers.

As described above and shown in FIGURE 6, power supply 10B may provide a higher supply voltage V_{SUPPLY_HI} and a lower supply voltage V_{SUPPLY_LO}. Accordingly, amplifier 16 may be configured as a Class-G amplifier that may select between higher supply voltage V_{SUPPLY_HI} and lower supply voltage V_{SUPPLY_LO} depending upon a magnitude of output signal V_{OUT}. In these and other embodiments, a system may include a plurality of devices (e.g., amplifiers 16 or other devices) each of which may operate at a specific supply voltage, in which case some of such devices may use higher supply voltage V_{SUPPLY_HI} supplied from power supply 10B and other device may use lower supply voltage V_{SUPPLY_LO} supplied from power supply 10B.

FIGURE 7A illustrates a block diagram of selected components of an example power converter 20B which may be used to implement power supply 10B shown in FIGURE 6, in accordance with embodiments of the present disclosure. In many respects, power converter 20B may be similar in structure and function to boost converter 20A depicted in FIGURE 3 (including, e.g., similar components of control circuit 32, details of which are omitted from FIGURE 7A). As shown in FIGURE 7A, power converter 20B may include a boost converter comprising a power inductor 30 and switches 28 and 29 under the control of control circuit 32 in order to generate a supply voltage V_{SUPPLY_HI} across a boost capacitor 26, wherein supply voltage V_{SUPPLY_HI} is higher than a battery voltage V_{BAT} of battery 22. In some embodiments, battery 22 may comprise a multi-cell battery.

In order to operate with greater power efficiency (e.g., as compared to power converter 20B supplying only supply voltage V_{SUPPLY_HI}), power converter 20B may also supply a supply voltage V_{SUPPLY_LO} lower than supply voltage V_{SUPPLY_HI}. Thus, to reduce power consumption, including idle power consumption of an amplifier 16 or other circuit supplied from power converter 20B, such amplifier 16 or other circuit (or control circuitry for such amplifier or other circuity) may select between supply voltage V_{SUPPLY_LO} and supply voltage V_{SUPPLY_HI} based on actual power supply needs of such amplifier 16 or other

circuit (e.g., a magnitude of an output signal V_{OUT} driven by amplifier 16). Thus, as shown in FIGURE 7A, power converter 20B may provide battery voltage V_{BAT} of battery 22 as lower supply voltage V_{SUPPLY_LO}.

However, for higher values of battery voltage V_{BAT}, as may be the case when battery 22 comprises a multi-cell battery, the use of battery voltage V_{BAT} as lower supply voltage V_{SUPPLY_LO} may provide minimal power savings, particularly for low levels of output signal V_{OUT} driven by amplifier 16.

To overcome such limitation, FIGURE 7B illustrates a block diagram of selected components of another example power converter 20C which may be used to implement power supply 10B shown in FIGURE 6, in accordance with embodiments of the present disclosure. A main difference between power converter 20C of FIGURE 7B as compared to power converter 20B of FIGURE 7A is that instead of battery voltage V_{BAT} of battery 22 being supplied as lower supply voltage V_{SUPPLY_LO}, power converter 20C may provide a voltage supply lower than battery voltage V_{BAT} external to power converter 20C as lower supply voltage V_{SUPPLY_LO}. However, the use of a voltage supply lower than battery voltage V_{BAT} may provide minimal power savings for medium levels of output signal V_{OUT} driven by amplifier 16.

To overcome both the limitations of power converter 20B and power converter 20C, FIGURE 7C illustrates a block diagram of selected components of yet another example power converter 20D which may be used to implement power supply 10B shown in FIGURE 6, in accordance with embodiments of the present disclosure. As shown in FIGURE 7C, power converter 20D may implement a boost converter comprising a power inductor 30 and switches 28 and 29 under the control of control circuit 32 in order to generate a supply voltage V_{SUPPLY_HI} across a boost capacitor 26, wherein supply voltage V_{SUPPLY_HI} is higher than a battery voltage V_{BAT} of battery 22. In addition, power converter 20D may implement a Class-H envelope tracking buck converter comprising a power inductor 70, buck capacitor 76, and switches 78 and 79 under the control of a Class-H buck control circuit 72 in order to generate a supply voltage V_{SUPPLY_LO} across a boost capacitor 26, wherein supply voltage V_{SUPPLY_LO} is lower than a battery voltage V_{BAT} of battery 22 and tracks a signal envelope of output signal V_{OUT}. Advantageously, the topology of power converter 20D may be capable of using the same amount of stored energy of boost capacitor 26 as power converter 20B, but the presence of the Class-H tracking buck converter in

power converter 20D and the ability to provide higher supply voltage V_{SUPPLY_HI} and lower supply voltage V_{SUPPLY_LO} may result in significantly lower idle power consumption and greater power efficiency of power converter 20D compared to that of power converter 20B.

To leverage the advantages of both power converters 20A and 20D, FIGURE 8 illustrates a block diagram of selected components of an example hybrid power converter 20E which may be used to implement power supply 10B shown in FIGURE 6, in accordance with embodiments of the present disclosure. As shown in FIGURE 8, hybrid power converter 20E may implement a boost converter comprising a power inductor 30 and switches 28 and 29 under the control of control circuit 32 in order to generate a supply voltage V_{SUPPLY_HI} across a boost capacitor 26, wherein supply voltage V_{SUPPLY_HI} is higher than a battery voltage V_{BAT} of battery 22. In addition, hybrid power converter 20E may implement a Class-H envelope tracking buck converter comprising a power inductor 70, buck capacitor 76, and switches 78 and 79 under the control of a Class-H buck control circuit 72 in order to generate a supply voltage V_{SUPPLY_LO} across boost capacitor 26, wherein supply voltage V_{SUPPLY_LO} is lower than a battery voltage V_{BAT} of battery 22 and tracks a signal envelope of output signal V_{OUT}. In addition, hybrid power converter 20E may operate in one of at least two modes. In a first mode, switch 62B may be activated (e.g., on, closed, enabled) and switch 62A may be deactivated (e.g., off, open, disabled) such that a bottom plate of boost capacitor 26 corresponding to the negative terminal of supply voltage V_{SUPPLY} is coupled to ground voltage. In a second mode, switch 62A may be activated and switch 62B may be deactivated such that a bottom plate of boost capacitor 26 (e.g., opposite of the top plate of boost capacitor 26 at which supply voltage V_{SUPPLY} is present) is coupled to supply voltage V_{SUPPLY_LO}. Switching between the first mode and the second mode may be controlled by a hybrid mode switch controller 60. Hybrid mode switch controller 60 may be configured to transition from operation in the first mode to operation in the second mode when supply voltage V_{SUPPLY_HI} drops below a predetermined threshold voltage V_{TH}. In addition, hybrid mode switch controller 60 may be configured to transition from operation in the second mode to operation in the first mode when supply voltage V_{SUPPLY_HI} rises above a predetermined threshold voltage V_{TH}. Although not shown in FIGURE 8, in some embodiments, hybrid mode switch controller 60 may operate with hysteresis, such that a threshold voltage V_{TH} for switching from the first mode to the second

mode may be lower than a threshold voltage V_{TH} for switching from the second mode to the first mode.

To further illustrate hybrid operation between the first mode and the second mode, FIGURE 9 illustrates graphs depicting example waveforms for selected voltages of example hybrid power converter 20E when switched between the first mode and the second mode and between the second mode and the first mode, in accordance with embodiments of the present disclosure. As shown in FIGURE 9, at a time t_0, hybrid mode switch control 60 may set the operating mode of hybrid power converter 20E to the first mode, and a Class-G control of an amplifier 16 may select supply voltage V_{SUPPLY_LO} as its supply voltage. As output signal V_{OUT} increases, Class-H buck control circuit 72 may cause supply voltage V_{SUPPLY_LO} to track output signal V_{OUT}. At a time t_1, output signal V_{OUT} may increase to a level at which Class-H buck control circuit 72 can no longer track output signal V_{OUT}, and thus, at such time t_1 a Class-G control of an amplifier 16 may select supply voltage V_{SUPPLY_HI} as its supply voltage and supply voltage V_{SUPPLY_HI} may begin supplying current to such amplifier 16.

At a time t_2, due to further increase in output signal V_{OUT}, a boost current limit for the boost converter of hybrid power converter 20E may be reached, and a voltage ΔV across boost capacitor 26 may begin to decrease. At time t_3, at which voltage ΔV across capacitor 26 drops below a threshold voltage V_{TH}, Class-H buck control circuit 72 may set a target for supply voltage V_{SUPPLY_LO} to the difference between supply voltage V_{SUPPLY_HI} and threshold voltage V_{TH}, and hybrid mode switch control 60 may set the operating mode of hybrid power converter 20E to the second mode, thus coupling the bottom plate of boost capacitor 26 to supply voltage V_{SUPPLY_LO}.

Accordingly, once supply voltage V_{SUPPLY_LO} across buck capacitor 76 discharges to the maximum of supply voltage V_{SUPPLY_HI} (e.g., 20V) minus threshold voltage V_{TH} at time t_4, Class-H buck controller 72 and the buck converter of hybrid power converter 20E may regulate the voltage V_{BOT} at the bottom plate of boost capacitor 26. As the amplifier 16 loading hybrid power converter 20E continues to draw current, Class-H buck controller 72 and the buck converter of hybrid power converter 20E may attempt to regulate supply voltage V_{SUPPLY_HI} to its maximum voltage (e.g., 20V) by increasing voltage V_{BOT}, allowing boost capacitor 26 to discharge and use its stored energy to supply current to the amplifier 16 loading hybrid power converter 20E.

As output signal V_{OUT} decreases, supply voltage V_{SUPPLY_HI} may increase back to its maximum voltage (e.g., 20V) at time t_5, and may be held at such maximum voltage by Class-H buck controller 72 and the buck converter of hybrid power converter 20E decreasing voltage V_{BOT}. At time t_6, when voltage V_{BOT} has decreased to zero, hybrid mode switch control 60 may set the operating mode of hybrid power converter 20E to the first mode, thus coupling the bottom plate of boost capacitor 26 to ground. At such point, Class-H buck controller 72 and the buck converter of hybrid power converter 20E may increase supply voltage V_{SUPPLY_LO} to its maximum voltage (e.g., 9 V), so that it is ready to be selected as the supply voltage for amplifier 16 when output signal V_{OUT} decreases below such maximum voltage of supply voltage V_{SUPPLY_LO}.

As used herein, when two or more elements are referred to as "coupled" to one another, such term indicates that such two or more elements are in electronic communication or mechanical communication, as applicable, whether connected indirectly or directly, with or without intervening elements.

This disclosure encompasses all changes, substitutions, variations, alterations, and modifications to the example embodiments herein that a person having ordinary skill in the art would comprehend. Similarly, where appropriate, the appended claims encompass all changes, substitutions, variations, alterations, and modifications to the example embodiments herein that a person having ordinary skill in the art would comprehend. Moreover, reference in the appended claims to an apparatus or system or a component of an apparatus or system being adapted to, arranged to, capable of, configured to, enabled to, operable to, or operative to perform a particular function encompasses that apparatus, system, or component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative. Accordingly, modifications, additions, or omissions may be made to the systems, apparatuses, and methods described herein without departing from the scope of the disclosure. For example, the components of the systems and apparatuses may be integrated or separated. Moreover, the operations of the systems and apparatuses disclosed herein may be performed by more, fewer, or other components and the methods described may include more, fewer, or other steps. Additionally, steps may be performed in any suitable order. As used in this document, "each" refers to each member of a set or each member of a subset of a set.

Although exemplary embodiments are illustrated in the figures and described below, the principles of the present disclosure may be implemented using any number of techniques, whether currently known or not. The present disclosure should in no way be limited to the exemplary implementations and techniques illustrated in the drawings and described above.

Unless otherwise specifically noted, articles depicted in the drawings are not necessarily drawn to scale.

All examples and conditional language recited herein are intended for pedagogical objects to aid the reader in understanding the disclosure and the concepts contributed by the inventor to furthering the art, and are construed as being without limitation to such specifically recited examples and conditions. Although embodiments of the present disclosure have been described in detail, it should be understood that various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the disclosure.

Although specific advantages have been enumerated above, various embodiments may include some, none, or all of the enumerated advantages. Additionally, other technical advantages may become readily apparent to one of ordinary skill in the art after review of the foregoing figures and description.

To aid the Patent Office and any readers of any patent issued on this application in interpreting the claims appended hereto, applicants wish to note that they do not intend any of the appended claims or claim elements to invoke 35 U.S.C. § 112(f) unless the words "means for" or "step for" are explicitly used in the particular claim.

WHAT IS CLAIMED IS:

1. A system comprising:

a power converter having a maximum allowable input power drawn from a power source;

an energy storage element coupled to an output of the power converter at a top plate of the energy storage element, wherein the energy storage element is configured to store excess energy; and

control circuity configured to:

when an input power of the power converter exceeds the maximum allowable input power, cause excess energy stored in the energy storage element to be consumed by circuitry coupled to the output of the power converter; and

in order to maintain positive voltage headroom for the circuitry coupled to the output of the power converter, selectively couple a bottom plate of the energy storage element to the power source such that excess energy stored by the circuitry coupled to the output of the power converter is consumed from the energy storage device when the input power of the power converter exceeds the maximum allowable input power.

2. The system of Claim 1, wherein the maximum allowable input power is defined by an input current limit of the power converter.

3. The system of Claim 1, wherein the power source is a battery.

4. The system of Claim 1, wherein the control circuitry is configured to selectively enable and disable coupling of the bottom plate of the energy storage element to the power source at a first switching frequency significantly less than a second switching frequency at which switches of the power converter are switched.

5. The system of Claim 1, wherein the control circuitry is configured to selectively enable and disable coupling of the bottom plate of the energy storage element to the power source at a first switching frequency related to a second switching frequency of a signal driven to a load of an amplifier powered from the power converter.

6. A system comprising:

a power converter configured to generate a first supply voltage at a first supply output; and

a second supply output configured to generate a second supply voltage lower than the first supply voltage, wherein the second supply voltage tracks an envelope of an output signal generated by an amplifier coupled to the power supply.

7. The system of Claim 6, wherein the amplifier is configured to select between the first supply voltage and the second supply voltage as a supply voltage to the amplifier.

8. A system comprising:

a power supply comprising:

a power converter configured to generate a first supply voltage at a first supply output of the power supply; and

a second supply output configured to generate a second supply voltage lower than the first supply voltage; and

an amplifier coupled to the power supply and configured to select between the first supply voltage and the second supply voltage as a supply voltage to the amplifier.

9. The system of Claim 8, wherein the second supply voltage tracks an envelope of an output signal generated by the amplifier.

10. The method of Claim 8, wherein the second supply voltage is provided by a fixed voltage supply external to a switched mode power converter.

11. The method of Claim 8, wherein the second supply voltage is provided by a power source coupled to an input of a power supply.

12. The method of Claim 11, wherein the power source is a battery.

13. A system comprising:

a power converter configured to generate a first supply voltage at a first supply output of the power supply, the power converter having a maximum allowable input power drawn from a power source;

an energy storage element coupled to an output of the power converter at a top plate of the energy storage element, wherein the energy storage element is configured to store excess energy; and

a second supply output configured to generate a second supply voltage lower than the first supply voltage, wherein:

the second supply voltage tracks an envelope of an output signal generated by an amplifier coupled to the power supply when the amplifier consumes power from the second supply output; and

the second supply voltage regulates a voltage at a bottom plate of the energy storage element when the amplifier consumes power from the first supply output.

14. A method comprising, in a system having a power converter having a maximum allowable input power drawn from a power source and an energy storage element coupled to an output of the power converter at a top plate of the energy storage element, wherein the energy storage element is configured to store excess energy:

when an input power of the power converter exceeds the maximum allowable input power, causing excess energy stored in the energy storage element to be consumed by circuitry coupled to the output of the power converter; and

in order to maintain positive voltage headroom for the circuitry coupled to the output of the power converter, selectively coupling a bottom plate of the energy storage element to the power source such that excess energy stored by the circuitry coupled to the output of the power converter is consumed from the energy storage device when the input power of the power converter exceeds the maximum allowable input power.

15. The method of Claim 14, wherein the maximum allowable input power is defined by an input current limit of the power converter.

16. The method of Claim 14, wherein the power source is a battery.

17. The method of Claim 14, wherein the control circuitry is configured to selectively enable and disable coupling of the bottom plate of the energy storage element to the power source at a first switching frequency significantly less than a second switching frequency at which switches of the power converter are switched.

18. The method of Claim 14, wherein the control circuitry is configured to selectively enable and disable coupling of the bottom plate of the energy storage element to the power source at a first switching frequency related to a second switching frequency of a signal driven to a load of an amplifier powered from the power converter.

19. A method comprising:

generating a first supply voltage at a first supply output with a power converter; and

generating a second supply voltage lower than the first supply voltage with a second supply output, wherein the second supply voltage tracks an envelope of an output signal generated by an amplifier coupled to the power supply.

20. The method of Claim 19, further comprising selecting, by the amplifier, between the first supply voltage and the second supply voltage as a supply voltage to the amplifier.

21. A method comprising:

generating a first supply voltage of a power supply at a first supply output with a power converter;

generating a second supply voltage of the power supply lower than the first supply voltage with a second supply output; and

selecting, by an amplifier coupled to the power supply, between the first supply voltage and the second supply voltage as a supply voltage to the amplifier.

22. The method of Claim 21, further comprising tracking, by the second supply voltage, an envelope of an output signal generated by the amplifier.

23. The method of Claim 21, comprising supplying the second supply voltage from a fixed voltage supply external to the switched mode power converter.

24. The method of Claim 21, comprising supplying the second supply voltage from a power source coupled to an input of a power supply.

25. The method of Claim 24, wherein the power source is a battery.

26. A method in a system having a power converter configured to generate a first supply voltage at a first supply output of a power supply, the power converter having a maximum allowable input power drawn from a power source, an energy storage element coupled to an output of the power converter at a top plate of the energy storage element, wherein the energy storage element is configured to store excess energy, and a second supply output configured to generate a second supply voltage lower than the first supply voltage, the method comprising:

tracking, with the second supply voltage, an envelope of an output signal generated by an amplifier coupled to the power supply when the amplifier consumes power from the second supply output; and

regulating, with the second supply voltage, a voltage at a bottom plate of the energy storage element when the amplifier consumes power from the first supply output.

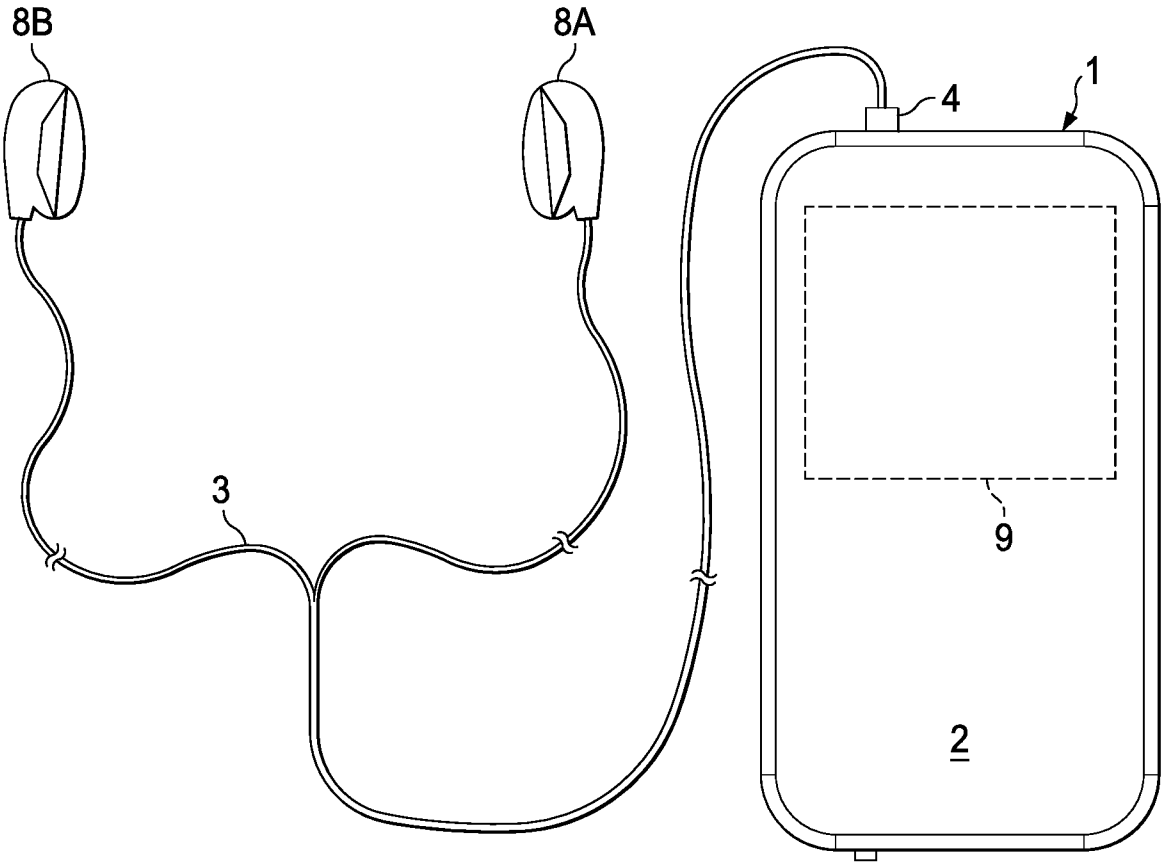
8B
8A
1
4
3
9
2

FIG. 1

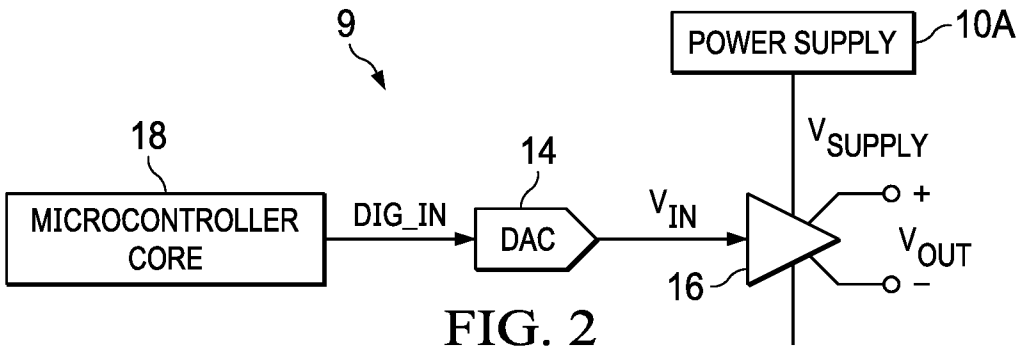
9
POWER SUPPLY
10A
18
14
V SUPPLY
MICROCONTROLLER CORE
DIG_IN
DAC
V IN
+
V OUT
16
–

FIG. 2

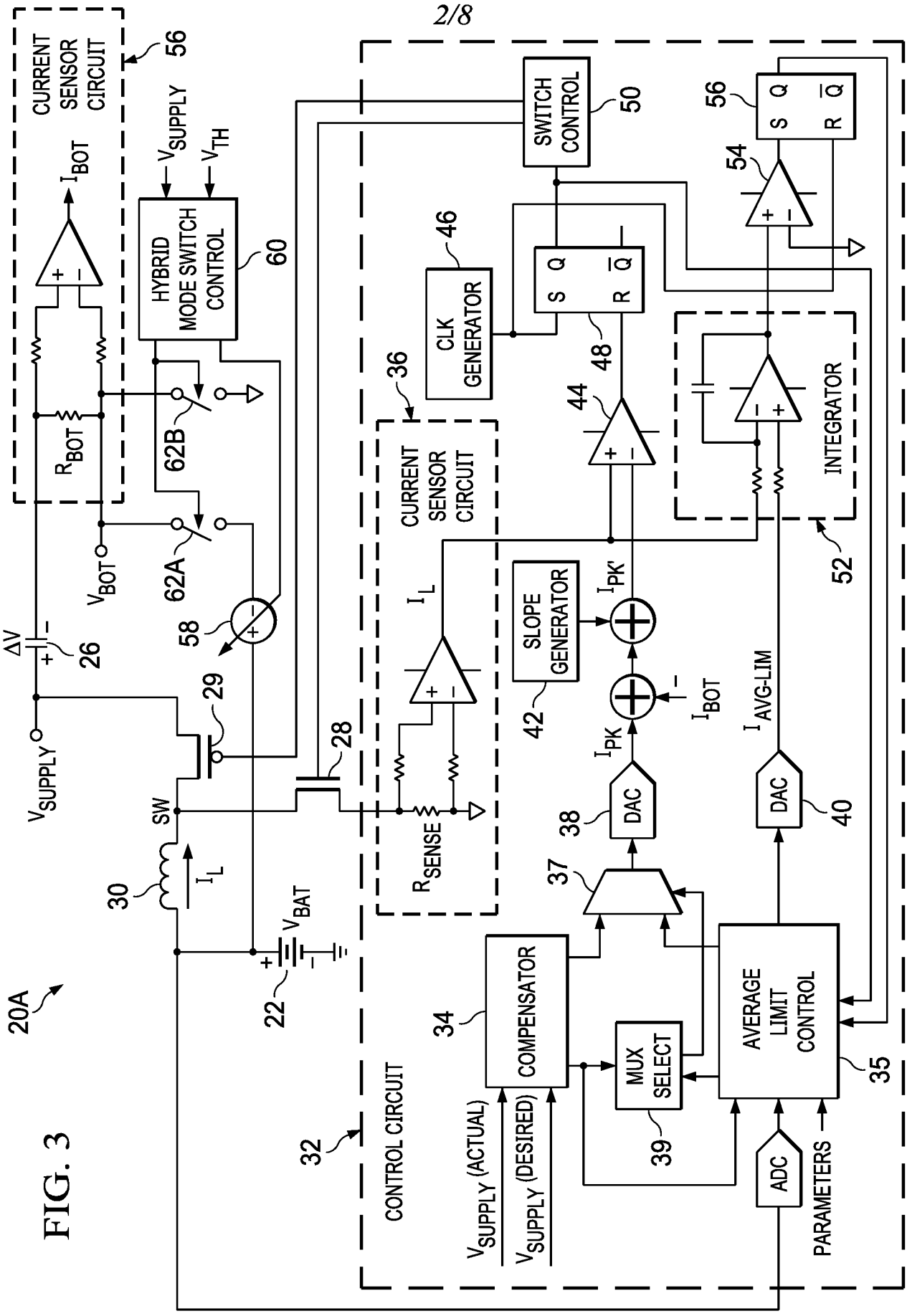
20A
CONTROL CIRCUIT
32
CURRENT SENSOR CIRCUIT
56
I_{BOT}
V_{SUPPLY}
V_{TH}
HYBRID MODE SWITCH CONTROL
60
R_{BOT}
62B
62A
V_{BOT}
58
ΔV
26
29
V_{SUPPLY}
SW
30
I_L
V_{BAT}
22
28
CURRENT SENSOR CIRCUIT
36
I_L
R_{SENSE}
SWITCH CONTROL
50
CLK GENERATOR
46
S Q
R $\bar{Q}$
48
44
SLOPE GENERATOR
42
$I_{PK'}$
I_{PK}
I_{BOT}
DAC
38
37
34
COMPENSATOR
MUX SELECT
39
V_{SUPPLY} (ACTUAL)
V_{SUPPLY} (DESIRED)
54
56
S Q
R $\bar{Q}$
INTEGRATOR
52
$I_{AVG-LIM}$
DAC
40
AVERAGE LIMIT CONTROL
35
ADC
PARAMETERS

FIG. 3

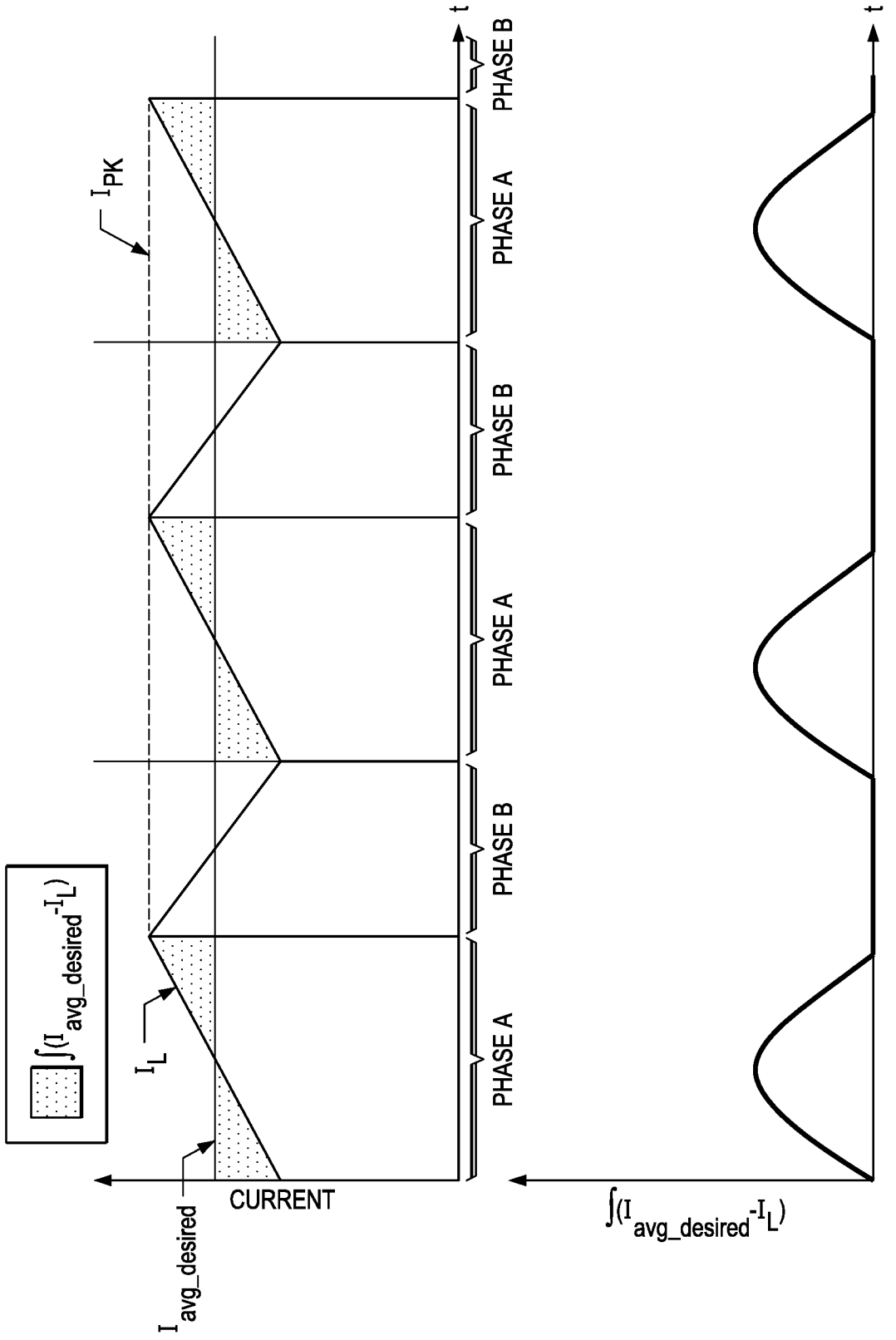
t
PHASE A
PHASE B
PHASE A
PHASE B
PHASE A
PHASE B
I_{PK}
I_L
$\int(I_{avg\_desired}-I_L)$
$I_{avg\_desired}$
CURRENT
t
$\int(I_{avg\_desired}-I_L)$

FIG. 4

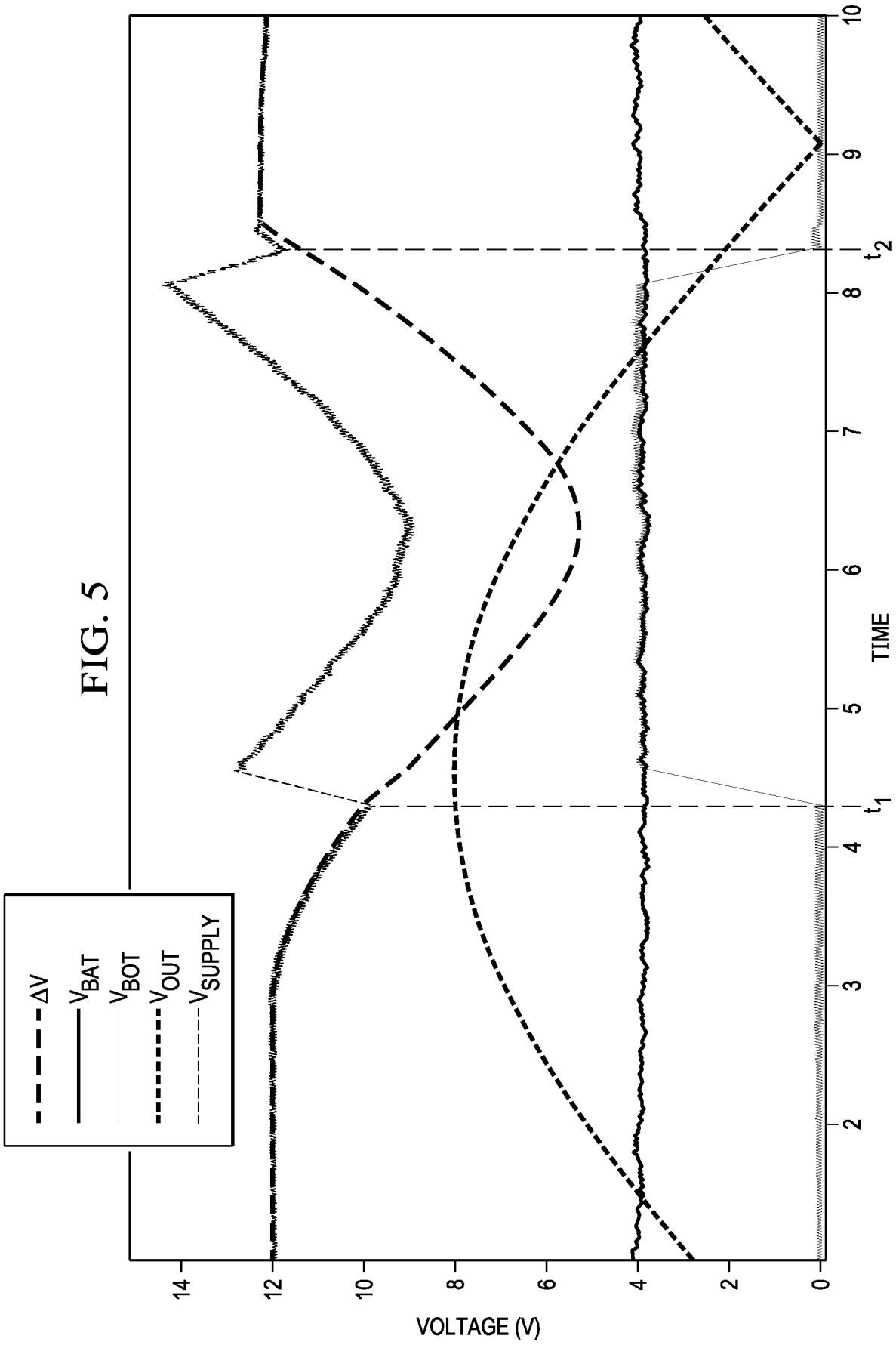
ΔV
V_{BAT}
V_{BOT}
V_{OUT}
V_{SUPPLY}
VOLTAGE (V)
0
2
4
6
8
10
12
14
TIME
2
3
4
5
6
7
8
9
10
t_1
t_2

FIG. 5

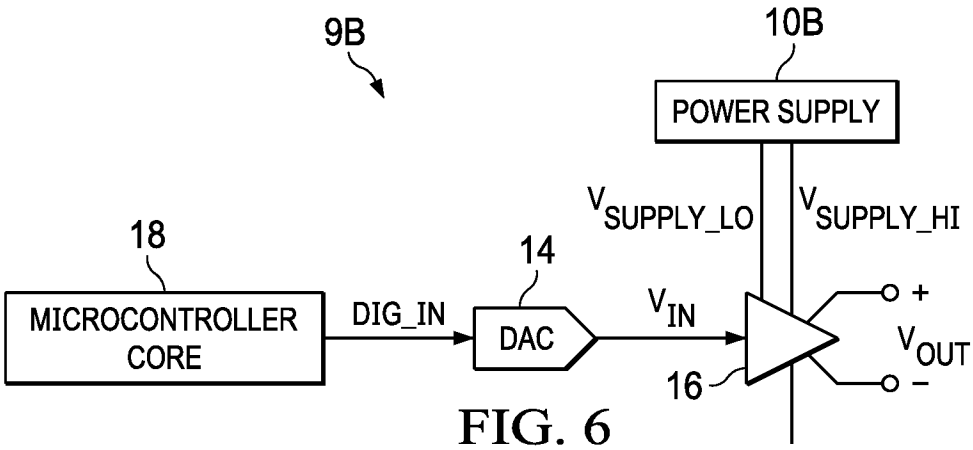
9B
10B
POWER SUPPLY
V_{SUPPLY_LO}
V_{SUPPLY_HI}
18
14
MICROCONTROLLER CORE
DIG_IN
DAC
V_{IN}
+
V_{OUT}
−
16

FIG. 6

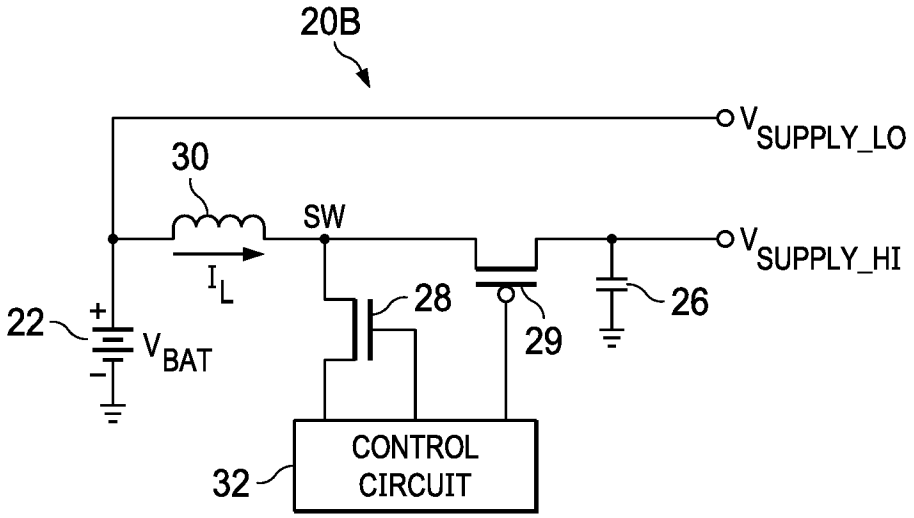
20B
V_{SUPPLY_LO}
30
SW
V_{SUPPLY_HI}
I_L
22
+
V_{BAT}
−
28
29
26
CONTROL CIRCUIT
32

FIG. 7A

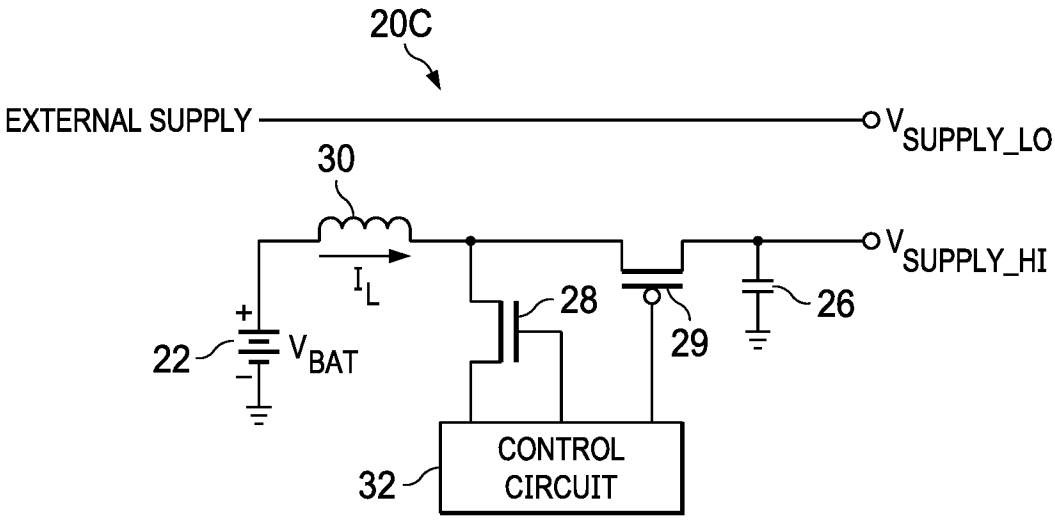
20C
EXTERNAL SUPPLY
V_{SUPPLY_LO}
30
V_{SUPPLY_HI}
I_L
28
26
29
22
V_{BAT}
CONTROL CIRCUIT
32

FIG. 7B

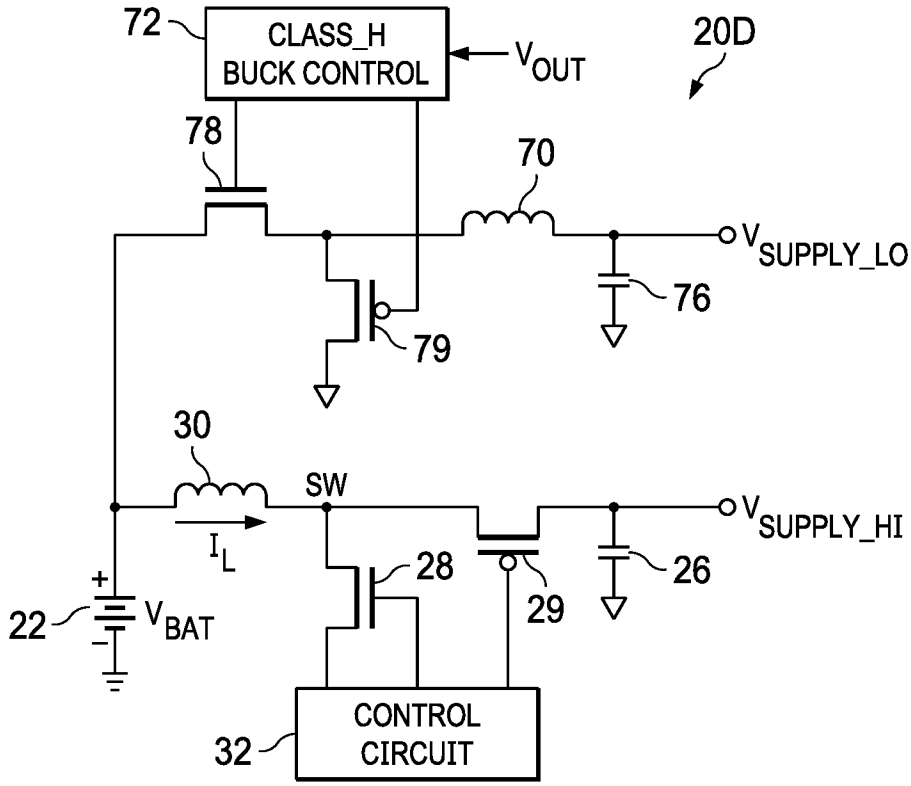
72
CLASS_H BUCK CONTROL
V_{OUT}
20D
78
70
V_{SUPPLY_LO}
76
79
30
SW
V_{SUPPLY_HI}
I_L
28
26
29
22
V_{BAT}
CONTROL CIRCUIT
32

FIG. 7C

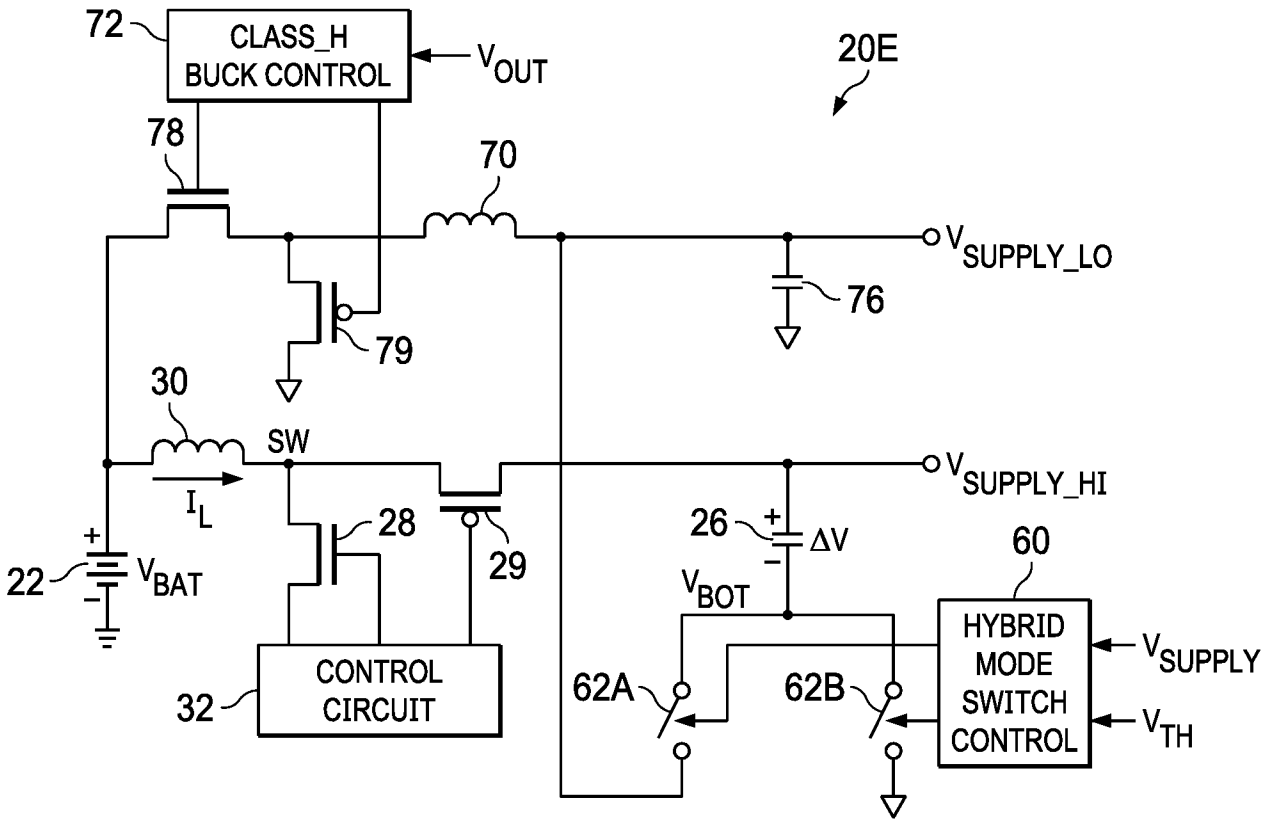
72
CLASS_H
BUCK CONTROL
V_{OUT}
20E
78
70
V_{SUPPLY_LO}
76
79
30
SW
V_{SUPPLY_HI}
I_L
28
29
26
+
ΔV
−
60
22
+
V_{BAT}
−
V_{BOT}
HYBRID
MODE
SWITCH
CONTROL
V_{SUPPLY}
V_{TH}
62A
62B
CONTROL
CIRCUIT
32

FIG. 8

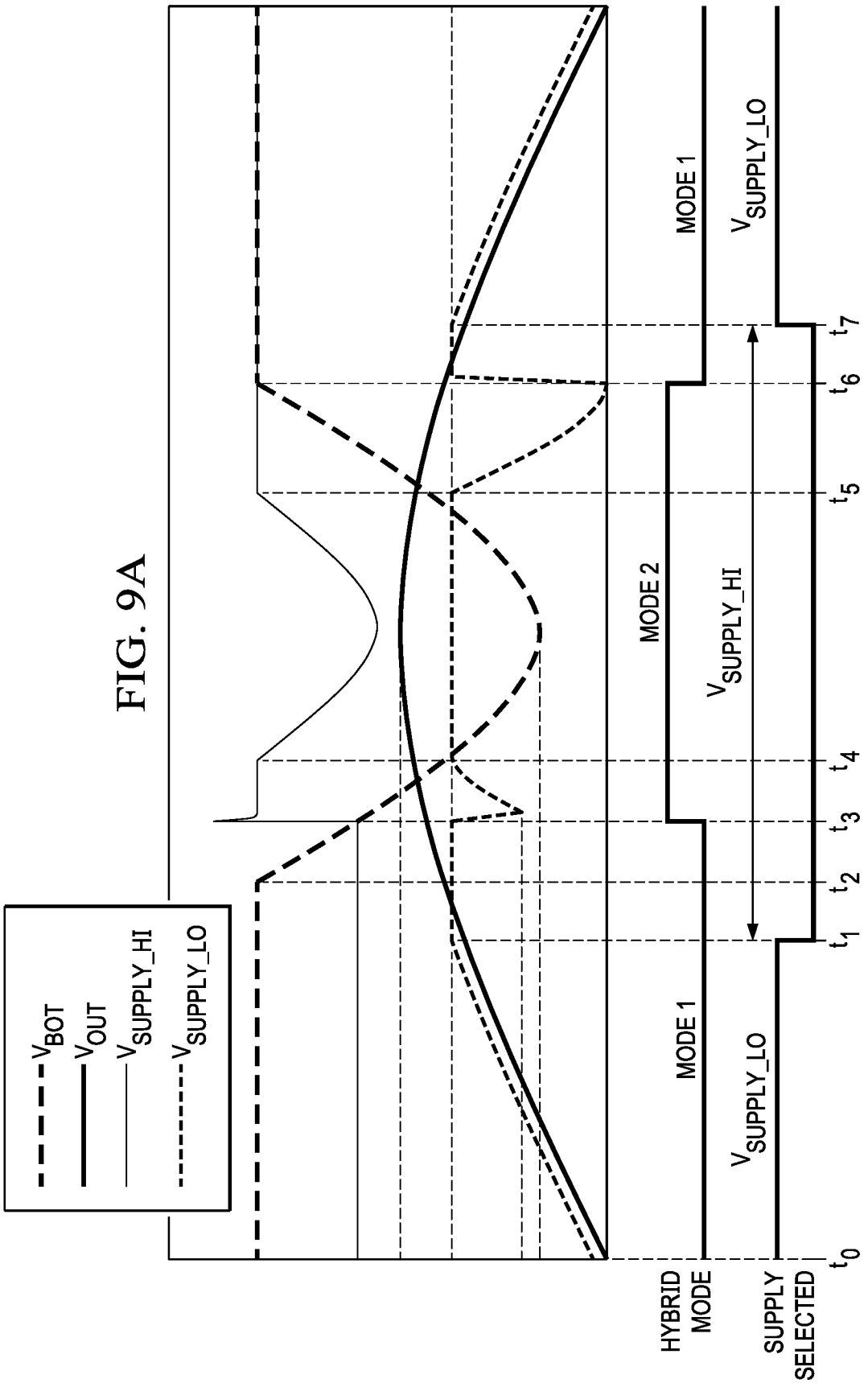
V_{BOT}
V_{OUT}
V_{SUPPLY_HI}
V_{SUPPLY_LO}
HYBRID MODE
SUPPLY SELECTED
MODE 1
MODE 2
MODE 1
V_{SUPPLY_LO}
V_{SUPPLY_HI}
V_{SUPPLY_LO}
t_0
t_1
t_2
t_3
t_4
t_5
t_6
t_7

FIG. 9A

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2020/047237

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M1/32 H02M3/156 H02M3/158 H02M1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	STALA ROBERT ET AL: "A Switched-Capacitor DC-DC Converter With Variable Number of Voltage Gains and Fault-Tolerant Operation", IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 66, no. 5, 1 May 2019 (2019-05-01), pages 3435-3445, XP011695271, ISSN: 0278-0046, DOI: 10.1109/TIE.2018.2851962 [retrieved on 2018-12-31]	1-5, 14-18
Y	figures 1-2	13,26
A	page 3436 - page 3437 page 3440	6-12, 19-25
	----- -/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 October 2020	30/10/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Riehl, Philippe

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2020/047237

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 2014/197814 A1 (SHI SONG S [US] ET AL) 17 July 2014 (2014-07-17) figure 11 paragraph [0070] - paragraph [0072] ----	6-12, 19-25 13,26 1-5, 14-18
A	GB 2 555 902 A (CIRRUS LOGIC INT SEMICONDUCTOR LTD [GB]) 16 May 2018 (2018-05-16) figure 2 figure 4 page 6, line 19 - page 7, line 3 page 8, line 10 - line 19; figure 19 ----	1-26

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2020/047237

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014197814 A1	17-07-2014	CN 104904116 A	09-09-2015
		EP 2944023 A1	18-11-2015
		JP 6046270 B2	14-12-2016
		JP 2016506231 A	25-02-2016
		KR 20150104598 A	15-09-2015
		US 2014197814 A1	17-07-2014
		WO 2014110457 A1	17-07-2014
GB 2555902 A	16-05-2018	NONE	