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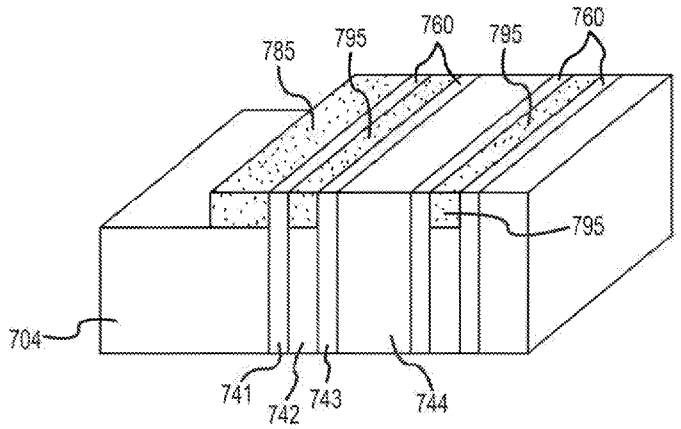

FIG7C

(57) Abstract: A structure usable in a molecular sensor device comprises a substrate defining a substrate plane and spaced apart pairs of reducible metal oxide or metal nitride sheets attached to the substrate at an angle to the substrate plane. The structure further includes intervening dielectric sheets. Fabrication methods for manufacturing structures for molecular sensors are disclosed comprising oblique angle deposition of reducible metal oxide or metal nitride and dielectric layers, planarization of the resulting stack, and reduction of portions of the reducible metal oxide or metal nitride sheets to the corresponding base metal.

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TITLE: METHODS OF FABRICATING NANOSCALE STRUCTURES USABLE IN MOLECULAR SENSORS AND OTHER DEVICES

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to and the benefit of U.S. Provisional Patent Application Serial No. 62/896,896 filed September 6, 2019 and entitled "Methods of Fabricating Nanoscale Structures Usable in Molecular Sensors and Other Devices," the disclosure of which is incorporated herein by reference in its entirety for all purposes.

FIELD

The present disclosure generally relates to nanofabrication and nanoelectronics, and more particularly relates to device structures and the fabrication of structures usable in molecular sensors for sensing and analyzing molecules.

BACKGROUND

Molecular analysis has received an increasing amount of attention in various fields such as precision medicine or nanotechnology. One example includes the analysis of molecules for sequencing genomes. The seminal work of Avery in 1946 demonstrated that DNA was the material that determined traits of an organism. The molecular structure of DNA was then first described by Watson and Crick in 1953, for which they received the 1962 Nobel Prize in Medicine. This work made it clear that the sequence of chemical letters (bases) of the DNA molecules encode the fundamental biological information. Since this discovery, there has been a concerted effort to develop means to actually experimentally measure this sequence. The first method for systematically sequencing DNA was introduced by Sanger in 1978, for which he received the 1980 Nobel Prize in Chemistry.

A basic method for sequencing a genome was automated in a commercial instrument platform in the late 1980's, which ultimately enabled the sequencing of the first human genome in 2001. This was the result of a massive public and private effort taking over a decade, at a cost of billions of dollars, and relying on the output of thousands of dedicated DNA sequencing instruments. The success of this effort motivated the development of a number of "massively parallel" sequencing platforms with the goal of dramatically reducing the cost and time required to sequence a human genome. Such massively parallel sequencing platforms generally rely on processing millions to billions of sequencing reactions at the same time in highly miniaturized microfluidic formats. The first of these was invented and commercialized by Rothberg in 2005 as the 454 platform, which achieved thousand fold reductions in cost and instrument time. However, the 454 platform still required approximately a million dollars and took over a month to sequence a genome.

Further improvements in quality and accuracy of sequencing, as well as reductions in cost and time are still needed. This is especially true to make genome sequencing practical for widespread use in precision medicine, where it is desirable to sequence the genomes of millions of individuals with a clinical grade of quality.

While many DNA sequencing techniques utilize optical means with fluorescence reporters, such methods can be cumbersome, slow in detection speed, and difficult to mass produce to further reduce costs. Label-free DNA or genome sequencing approaches provide advantages of not having to use fluorescent type labeling processes and associated optical systems, especially when combined with electronic signal detection that can be achieved rapidly and in an inexpensive way.

In this regard, certain types of molecular electronic devices can detect single molecule, biomolecular analytes such as DNAs, RNAs, proteins, and nucleotides by measuring electronic signal changes when the analyte molecule is attached to a circuit. Such

methods are label-free and thus avoid using complicated, bulky and expensive fluorescent type labeling apparatus

While current molecular electronic devices can electronically measure molecules for various applications, they lack the scalability and manufacturability needed for rapidly sensing many analytes at a scale of up to millions in a practical manner. Such highly scalable methods are particularly important for DNA sequencing applications, which often need to analyze millions to billions of independent DNA molecules. In addition, the manufacture of current molecular electronic devices is generally costly due to the high level of precision needed.

Thus, new and improved structures e.g., device stacks, and methods of fabricating new structures are needed to lower cost and improve performance of molecular sensors comprising structure assemblies.

SUMMARY

In various embodiments of the present disclosure, new structures such as device stacks, and methods of fabrication of structures usable in molecular sensors are described.

In various aspects of the present disclosure, a method of manufacturing a structure usable in a molecular sensor device is disclosed. The method comprises: providing a substrate defining a substrate plane with a protrusion protruding from the substrate at an angle to the substrate plane; depositing a first reducible metal oxide or metal nitride layer in an orientation along a side of the protrusion to form a first reducible metal oxide or metal nitride sheet at the angle to the substrate plane; depositing an inner dielectric layer on the first reducible metal oxide or metal nitride layer to form an inner dielectric sheet at the angle to the substrate plane; depositing a second reducible metal oxide or metal nitride layer on the inner dielectric layer to form a second reducible metal oxide or metal nitride sheet at the angle to the

substrate plane, wherein the first reducible metal oxide or metal nitride sheet and the second reducible metal oxide or metal nitride sheet form a pair of sheets spaced apart by the inner dielectric sheet between the first reducible metal oxide or metal nitride sheet and the second reducible metal oxide or metal nitride sheet; depositing an outer dielectric layer on the second reducible metal oxide or metal nitride layer to form an outer dielectric sheet at an angle to the substrate plane; repeating the depositing of the first reducible metal oxide or metal nitride layer, the inner dielectric layer, the second reducible metal oxide or metal nitride layer, and the outer dielectric layer at least once to form spaced apart pairs of reducible metal oxide or metal nitride sheets with an inner dielectric sheet between each reducible metal oxide or metal nitride sheet in the pair of reducible metal oxide or metal nitride sheets and an outer dielectric sheet between each pair of reducible metal oxide or metal nitride sheets; planarizing the pairs of reducible metal oxide or metal nitride sheets, the inner dielectric sheets, and the outer dielectric sheets to form exposed end portions of each; and reducing the exposed end portions of the reducible metal oxide or metal nitride sheets to the corresponding metal to form parallel metal electrode strips.

In various aspects, each inner dielectric layer is deposited with a first thickness, each outer dielectric sheet is deposited with a second thickness, and the second thickness is at least one order of magnitude greater than the first thickness.

In certain aspects the method may further comprise attaching a mechanically supportive block material adjacent a stack formed by the deposited first reducible metal oxide or metal nitride layers, inner dielectric layers, second reducible metal oxide or metal nitride layers, and outer dielectric layers, prior to the step of planarizing.

In various embodiments, the inner dielectric sheets and the outer dielectric sheets may comprise different dielectric materials. Reducing the exposed end portions of the reducible metal oxide or metal nitride sheets to the corresponding metal may comprise exposure to H_2.

In certain aspects, the method may further comprise (i) placing at least one portion of a dielectric mask layer across the metal electrode strips to leave short segments of electrode strips exposed in a gap; and (ii) depositing metal islands on the short segments of electrode strips. The gap may measure from about 2 nm to about 40 nm.

In various aspects of the method, a plurality of lead conductors may be connected to metal electrode strips with each lead conductor connected to a respective electrode strip, wherein each lead conductor diverges in width as the lead conductor extends away from an edge of the electrode strip. The method may further comprise depositing a gate electrode parallel to the substrate plane and perpendicular to a reducible metal oxide or metal nitride plane defined by a reducible metal oxide or metal nitride sheet in the spaced apart pairs of reducible metal oxide or metal nitride sheets.

In various embodiments of the present disclosure, a method of manufacturing a structure usable in a molecular sensor device is disclosed. The method comprises: providing a substrate defining a substrate plane with a protrusion protruding from the substrate at an angle to the substrate plane; depositing a first reducible metal oxide or metal nitride layer in an orientation along a side of the protrusion to form a first reducible metal oxide or metal nitride sheet at the angle to the substrate plane; depositing an inner dielectric layer on the first reducible metal oxide or metal nitride layer to form an inner dielectric sheet at the angle to the substrate plane; depositing a second reducible metal oxide or metal nitride layer on the inner dielectric layer to form a second reducible metal oxide or metal nitride sheet at the angle to the substrate plane, wherein the first reducible metal oxide or metal nitride sheet and the second reducible metal oxide or metal nitride sheet form a pair of sheets spaced apart by the inner dielectric sheet between the first reducible metal oxide or metal nitride sheet and the second reducible metal oxide or metal nitride sheet; depositing an outer dielectric layer on the second reducible metal oxide or metal nitride layer to form an outer dielectric sheet at an

angle to the substrate plane; repeating the depositing of the first reducible metal oxide or metal nitride layer, the inner dielectric layer, the second reducible metal oxide or metal nitride layer, and the outer dielectric layer at least once to form spaced apart pairs of reducible metal oxide or metal nitride sheets with an inner dielectric sheet between each reducible metal oxide or metal nitride sheet in the pair of reducible metal oxide or metal nitride sheets and an outer dielectric sheet between each pair of reducible metal oxide or metal nitride sheets; planarizing the pairs of reducible metal oxide or metal nitride sheets, the inner dielectric sheets, and the outer dielectric sheets to form exposed end portions of each; selectively etching an exposed end portion of each inner dielectric sheet to form grooves in each inner dielectric sheet descending from the planarized edge toward the substrate; filling the grooves with PMMA-type resist material; depositing a metal layer on the planarized surface of the structure; and removing the PMMA-type resist material along with deposited metal residing thereon leaving an arrangement of pairs of spaced apart parallel metal electrode strips with the metal electrode strips in a pair of strips separated by a groove.

In various aspects, the method may further comprise attaching a mechanically supportive block material adjacent a stack formed by the deposited first reducible metal oxide or metal nitride layers, inner dielectric layers, second reducible metal oxide or metal nitride layers, and outer dielectric layers, prior to the step of planarizing. In other aspects, the inner dielectric sheets and the outer dielectric sheets may comprise different dielectric materials.

In certain embodiments, the inner dielectric layer has a first thickness, the outer dielectric layer has a second thickness, and the second thickness is at least one order of magnitude greater than the first thickness.

In various aspects, the method may further comprise: (i) placing at least one portion of a dielectric mask layer across the metal electrode strips to leave short segments of

electrode strips exposed in a gap; and (ii) depositing metal islands on the short segments of electrode strips. The gap may measure from about 2 nm to about 40 nm.

In various embodiments, a structure usable in a molecular sensor device is disclosed. The structure comprises: a substrate defining a substrate plane; spaced apart pairs of reducible metal oxide or metal nitride layer sheets attached on an edge of the reducible metal oxide or metal nitride layer sheet to the substrate at an angle to the substrate plane; an inner dielectric sheet disposed between the reducible metal oxide or metal nitride layer sheets in each pair of reducible metal oxide or metal nitride layer sheets; and an outer dielectric sheet disposed between spaced apart pairs of reducible metal oxide or metal nitride layer sheets, wherein an edge of each reducible metal oxide or metal nitride layer sheet, inner dielectric sheet and outer dielectric sheet opposite the substrate are coplanar.

In certain aspects, each inner dielectric sheet has a first thickness, each outer dielectric sheet has a second thickness, and the second thickness is at least one order of magnitude greater than the first thickness. In various aspects, the inner dielectric sheets and the outer dielectric sheets comprise different dielectric materials.

In various examples, the structure may further comprise a groove located on an exposed end portion of each inner dielectric sheet opposite the substrate.

In certain aspects, the structure may comprise metal on the edge of each reducible metal oxide or metal nitride layer sheet that are coplanar to the edges of inner dielectric sheet and outer dielectric sheet opposite the substrate.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. A more complete understanding of the

present disclosure, however, may best be obtained by referring to the detailed description and claims when considered in connection with the drawing figures:

FIG. 1 is a flowchart depicting an embodiment of a fabrication process in accordance to the present disclosure;

FIG. 2 illustrates a structure obtainable by fabrication processes of the present disclosure;

FIG. 3 illustrates an embodiment of a structure obtainable by planarizing the structure of FIG. 2;

FIG. 4 is a flowchart depicting an embodiment of a fabrication process in accordance to the present disclosure;

FIGS. 5A-5D illustrate embodiments of structures obtainable by fabrication processes of the present disclosure;

FIG. 6 is a flowchart depicting an embodiment of a fabrication process in accordance to the present disclosure; and

FIGS. 7A-7F illustrate embodiments of structures obtainable by fabrication processes of the present disclosure.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth to provide a full understanding of the present disclosure. It will be apparent, however, to one of ordinary skill in the art that the various embodiments disclosed may be practiced without some of these specific details. In other instances, well-known structures and techniques have not been shown in detail to avoid unnecessarily obscuring the various embodiments.

As described in more detail herein, various embodiments of the present disclosure generally comprise structures usable in molecular sensors and other devices, and methods of

fabricating structures. In various examples, a structure comprises spaced apart electrode pairs, wherein the electrodes in each pair of electrodes are separated by an inner dielectric layer. Further, each pair of electrodes in a structure may be spaced apart by outer dielectric layers.

In certain variations, electrodes are first deposited as reducible metal oxide or metal nitride layers and the layers planarized to expose end portions of the metal oxide or metal nitride layers which can subsequently reduce to the corresponding metal.

Definitions and considerations

As used herein, the term "structure" refers generally to physical constructs comprising at least one of a substrate layer, electrode layer, metal oxide layer, metal nitride layer, or dielectric layer, in any combination, such as structures formed by depositing metal, metal oxide, metal nitride and/or dielectric layers onto a substrate. A "structure" herein may be a part of a molecular sensor or part of a molecular electronics component or any other device. In some instances, a "structure" herein can be converted into a working molecular sensor by disposing a biomolecule or other molecule across a pair of electrodes or a pair of gold (Au) islands in a structure, amongst other processes. In some instances, a structure, e.g., comprising alternating electrode and dielectric layers on a substrate, may also be referred to as a structure usable in, or usable for, a molecular sensor.

As used herein, the term "device stack" generally refers to a structure having multiple layers of material, such as layers comprising metal, metal oxide or metal nitride, and dielectric layers, repeating in a pattern. In various examples, a device stack comprises a three-layer (or "tri-layer") arrangement comprising a dielectric layer disposed between two layers of metal, metal oxide, or metal nitride. In various embodiments, a device stack may comprise at least two spaced apart pairs of metal, metal oxide, or metal nitride layers separated by dielectric material, wherein the metal, metal oxide, or metal nitride layers of each pair are also separated by dielectric material.

As used herein, oblique angle deposition, or "OAD," refers to the process of depositing material, such as a metal, metal oxide, metal nitride, or dielectric, at an incident angle less than 90° relative to a planar substrate receiving the deposition. Normal deposition generally refers to deposition of materials orthogonal (90°) to a substrate, which necessarily creates layers that are co-planar with a top surface of the substrate. OAD, on the other hand, comprises deposition of materials onto a substrate at an angle less than 90°, (including at 0° or "horizontally"), such that vertical or other angled surfaces protruding from a substrate plane can also receive deposition of materials. The definition of OAD is extended herein to include 0° (also referred to as "horizontal" or "sideways") deposition, which can result in no material being deposited onto the top plane of a substrate sheet, but rather only deposition on the edge of the substrate facing the deposition stream and on the surfaces of any protrusions projecting from the substrate that include a surface facing the deposition stream. Herein, "low angle deposition" generally refers to OAD at an incident angle of from about 0° to about 20° relative to a major surface of a substrate, whereas "high angle deposition" generally refers to OAD at an incident angle of from about 20° to about 70° relative to a major surface of a substrate.

With reference now to the drawing figures, FIG. 1 is a flowchart illustrating an embodiment of a fabrication method in accordance to the present disclosure. FIGS. 2 and 3 illustrate embodiments of structures that result from various aspects of the method of FIG. 1. For ease of understanding, the structures depicted in FIGS. 2 and 3 may be referred to in conjunction with the steps of the method in FIG. 1. Further, and as discussed in more detail herein, the method of FIG. 1 may continue to either the method of FIG. 4 or the method of FIG. 6 as indicated by the branched arrow at the bottom of the flowchart of FIG. 1.

In FIG. 1, an embodiment of a fabrication method begins with step 102, providing a substrate defining a substrate plane. A substrate herein is typically dimensioned such that the

length L and width W are much larger (e.g., an order of magnitude larger) than the height H or thickness. A substrate provided in step 102 may comprise a square silicon (Si) wafer measuring about 10 mm L x 10 mm W x 0.5 mm H, or a similarly sized disc-shaped Si wafer. A substrate may further comprise an oxide deposit on one side, such as a SiO_2 deposit measuring about 100 nm to about 300 nm in thickness.

Substrates, such as wafers, can be described as having a top surface and a bottom surface, wherein these two surfaces are considered "major surfaces" because of their larger 2-dimensional size (L x W) relative to the thickness (H) of the substrate. The edges of a substrate are relatively small in comparison, and are thus considered minor surfaces. Although "top" and "bottom" are relative terms depending on orientation of an object with respect to an observer, a substrate wafer laying flat on a table parallel to the ground has a bottom surface in contact with the table, and a top surface that is visible to an observer looking down onto the substrate from above. Further, if the substrate wafer further comprises a SiO_2 or other deposit layer, then the layer is on the "top" surface. The top surface, a major surface, has a generally planar surface which defines a "substrate plane." The substrate plane can be defined by being parallel with a major surface of the substrate, such as a top or bottom surface used for supporting dielectric and/or electrode layers.

Fabrication on the top surface of a substrate may be at various angles to the substrate plane (such as 90° or vertical to the substrate plane) or may be parallel to the substrate plane (i.e., flat on the top surface, such as the case for a SiO_2 or other deposit layer on the top surface). With reference to FIG. 2, a fabricated structure may comprise a base substrate 202 on which various material layers are deposited. The substrate 202 defines a substrate plane 203. Similarly, in FIG. 3, a substrate 302 defines a substrate plane 303. In these examples, the substrates are generally square or rectangular wafers such that in cross-section they appear as rectangular cuboids.

With continued reference to FIG. 1, and in particular, step 104, a protrusion (e.g., a protrusion 204 in FIG. 2) is attached to the substrate to form a step-shape for the combined substrate and protrusion. In alternative embodiments, the protrusion is formed by removing (e.g., ablating) one or more portions of a larger block of substrate material, generating a cut-out "step" in the initially thicker supporting substrate. In various examples, a dielectric material in a block or other shape may be attached to the substrate to form the protrusion at a desired angle to the substrate plane. As noted above, the protrusion (regardless if attached material or formed by cutting out a step in a thicker substrate) protrudes from the substrate plane at an angle, such as about 90°. In various examples, a protrusion such as 204 in FIG. 2 may protrude from the substrate 202 at a different angle, such as for example, a 45° or 60° angle, relative to the substrate plane 203. A protrusion, such as protrusion 204 in FIG. 2, may comprise, for example, a dielectric material such as SiO_2, Al_2O_3, or MgO. The protrusion 204 can provide structural support for the depositing of dielectric and/or metal, metal oxide or metal nitride layers at an angle to the substrate plane 203.

Steps 106, 108, 110 and 112 provide an embodiment of a fabrication method to produce a tri-layer thin film structure or device stack further comprising spaced apart pairs of reducible metal oxide or metal nitride sheet. The steps comprise OAD (low or high angle), or any other deposition techniques. Complementary Metal-Oxide Semiconductor (CMOS) processes, such as OAD, can ordinarily allow for the layers to be deposited with an accurate and repeatable thickness. Steps 106, 108, 110 and 112 comprise (106) depositing a first reducible metal oxide or metal nitride sheet as a thin film; (108) depositing an inner dielectric thin film sheet over the first reducible metal oxide or metal nitride sheet; (110) depositing a second reducible metal oxide or metal nitride sheet as a thin film over the inner dielectric thin film sheet; and (112) depositing an outer dielectric thin film sheet over the first reducible metal oxide or metal nitride sheet. In this manner, the inner dielectric sheet comprise the

separator layer between the reducible metal oxide or metal nitride sheets, while the outer dielectric thin film sheet comprises the separator between the pairs of reducible metal oxide or metal nitride sheets. This process may then be repeated to form multiple device stacks having a thicker dielectric separator sheet deposited between adjacent tri-layer stacks.

Depending on the incident angle of the OAD, these deposited layers provided by steps 106, 108, 110 and 112 in FIG. 1 may end up on the top surface of the substrate not covered by the protrusion, on an edge of the substrate wafer facing into the deposit stream, on a surface of the protrusion facing into the deposit stream, and on the top surface of the protrusion. In various embodiments, detachable shades may be added that can act as shields against the deposition onto one or more of these surfaces, such as for example, on the top surface of the protrusion. Such shades may comprise a detachable metallic, ceramic, or polymer material. In other examples, one or more sacrificial layers may be added to a surface targeted for OAD, including, for example, a dissolvable polymer layer, such as acetone-dissolvable (poly)methylmethacrylate (PMMA), common in lift-off processing in semiconductor fabrication. In other embodiments, no shields or sacrificial layers are used and a subsequent planarization step provides removal of any unwanted deposited layers from a structure.

Steps 106 and 110 in FIG. 1 may comprise deposition of metal thin film sheets, (e.g., comprising Au, Pt, Pd, Ag, Os, Ir, Rh, or Ru), rather than deposition of reducible metal oxide or metal nitride sheets, to produce spaced apart pairs of metal electrode sheets and dielectric separator layers. However, in some instances, each tri-layer structure acts as a capacitor, and the high capacitance may interfere with the deposition of subsequent layers, such as if steps 106, 108, 110 and 112 are repeated. Deposition of reducible metal oxide or metal nitride sheets, on the other hand, obviates the possibility for each tri-layer substructure to act as a capacitor. As discussed herein, a later chemical reduction of at least a portion of the reducible

metal oxide or metal nitride sheets produces spaced apart electrode pairs, and avoids any deleterious effects of capacitance during various fabrication steps. In various embodiments, portions of each reducible metal oxide or metal nitride layer may be converted to highly conductive oxides (e.g., nickel (Ni) or cobalt (Co)) rather than to the corresponding metal.

The method exemplified in FIG. 1 further comprises a decision step 114. In step 114, it is determined whether a final number of pairs of reducible metal oxide or metal nitride sheets has been reached. In some implementations, the final number of pairs of reducible metal oxide or metal nitride sheets may be as few as one pair of reducible metal oxide or metal nitride sheets (i.e., one device stack). For two or more pairs of reducible metal oxide or metal nitride sheets, the steps 106 to 112 is repeated at least once more to provide for at least two pairs of reducible metal oxide or metal nitride sheets. In some implementations, the final number of pairs of reducible metal oxide or metal nitride sheets may be as large as several thousand pairs of reducible metal oxide or metal nitride sheets for example. The final number of pairs of reducible metal oxide or metal nitride sheets desired may depend on the design considerations for a sensor being manufactured from the fabricated structures disclosed herein, such as a desired testing speed, a type of molecule to be analyzed, or a desired footprint for the sensor, and other considerations. If the final number of pairs of reducible metal oxide or metal nitride sheets has not been reached in step 114, the process returns to step 106 to deposit another first reducible metal oxide or metal nitride layer on top of the previous outer dielectric thin film sheet.

Steps 106, 108, 110, 112 and 114 in FIG. 1 are better understood with reference to a structure produced by these steps and illustrated in FIG. 2. In FIG. 2, a protrusion 204 is attached to substrate 202, or a portions of a thicker substrate are cut away to form the step-like configuration. In the latter embodiment, substrate 202 and protrusion 204 comprise a contiguous material since the configuration was cut from a single block of substrate material.

OAD at an angle of from about 20° to about 70° relative to the substrate plane 203 can produce the layering depicted in the structure of FIG. 2. In various examples, an incident angle of from about 30° and about 60° may be used. The high angle of deposition results in deposition of each thin film layer on both the substrate surface (or on the previous layer deposited on the substrate surface) and also on the surfaces of the protrusion 204 (or onto the layers previously deposited on the protrusion 204). The vertical or near vertical deposits on the protrusion 204 are labeled as first reducible metal oxide or metal nitride sheet 207, inner dielectric layer 208, second reducible metal oxide or metal nitride sheet 215, and outer dielectric layer 212, whereas the horizontal or near horizontal deposits are labeled as first reducible metal oxide or metal nitride sheet 205, inner dielectric layer 209, second reducible metal oxide or metal nitride sheet 213, and outer dielectric layer 218. The vertical or near vertical portion and the horizontal or near horizontal portion of each layer necessarily connect since each deposit was cast onto both surfaces in each OAD step.

Step 106 of the method of FIG. 1 provides the first reducible metal oxide or metal nitride layer 207/205, which is in contact with the top surface of the substrate, the side of the protrusion facing the deposit stream, and on the top surface of the protrusion. Any depositing of the multiple layers on the edge of the substrate 202 facing the deposit stream is ignored (or were shielded and thus prevented). Each subsequent layer is then on top of the previous layer. Step 108 of the method of FIG. 1 provides the inner dielectric layer 208/209. Step 110 of the method of FIG. 1 provides the second reducible metal oxide or metal nitride sheet layer 215/213. Lastly, step 112 of the method of FIG. 1 provides the outer dielectric layer 212/218. As evident from the structure in FIG. 2, repetition of the steps 106, 108, 110 and 112 of FIG. 1 provides the tri-layer stack as shown.

Depositing the reducible metal oxide or metal nitride layers and the dielectric layers at an angle to the substrate plane 203 can allow for exposing multiple pairs of reducible metal

oxide or metal nitride sheets with a single planarization step. This can allow for scalability in fabricating a large number of reducible metal oxide or metal nitride pairs by depositing many reducible metal oxide or metal nitride and dielectric layers.

In various embodiments, OAD in steps 106 and 110 of FIG. 1 provide deposited reducible metal oxide or nitride layers (e.g., 207, 215 in FIG. 2) of from about 1 nm to about 100 nm in thickness. In some examples, the thickness of the deposited metal oxide or nitride layers is from about 1 nm to about 40 nm, or from about 5 nm to about 15 nm. In other examples, the thickness of the metal oxide or metal nitride layers is from about 2 nm to about 15 nm. The tolerance in the thicknesses of all of the deposited metal oxide or nitride layers is about 5%. The number of deposited metal oxide or nitride layers total from 2 to at least 10,000 layers. The depositing of reducible oxide or nitride layers may comprise RF sputtering, any other PVD, CVD, ALD methods, or electrodeposition.

A reducible metal oxide material for deposition herein can be selected from transition metal oxide or refractory metal oxide. In various embodiments, the reducible metal oxide material may comprise, but is not limited to, NiO, CoO, FeO, CuO, ZrO_2, TiO_2, VO_2, Cr_2O_3, and mixtures thereof. A reducible metal nitride material for deposition herein can be selected from p-block element nitrides, alkaline earth nitrides, transition metal nitrides and refractory metal nitrides. Nitrides for use herein include, but are not limited to, the nitrides of Mg, Be, Ca, Sr, Li, Zn, B, Si, Al, Ga, In, Tl, Zr, W, Ti, Va, Ta, Nb, Ni, Cr, Co, Fe, Ag, Au, Pt, Pd, Zr, Hg, and Cu. In various examples, nitrides that can provide a conductive metal upon reduction are useful. These include, but are not limited to, AuN, TiN, PtN, Pd_3N_4, ZrN, Ni_3N_2, Zn_3N_2, VN, CrN, Fe_2N, Ag_3N, Co_2N, Co_4N_2, and Cu_3N. In other embodiments, a metal oxide or nitride is converted to a highly conductive metal oxide, e.g., to produce a nickel or a cobalt oxide.

In various embodiments, deposition steps 108 and 112 of FIG. 1 comprise deposition of inner and outer dielectric layers (e.g., inner dielectric layer 208 and outer dielectric layer 212 in the structure of FIG. 2). The dielectric material can include an oxide, nitride, or fluoride, or other dielectric material, provided the material is not easily reduced during the process of reducing portions of the metal oxide or metal nitride layers to metal. In certain examples, inner and outer dielectric layers may comprise any combination of oxides such as SiO_2, MgO, CaO, Al_2O_3, various rare earth oxides, or other oxide, nitride (e.g., AlN, Si_3N_4, refractory nitride, rare earth nitride or a mixture of nitrides), fluoride, oxyfluoride, or oxynitride, or any other dielectric material not easily reduced by hydrogen annealing, forming gas (e.g., 5 vol. % H_2 in 95% Ar gas), or other reductive methods.

As illustrated in the structure of FIG. 2, deposition of the non-reducible dielectric layers 208/209, e.g., by sputter deposition, CVD, or ALD deposition, results in a thickness of from about 1 nm to about 40 nm for the inner dielectric layers 208/209. In other examples, the thickness of the inner dielectric layers is from about 2 nm to about 15 nm thick. The tolerance in the thicknesses of all of the deposited inner dielectric layers is about 5%.

In various embodiments, each outer dielectric layer 212 separating neighboring tri-layer device stacks may have a width of from about 500 to at least about 20,000 nm, or about one order of magnitude thicker than the thickness of any one inner dielectric sheet separating first and second reducible metal oxide or metal nitride layers in a device stack. In various examples, a thickness for an outer dielectric layer 212 can be, for example, in the range of from about 500 to about 5,000 nm. The tolerance in the thicknesses of all of the deposited outer dielectric layers is about 5%. A separation between adjacent tri-layer device stacks of about 500 to about 5,000 nm reduces electrical, inductive, capacitive, or other interferences.

In various embodiments, a desired thickness for each of the outer dielectric sheets can be at least about 1 μm or at least about 10 μm, while a desired thickness for each of the inner

dielectric sheets can be at most about 50 nm or at most about 20 nm. In some implementations, the thickness of the inner dielectric sheets can be at most about 10 nm. Having an accurately controlled inner dielectric layer thickness can improve the chances for reliable and reproducible attachment of certain molecules to the pairs of metal sheets once reduced from the oxide or nitride. Reliable and reproducible attachment of certain molecules in a molecular sensor results in more accurate readings from a molecular sensor constructed out of the structures herein, since it is less likely that other types of molecules inadvertently attach given the relatively precise spacing to coordinate with the size of the chosen molecules.

With continued reference to FIG. 2, utilizing OAD without any dissolvable sacrificial layers or removable shades on the protrusion 204 results in the top surface of the protrusion 204 (the surface opposite the substrate 202) being covered with multilayer thin films. Nonetheless, a planarization polishing process removes these film depositions on the surface of the protrusion 204 so as to achieve a structure as in FIG. 3. In some instances, the very top layer of the protrusion 204 is sacrificed in the planarization that removes all of the layers deposited on the protrusion 204.

In other embodiments, a thin adhesion promoting layer may be deposited at the interface between the metal oxide or nitride sheets and the inner dielectric sheet to improve the adhesion at the interface. For example, an about 1 to about 5 nm thick film may be deposited at any interface of layers. In various examples, the film may comprise a material such as Ti, Cr, Al, Zr, Mo, Nb, Ta, or Hf.

With reference again to FIG. 1, various embodiments of a fabrication method in accordance to the present disclosure further comprise step 115, which is to add a mechanically supportive block material to the structure resulting from the repetition of deposition steps 106, 108, 110 and 112. A mechanically supportive block can be added with a

gap-filling curable polymer. A mechanically supportive block material may be attached adjacent to the deposited multilayer stack. In some implementations, this is accomplished by attaching a block of ceramic material or polymer material, or by depositing a polymer material and subsequently curing the polymer. Any space between the added supporting block and the previously deposited multilayers can be filled with a UV-curable, electron beam curable, or thermally curable polymer such as PMMA or hydrogen silsesquioxane (HSQ) resist. The HSQ resist layer thus deposited can be hardened by additional thermal curing to be close to the hardness of SiO_2 type material. The mechanically supportive block material can be added in step 115 to facilitate subsequent planarization of the structure, as discussed herein. Further a mechanically supportive block material can provide support during subsequent manipulations of the structure, such as during a subsequent packaging into devices.

An exemplary mechanically supportive block material 223 is illustrated on the structure of FIG. 2. As disclosed, this material can be added in step 115 by attaching a block of ceramic material or polymer material, or by depositing a polymer material and subsequently curing the polymer.

With reference again to the method of FIG. 1, step 116 comprises planarizing the structure produced from the previous steps in FIG. 1. As discussed, the added mechanically supportive block material aids in mechanically stabilizing the structure during the planarization process. The step 116 of planarizing may comprise, for example, CMP polishing, focused ion beam (FIB) etching, or PMMA or HSQ filling and subsequent "etching back" by reactive ion etch (RIE). Planarization step 116 levels all of the top edges of the metal oxide or nitride layers along with the inner and outer dielectric layers. The step 116 also exposes end portions of each of these layers, on which certain additional processes may be implemented.

Planarization step 116 of FIG. 1 is more clearly understood by reference to the structure in FIG. 3, which is an exemplary structure resulting from planarization of the structure in FIG. 2 across the planarization plane 217. Planarization plane 217 may be substantially parallel to substrate plane 203, or may be at an angle relative to substrate plane 203. Note that the structure in FIG. 3 would look the same if the planarization plane 217 in FIG. 2 was lowered slightly closer to the substrate plane 203 such that a small portion of the protrusion 204 and a small portion of the mechanically supportive block material 223 were both sacrificed. In various examples, planarization at plane 217 or just below the top surface of the protrusion 204 suffices to remove the very top surfaces of the protrusion 204, the metal oxide or nitride sheets, the inner dielectric sheets, and the outer dielectric sheets, to expose the edges of all of the layers and to level them substantially co-planar with the top surface of the protrusion 204. In various embodiments, planarization results in a structure having a top surface 385 substantially parallel to the substrate plane 303, as illustrated by the resulting structure of FIG. 3.

With continued reference to FIG. 3, the planarized structure illustrated comprises protrusion 304, mechanically supportive block material 323, and a number of tri-layer device stacks 340, 350, 360, 370, and so forth, (depending on how many times steps 106, 108, 110 and 112 in FIG. 1 were repeated prior to planarization), all with co-planar top surfaces exposed from the planarization step. Each device stack, such as tri-layer stack 340 further comprises a first reducible metal oxide or metal nitride layer 341, an inner non-reducible dielectric layer 342, and a second reducible metal oxide or metal nitride layer 343. Each tri-layer stack is arranged with the inner non-reducible dielectric layer sandwiched between two reducible metal oxide or metal nitride layers. Each tri-layer stack, 340, 350, 360, 370, etc., is separated by a wider outer dielectric layer, such as outer dielectric layer 344 that separates tri-layer stack 340 and tri-layer stack 350. At top surface 385, each of the layers 341, 342, 343,

344, and so forth, (depending on total number of tri-layer device stacks), further comprise exposed end portions co-planer with the top surface 385. These exposed end portions, made by planarization, are available for subsequent manipulation such as reductive chemistry.

FIG. 4 is a flowchart of an embodiment of a fabrication method that begins with a planarized substrate (such as the structure illustrated in FIG. 3) and comprises a continuation of the method of FIG. 1. FIG. 4 describes the process of obtaining gold (Au) electrode islands beginning with accurate thickness controlled metal oxide or metal nitride layer pairs. In other embodiments, a structure such as in FIG. 3 may be sliced into several or more wafers or "chips" prior to reduction of metal oxide or nitride to metal. The slicing may be conducted parallel to the plane 303 of substrate 302 to produce wafers of uniform dimensions. Then a plurality of these wafers may be collectively exposed to the reduction conditions in Step 402.

Step 402 of the method of FIG. 4 comprises reducing the exposed end portions of the reducible metal oxide or metal nitride sheets within each tri-layer device stack using a suitable reducing agent, such as hydrogen, optionally in an inert atmosphere such as Argon (Ar).

In certain instances, the reduction of a reducible metal oxide, such as NiO, CoO, FeO, CuO, by hydrogen follows the generalized chemical equation:

$$MO + H_2 \rightarrow M + H_2O$$

In certain instances, the reduction of a reducible metal nitride, such as Fe_2N, with hydrogen follows the generalized chemical equation (also called "denitridation"):

$$2Fe_2N + 3H_2 \rightarrow 4Fe + 2NH_3$$

The depth to which the exposed end portion of a reducible metal oxide or metal nitride sheet is reduced by these and other reactions is dependent on the reducing atmosphere strength (i.e., $[H_2]$), the temperature and pressure and length of time of the reaction, amongst other variables. In various examples, the reduction of a reducible transition metal oxide, such

as NiO, CoO, FeO, CuO, or refractory metal oxides like ZrO_2, TiO_2, or the reduction of a reducible transition metal nitride, such as Ti_2N, $TiN_{0.9}$, TiN, V_2N, VN, Cr_2N, CrN, Mn_4N, Mn_2N, Mn_3N_2, Fe_4N, Fe_2N, Co_3N, Co_2N, Ni_3N, ZrN, Nb_4N_3, Nb_2N, NbN, $NbN_{0.95}$, Mo_2N, MoN, $TcN_{0.75}$, Hf_3N_2, HfN, Ta_3N_5, Ta_2N, TaN, $TaN_{0.8}$, $TaN_{0.1}$, W_2N, WN and Re_2N, by hydrogen is conducted at a temperature of from about 300° C to about 800° C. In other examples, step 402 may comprise a forming gas anneal conducted at from about 300° C to about 600° C. The reaction conditions may be adjusted so as not to adversely affect the exposed end portions of any of the inner or outer dielectric sheets comprising a non-reducible oxide such as SiO_2, Al_2O_3, or MgO.

In various examples, methods for reducing exposed end portions of the reducible metal oxide or nitride layers without damaging the exposed end portions of the inner and outer dielectric sheets include, but are not limited to, providing selective reducing conditions (e.g., particular concentration of reducing gas, pressure and temperature), and providing different materials between reducible metal oxide or nitride layers and the dielectric layers. In the latter method, for example, the reducible metal oxide or nitride layers may comprise only nitride, whereas the inner and outer dielectric layers may comprise only oxide. In other instances, the reducible oxide or nitride layers may comprise only an oxide, but the metal of the oxide may be different from the metal of the oxide in the inner and outer dielectric layers. For example, a reducible metal oxide layer may comprise TiO_2 whereas the inner and outer dielectric layers may comprise SiO_2.

In various embodiments, the reduction step 402 in the method of FIG. 4 results in the formation of metal from the reducible metal oxide or metal nitride to a depth of from about 10 nm to about 10 μm as measured from the exposed end surface created by the planarization step. Thus, a structure after step 402 comprises metal electrode pairs at the top surface of the structure, i.e., the planarization surface, with the electrode metal ranging to a depth of from

about 10 nm to about 10 μm. The remaining portions of the metal oxide or metal nitride sheets are inaccessible to the reducing agent and remain as oxide or nitride material. However, it is important to note that the sides of the structure (e.g., the sides perpendicular to the planarized surface) are also exposed to the reducing atmosphere, and thus the resulting metal electrodes extend all the way from the planarized top of the structure down to the substrate for at least two sides of the structure or on each side that is exposed to the reducing conditions. If the resulting reduced structure is then cross-sectioned perpendicular to the planarized top surface (e.g., see FIG. 5B which illustrates this), then the depth of the reduction from the top can be seen. In various embodiments, reduction of metal oxide or nitride to the corresponding metal on one side of a structure, all the way from substrate up to top planarized surface, facilitates a later connection of the sheets into electrical circuits, regardless that inner portions of the metal oxide or nitride sheets still remain oxide or nitride.

In some variations, exposed end portions of metal oxide sheets are partially converted to highly conductive oxides, or to a mixture of metal and metal oxide. These conversions may be dependent on the lattice structure of the metal oxides.

The method then proceeds with step 404 to obtain a narrow exposed gap across the exposed end portions of the electrode pairs created in step 402. In step 404, two portions of mask, e.g., dielectric cover layers, are deposited on the top planarized surface of the device stack orthogonal or close to orthogonal to the electrode strips, and separated by a gap, thereby exposing only a short length of each end portion of the electrode sheet pairs within this gap. In other variations, two masked regions separated by a gap may be formed by using a patterning process, such as e-beam lithography or nano-imprinting, followed by etching an unmasked region to form the gap. In other examples, a mask line may be deposited on the planarized top surface of the structure, perpendicular to the exposed edges of electrodes and dielectric layers appearing as parallel strips on the planarized surface. The mask line can be

deposited on the top surface of the structure using, for example, an HSQ resist. Two portions of dielectric cover layer are then deposited on both sides of the mask line. After removal of the mask line, the dielectric cover layer appears as a single portion with a "window" where the mask line was, having a width of the desired gap. In some examples, the gap between dielectric cover layers can have a width between about 2 nm to about 40 nm, or from about 5 to about 15 nm, such as to facilitate targeted deposition of metal islands and/or selective attachment of only a single molecule across each pair of electrode strips. The dielectric cover layers forming these masked regions are optionally removable. This process is more clearly understood when the structures that result from these steps are illustrated and described. The mask material may comprise, for example, SiO_2, or polymethylmethacrylate (PMMA).

In step 406, small metal "islands" are deposited on the exposed electrode pairs such that there is one metal island per electrode, located close to the end of the electrode facing the other electrode in the pair of electrodes. These metal islands may comprise gold (Au), platinum (Pt) or palladium (Pd), amongst other metals. The metal islands may be electro-deposited or vacuum deposited onto the ends of the electrodes.

In various embodiments, steps 402, 404 and 406 of FIG. 4 produce the various structures depicted in FIGS. 5A-5D.

With reference now to FIG. 5A, a planarized structure (e.g., resulting from completion of the steps of FIG. 1) comprises an arrangement of reducible metal oxide or metal nitride sheet pairs, each pair separated by outer dielectric layers and each metal oxide or metal nitride sheet within a pair of sheets separated by an inner dielectric layer. Specifically, the structure 500a comprises the protrusion 504, first reducible metal oxide or metal nitride layer 541, inner dielectric layer 542, second reducible metal oxide or metal nitride layer 543, and outer dielectric layer 544, with the entire stack planarized on the surface opposite the substrate. The pattern including the elements 541, 542, 543 and 544

repeats for as many times as the method steps 106, 108, 110 and 112 of FIG. 1 were repeated. The structure 500a shows a stack of layers resulting from only 4-cycles of the deposition process, followed by planarization to level the layers into coplanarity and provide the exposed end portions of each layer on the surface opposite the substrate. Note that in structure 500a the last outer dielectric layer was not deposited, and instead, a mechanically supportive block material 523 was used at the end of the multi-layered stack for mechanical support, which is attached to the final second reducible metal oxide or metal nitride layer.

With continued reference to structure 500a in FIG. 5A, the top of the structure opposite the substrate comprises the exposed end portions 560 of each of the reducible metal oxide or metal nitride layers. This planarized top surface also comprises exposed end portions for all of the inner and outer dielectric layers, the protrusion and the mechanically supportive block material (unlabeled in this illustration). These exposed end portions of reducible metal oxide or metal nitride layers, the inner and outer dielectric layers all appear as thin parallel strips on the planarized top surface of the structure. The exposed end portions of reducible metal oxide or metal nitride layers are available for reduction to the corresponding metal, e.g., by exposure to H_2.

FIG. 5B illustrates the structure 500b resulting from reduction of portions of the reducible metal oxide or metal nitride layers in the structure 500a of FIG. 5A, in accordance with step 402 in FIG. 4. The exposed metal portions 551 and 553 are the result of treatment of the structure 500a in FIG. 5A with a suitable reducing agent that reduces the exposed reducible metal oxide or nitride end portions into the corresponding base metal. With the structure 500b cross-sectioned as shown, the depth of the reduction from oxide/nitride to metal can be seen by the height of the metal portions 561 and 563, which measure from about 10 nm to about 10 μm in height. The cross-sectioned portion of the structure shown also shows the remaining reducible metal oxide or metal nitride material 571 and 573 untouched

by the reducing conditions. Other than on the sides of the structure, these intact metal oxide or metal nitride portions extend down to the substrate. As illustrated in structure 500b, the inner dielectric layers, e.g., 572, the outer dielectric layers, e.g., 574, as well as the protrusion 504 and the mechanically supportive block material 523 remain untouched by the reducing conditions for converting exposed portions of metal oxide or nitride to metal.

FIG. 5C illustrates an embodiment of a structure 500c resulting from addition of mask layers onto the planarized surface of substrate 500b in FIG. 5B in order to block some of the surface area of the metal strips, in accordance with step 404 of FIG. 4. The masked structure 500c comprises two masked layer portions 580 and 581. Since the exposed parallel metal strips span across the planarized surface of the structure, there may be too much exposed metal surface area for precise placement of metal islands onto the metal strips. Thus, the purpose of the mask regions 580 and 581 is to mask all of the exposed metal strips except for short segments such as 556 and 557. As mentioned in the context of FIG. 4 and step 404, the masked regions may be deposited on the planarized surface substantially perpendicular to the parallel metal strips, such as with two portions of masking separated by a gap of from about 2 nm to about 40 nm, or from about 5 to about 15 nm for targeted placement of metal islands and/or for controlled attachment of molecules onto the metal electrode strips. The gap is indicated as "GAP 585" in structure 500c of FIG. 5C. As mentioned herein, the masking need not comprise separate masking layer portions, but may instead comprise a continuous portion with a "window" defining the gap.

With continued reference to FIG. 5C, the exposed portions 556 and 557 of each electrode strip, appearing substantially as rectangles of nanoscale proportions, measure, for example, from about 1 nm to about 40 nm, or from about 5 nm to about 15 nm, or from about 2 nm to about 15 nm in width, by about 2 nm to about 40 nm, or from about 5 to about 15 nm in length. In various embodiments, an exposed electrode strip segment 556 may measure

about 2 nm in width by about 10 nm in length. In other embodiments, the exposed strip segment 556 may measure about 5 nm in width by about 15 nm in length. These short segments of electrode strips then become the targets for metal island deposition, as per step 406 of FIG. 4.

FIG. 5D illustrates an embodiment of a structure 500d resulting from metal island deposition to the exposed portions of the electrode strips, in accordance with step 406 of FIG. 4. As discussed in the context of FIG. 4, gold (Au), platinum (Pt) or palladium (Pd) islands may be deposited onto the exposed electrode strip segments by electro-deposition or vacuum deposition, for example. As illustrated in FIG. 5D, the metal islands 591 and 592 (e.g., comprising Au, Pt, or Pd), are deposited on the exposed electrode strip segments 556 and 557 respectively. In various embodiments, one discrete island is deposited per exposed electrode strip segment. In certain aspects, the GAP 585 can be narrowed as necessary to promote deposition of only one metal island per exposed electrode strip segment. As shown in the exemplary structure 500d of FIG. 5D, each exposed electrode strip segment has a single metal island deposited thereon. The structure is only shown with eight such segments and islands, although as discussed herein, the number of these segments and islands may number in the thousands, tens of thousands, hundreds of thousands, millions, tens of millions, or more.

In an optional step, the metal islands, e.g., Au, Pt or Pd islands 591 and 592 in FIG. 5D, may be "balled up" into substantially spheroidal configuration by an annealing step. The metal islands initially deposited may be square or rectangular in shape, and therefore the annealing step after deposition can further reduce the exposed surface area of the deposited islands by converting each island into more of a spheroidal shape. After reshaping of the metal islands, molecules may then be bonded to each metal island. In various embodiments, a single long molecule, such as a double-stranded DNA oligomer, with both the 3' and 5' ends

functionalized with groups capable of bonding to the metal islands, may be placed across each pair of metal islands in each electrode pair.

FIG. 6 sets forth another embodiment of a method of producing a structure usable in a molecular sensor that also begins from the end of the method of FIG. 1. As indicated at the bottom of FIG. 1, processes to reach a structure usable in a molecular sensor may follow two separate and distinct pathways, namely the method depicted in FIG. 4 or the method depicted in FIG. 6.

The fabrication method exemplified by the steps in FIG. 6 comprises a metal deposition and selective lift-off process to provide metal islands on electrode strips. The fabrication process begins with a planarized structure, such as the structure depicted in FIG. 3, or the similar structure depicted in FIG. 7A, or wafer slices obtained therefrom. In these beginning structures, the exposed end portions of the protrusion, reducible metal oxide or nitride layers, the inner and outer dielectric layers, and the optional mechanically supportive block material are coplanar, and the exposed end portions of the reducible metal oxide or nitride layers and the inner dielectric layers appear as parallel bands or strips on the top planarized surface of the structure.

In various embodiments, a structure usable in the metal deposition and selective lift-off process set forth in FIG. 6 may comprise different materials for the reducible metal oxide or nitride layers and the inner dielectric layers, such as to enable selective etching of the inner dielectric layers in the presence of the reducible metal oxide or nitride layers. In a non-limiting example shown in FIG. 7A, the inner dielectric layers 742 may comprise SiO_2, whereas the reducible metal oxide or nitride layers 741, 743 may comprise NiO, CuO or CoO, such as to allow for selective etching of the exposed end portions 740 of the inner dielectric layers in the presence of the exposed end portions 760 of the reducible metal oxide or nitride layers. In various aspects, the protrusion (e.g., protrusion 704 in FIGS. 7A-F) may

also comprise a dielectric material such as SiO_2, Al_2O_3 or MgO, and the protrusion may also be etched concurrently with the exposed end portions of the inner dielectric layers. The exemplary structure in FIG. 7B illustrates a result of selective etching of both the exposed end portions 740 of the inner dielectric sheets and the exposed top surface of the protrusion 704, without damage to the exposed end portions 760 of the reducible metal oxide or nitride layers.

The first step 602 of the fabrication process in FIG. 6 comprises selective etching of the exposed end portions of the inner dielectric layers to form grooves, (e.g., grooves 710 in FIG. 7B). In some implementations, removal of an exposed end portion of inner dielectric material to create each groove can be accomplished by etching the inner dielectric sheet using an etching process such as RIE, sputter etching, or chemical etching, such as with HF. In these ways, a groove 710 is formed in each of the inner dielectric sheets. In various embodiments, each groove etched in the inner dielectric sheets measures from about 0.1 to about 1 mm in depth from the planarization surface, as illustrated by the dimension "*d*" in FIG. 7B. In other words, the extent of removal of inner dielectric sheet material, "*d*," is from about 0.1 to about 1 nm from the exposed end portion of the inner dielectric sheet 742 created by the planarization. Removal of the exposed end portions of each of the inner dielectric sheets provides free space for depositing PMMA-type resist in the next step 604 of the process. In this particular example in FIG. 7B, illustrating the effects of selective etching (step 602 in FIG. 6), the protrusion 704 is shown to also be etched to about the same degree as the exposed end portions of the inner dielectric sheets. Such concomitant etching can be seen in structures wherein the protrusion 704 comprises the same material as the inner dielectric sheet layers, such as SiO_2.

Depending on the method used to remove the exposed end portions of each inner dielectric sheet, the groove (e.g., 710 in FIG. 7B) thus created may have a shape other than

rectangular cuboid as illustrated. For example, portions of the inner dielectric sheet adjacent each reducible metal oxide or nitride sheet may remain after partial removal of dielectric material such that a cross-sectional view of the groove may appear parabolic rather than rectangular or square. Grooves need not be fully cleaned out of all dielectric material to provide the air space to be filled by PMMA-type resist in the next step.

As set forth in FIG. 6, the fabrication process continues with step 604, the filling in of the grooves with a PMMA-type resist material. The PMMA-type resist material, used to fill the grooves, may be selected from polymethylmethacrylate (PMMA), SU-8 (a bisphenol-A Novolac epoxy), poly(methy-2-chloroacrylate), or hydrogen silsesquioxane (HSQ), or other materials usable as sacrificial resist. The material for filling is chosen for its ability to be sacrificed (e.g., washed out) even when covered with a metal deposit layer in later steps of the fabrication method. Step 604 is also known in lithography as "trench filling." Optionally, the step 604 comprising trench filling of the grooves with PMMA-type resist material may be following by another planarization step 606 to level all the exposed end portions of the layers, including the PMMA-type material portions, into coplanarity.

An exemplary structure provided by step 604 in FIG. 6 (and optional second planarization step 606) is illustrated in FIG. 7C. The structure in FIG. 7C comprises portions 785 and 795 of PMMA-type resist material that will filled into the grooves in the inner dielectric sheet layers. Portion 785 is a block of PMMA-type resist material over the protrusion 704 while the portions 795 of PMMA-type resist material are the portions filling the grooves in the inner dielectric sheet layers. The intermediate structure in FIG. 7C further comprises the intact reducible metal oxide or nitride layers 741 and 743, with exposed end portions 760 on the newly planarized top surface of the structure, and the outer dielectric layers 744. In this structure, each of the exposed end portions of the PMMA-type resist, the reducible metal oxide or nitride layers, and the outer dielectric layers, appear as parallel strips

on the planarized top surface of the structure. In this structure, the inner dielectric layers cannot be seen on the planarized top surface since they are beneath the PMMA-type resist fill material.

The next step of the fabrication process set forth in FIG. 6 comprises step 608, the deposition of a metal layer across the top surface of the structure, over the top of all of the exposed end portions of the metal oxide or nitride layers, the outer dielectric layers and the PMMA-type resist portions. In certain embodiments, the metal deposited comprises gold (Au). In various aspects, a gold (Au) layer having a thickness of from about 5 nm to about 15 nm may be sputter deposited onto the structure.

A structure resulting from step 606 of FIG. 6 is illustrated in FIG. 7D. The structure in FIG. 7D comprises a deposited metal layer 775, further comprising, for example, sputter deposited gold (Au) of from about 5 nm to about 15 nm in thickness. The metal layer 775 is shown to cover the PMMA-type resist material portions 795 and the exposed end portions of each of the metal oxide or nitride layers 741 and 743. The inner dielectric layers 742 are shown to reside beneath the PMMA-type resist portions 795. The outer dielectric layers 744 extend up to the planarized surface, now coated with a metal deposit layer 775.

The next step in the metal deposition and selective lift-off process of FIG. 6 is step 610, the removal of the sacrificial PMMA-type resist portions. Washing away of the PMMA-type resist material also removes any metal deposited on top of the PMMA-type resist portions but not deposited metal on the metal oxide or nitride layers. A structure resulting from step 610 of FIG. 6 is illustrated in FIG. 7E. The resulting structure shown comprises parallel strips of metal (e.g., Au) 776, 777, 778 and 779, which can operate as pairs of metal electrodes in sensor devices comprising the structure shown. Each pair of metal strips is separated by an outer dielectric layer 744 as shown. Removal of the PMMA-type resist material is shown to have also restored the grooves 710 that were previously etched into the

exposed end portions of the inner dielectric sheet layers and temporarily trench filled with PMMA-type resist material. With these steps in the fabrication process, the reducible metal oxide or nitride layers 741 and 743 need not be reduced to the corresponding base metal because each of these layers are coated with the metal deposit 776, 777, 778 and 779, such as Au. However, if necessary, the structure shown in FIG. 7E may optionally be subjected to reducing conditions (e.g., H_2) to reduce the exposed edges of the metal oxide or nitride sheets on a side of the structure and not covered with metal deposits into base metal, such as to provide a conductive route to make various future electrical connections. Further illustrated in this structure is the protrusion 704, now cleaned off of any PMMA-type resist material and metal deposited on the PMMA-type resist material.

The next step in the metal deposition and selective lift-off process of FIG. 6 is step 612, which is the masking of selected regions of the top surface of the structure so that only short segments of deposited metal strips remain exposed for later manipulations. Step 612 of FIG. 6 is identical with step 404 of FIG. 4, and is therefore not detailed again in discussion of FIG. 6.

An exemplary structure resulting from the selective masking step 612 of FIG. 6 is illustrated in FIG. 7F. The structure comprises two separate masking layer portions 780 and 781 separated by a spacing designated as GAP 798. As mentioned in the context of FIG. 4 and step 404, the masked regions may be deposited on the top surface substantially perpendicular to the parallel metal strips, such as with the two portions of masking separated by a gap of from about 2 nm to about 40 nm, or from about 5 to about 15 nm for targeted placement of metal islands and/or for controlled attachment of molecules onto the exposed metal electrode strip segments. As mentioned previously herein, the masking need not comprise separate masking layer portions, but may instead comprise a continuous portion with a “window” defining the gap, such as obtained by first laying down a mask line. The

exposed portions 756 and 757 of each deposited metal strip, appearing substantially as rectangles of nanoscale proportions, measure, for example, from about 1 nm to about 40 nm, or from about 5 nm to about 15 nm, or from about 2 nm to about 15 nm in width, by about 2 nm to about 40 nm, or from about 5 to about 15 nm in length. In various embodiments, an exposed deposited metal strip segment 756 may measure about 2 nm in width by about 10 nm in length. In other embodiments, the exposed strip segment 756 may measure about 5 nm in width by about 15 nm in length.

These short segments of deposited metal strips then become the targets for metal island deposition, as per step 406 of FIG. 4 (with the option of annealing the deposits for ball-up), or for attachment of molecules, such as bridge molecules that can span across metal portions in each pair. In various embodiments, the deposited islands may comprise a different metal than the metal strip segments onto which they are deposited.

The notable difference between the masked structure in FIGS. 5C/5D and the structure in FIG. 7F is that the structure in FIG. 7F comprises slots 710. These slots 710 are what remain of the grooves selectively etched in the exposed end portions of the inner dielectric sheet layers. The slots run underneath the masked portions 780 and 781, and appear as small holes, one between each pair of exposed metal strip portions 756 and 757. This hole between metal strips facilitates bonding of a molecule between the pair of metal strips, bridging over the hole. Further, the hole improves electrical signaling in molecular sensors by allowing space for an analyte molecule to interact with a bridge molecule bonded to the metal strips.

By limiting the exposed area of the pairs of metal electrode strips to only a gap between dielectric cover layers, it is ordinarily possible to prevent more than one molecule from attaching to the exposed metal in each pair of metal strips. In a sensor application, when more than one molecule is attached to a pair of metal strips connected as source and

drain electrodes in a circuit, the readings for the particular circuit are affected. In the case where a current is measured between electrodes in a pair of electrodes through a bridging molecule in a circuit, the attachment of multiple molecules between the electrodes can lower the current measured across the electrodes and lead to undiscernible current measurements. Having only a single molecule per electrode pair improves the accuracy of a sensor device based on these structures. One bridge molecule per pair of metal electrode strips also ensures that analyte molecules only interact with one circuit, wherein the circuit comprises the pair of electrode strips and a single bridge molecule spanning between them.

In various embodiments, various structures disclosed herein are assembled into molecular sensor devices. These structures may be fabricated into large arrays, e.g., as many as 10,000 or at least 10 million structures. From structures such as the structures in FIG. 5D and in FIG. 7F, a plurality of lead conductors are connected to the plurality of electrode strips with each lead conductor connected to a respective electrode sheet. Depending on the fabrication route (FIG. 1 and FIG. 4, or alternatively FIG. 1 and FIG. 6), the electrode strips may comprise metal strips obtained from the reduction of reducible metal oxide or metal nitride, or metal strips obtained from deposition of a metal onto end portions of reducible metal oxide or metal nitride sheets. In various examples, the lead conductors may diverge in width as the lead conductor extends away from an edge of each metal electrode strip toward a contact. The lead conductors can be made of a conductive material such as gold for carrying a test signal from the electrode strips. The lead conductors may then fan out from a width of approximately 10 nm to a scale of micrometers to allow for soldering at the contacts. The contacts can include a contact pad array for circuit packaging, solder bonding, or wire bonding.

In some implementations, a gate electrode is optionally deposited parallel to the substrate plane and perpendicular to a reducible metal oxide or metal nitride plane defined by

a reducible metal oxide or metal nitride sheet. The gate electrode can include, for example, a Si or metallic electrode placed on a side of the substrate opposite the reducible metal oxide or metal nitride sheets or near a front portion of the reducible metal oxide or metal nitride sheets on the same side of the substrate as the reducible metal oxide or metal nitride sheets. Addition of an electrode gate can ordinarily improve the accuracy of readings from the pairs of electrode strips by imposing an electric field to regulate the charge carriers between the first electrode strip and the second electrode strip serving as source and drain electrodes in a pair of electrodes. An electrode gate can be especially useful in implementations where the electrodes include a semiconductor.

The foregoing description of the disclosed example embodiments is provided to enable any person of ordinary skill in the art to make or use the embodiments in the present disclosure. Various modifications to these examples will be readily apparent to those of ordinary skill in the art, and the principles disclosed herein may be applied to other examples without departing from the present disclosure. The described embodiments are to be considered in all respects only as illustrative and not restrictive, and the scope of the disclosure is therefore indicated by the following claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

CLAIMS

1. A method of manufacturing a structure usable in a molecular sensor device, the method comprising:

providing a substrate defining a substrate plane with a protrusion protruding from the substrate at an angle to the substrate plane;

depositing a first reducible metal oxide or metal nitride layer in an orientation along a side of the protrusion to form a first reducible metal oxide or metal nitride sheet at the angle to the substrate plane;

depositing an inner dielectric layer on the first reducible metal oxide or metal nitride layer to form an inner dielectric sheet at the angle to the substrate plane;

depositing a second reducible metal oxide or metal nitride layer on the inner dielectric layer to form a second reducible metal oxide or metal nitride sheet at the angle to the substrate plane, wherein the first reducible metal oxide or metal nitride sheet and the second reducible metal oxide or metal nitride sheet form a pair of sheets spaced apart by the inner dielectric sheet between the first reducible metal oxide or metal nitride sheet and the second reducible metal oxide or metal nitride sheet;

depositing an outer dielectric layer on the second reducible metal oxide or metal nitride layer to form an outer dielectric sheet at an angle to the substrate plane;

repeating the depositing of the first reducible metal oxide or metal nitride layer, the inner dielectric layer, the second reducible metal oxide or metal nitride layer, and the outer dielectric layer at least once to form spaced apart pairs of reducible metal oxide or metal nitride sheets with an inner dielectric sheet between each reducible metal oxide or metal nitride sheet in the pair of reducible metal oxide or metal nitride sheets and an outer dielectric sheet between each pair of reducible metal oxide or metal nitride sheets;

planarizing the pairs of reducible metal oxide or metal nitride sheets, the inner dielectric sheets, and the outer dielectric sheets to form exposed end portions of each; and

reducing the exposed end portions of the reducible metal oxide or metal nitride sheets to the corresponding metal to form parallel metal electrode strips.

2. The method of claim 1, wherein each inner dielectric layer is deposited with a first thickness and each outer dielectric sheet is deposited with a second thickness at least one order of magnitude greater than the first thickness.

3. The method of claim 1, further comprising attaching a mechanically supportive block material adjacent a stack formed by the deposited first reducible metal oxide or metal nitride layers, inner dielectric layers, second reducible metal oxide or metal nitride layers, and outer dielectric layers, prior to the step of planarizing.

4. The method of claim 1, wherein the inner dielectric sheets and the outer dielectric sheets comprise different dielectric materials.

5. The method of claim 1, wherein reducing the exposed end portions of the reducible metal oxide or metal nitride sheets to the corresponding metal comprises exposure to H_2.

6. The method of claim 1, further comprising placing at least one portion of a dielectric mask layer across the metal electrode strips to leave short segments of electrode strips exposed in a gap and depositing metal islands on the short segments of electrode strips.

7. The method of claim 5, wherein the gap measures from about 2 nm to about 40 nm.

8. The method of claim 1, further comprising connecting a plurality of lead conductors to metal electrode strips with each lead conductor connected to a respective electrode strip, wherein each lead conductor diverges in width as the lead conductor extends away from an edge of the electrode strip.

9. The method of claim 1, further comprising depositing a gate electrode parallel to the substrate plane and perpendicular to a reducible metal oxide or metal nitride plane defined by a reducible metal oxide or metal nitride sheet in the spaced apart pairs of reducible metal oxide or metal nitride sheets.

10. A method of manufacturing a structure usable in a molecular sensor device, the method comprising:

providing a substrate defining a substrate plane with a protrusion protruding from the substrate at an angle to the substrate plane;

depositing a first reducible metal oxide or metal nitride layer in an orientation along a side of the protrusion to form a first reducible metal oxide or metal nitride sheet at the angle to the substrate plane;

depositing an inner dielectric layer on the first reducible metal oxide or metal nitride layer to form an inner dielectric sheet at the angle to the substrate plane;

depositing a second reducible metal oxide or metal nitride layer on the inner dielectric layer to form a second reducible metal oxide or metal nitride sheet at the angle to the substrate plane, wherein the first reducible metal oxide or metal nitride sheet and the second reducible metal oxide or metal nitride sheet form a pair of sheets spaced apart by the inner

dielectric sheet between the first reducible metal oxide or metal nitride sheet and the second reducible metal oxide or metal nitride sheet;

depositing an outer dielectric layer on the second reducible metal oxide or metal nitride layer to form an outer dielectric sheet at an angle to the substrate plane;

repeating the depositing of the first reducible metal oxide or metal nitride layer, the inner dielectric layer, the second reducible metal oxide or metal nitride layer, and the outer dielectric layer at least once to form spaced apart pairs of reducible metal oxide or metal nitride sheets with an inner dielectric sheet between each reducible metal oxide or metal nitride sheet in the pair of reducible metal oxide or metal nitride sheets and an outer dielectric sheet between each pair of reducible metal oxide or metal nitride sheets;

planarizing the pairs of reducible metal oxide or metal nitride sheets, the inner dielectric sheets, and the outer dielectric sheets to form exposed end portions of each;

selectively etching an exposed end portion of each inner dielectric sheet to form grooves in each inner dielectric sheet descending from the planarized edge toward the substrate;

filling the grooves with PMMA-type resist material;

depositing a metal layer on the planarized surface of the structure; and

removing the PMMA-type resist material along with deposited metal residing thereon leaving an arrangement of pairs of spaced apart parallel metal electrode strips with the metal electrode strips in a pair of strips separated by a groove.

11. The method of claim 10, further comprising attaching a mechanically supportive block material adjacent a stack formed by the deposited first reducible metal oxide or metal nitride layers, inner dielectric layers, second reducible metal oxide or metal nitride layers, and outer dielectric layers, prior to the step of planarizing.

12. The method of claim 10, wherein the inner dielectric sheets and the outer dielectric sheets comprise different dielectric materials.

13. The method of claim 10, wherein the inner dielectric layer has a first thickness and the outer dielectric layer has a second thickness at least one order of magnitude greater than the first thickness.

14. The method of claim 10, further comprising placing at least one portion of a dielectric mask layer across the metal electrode strips to leave short segments of electrode strips exposed in a gap and depositing metal islands on the short segments of electrode strips.

15. The method of claim 14, wherein the gap measures from about 2 nm to about 40 nm.

16. A structure usable in a molecular sensor device, said structure comprising:

a substrate defining a substrate plane;

spaced apart pairs of reducible metal oxide or metal nitride layer sheets attached on an edge of the reducible metal oxide or metal nitride layer sheet to the substrate at an angle to the substrate plane;

an inner dielectric sheet disposed between the reducible metal oxide or metal nitride layer sheets in each pair of reducible metal oxide or metal nitride layer sheets; and

an outer dielectric sheet disposed between spaced apart pairs of reducible metal oxide or metal nitride layer sheets,

wherein an edge of each reducible metal oxide or metal nitride layer sheet, inner dielectric sheet and outer dielectric sheet opposite the substrate are coplanar.

17. The structure of claim 16, wherein each inner dielectric sheet has a first thickness and each outer dielectric sheet has a second thickness at least one order of magnitude greater than the first thickness.

18. The structure of claim 16, wherein the inner dielectric sheets and the outer dielectric sheets comprise different dielectric materials.

19. The structure of claim 16, further comprising a groove located on an exposed end portion of each inner dielectric sheet opposite the substrate.

20. The structure of claim 16, further comprising metal on the edge of each reducible metal oxide or metal nitride layer sheet that are coplanar to the edges of inner dielectric sheet and outer dielectric sheet opposite the substrate.

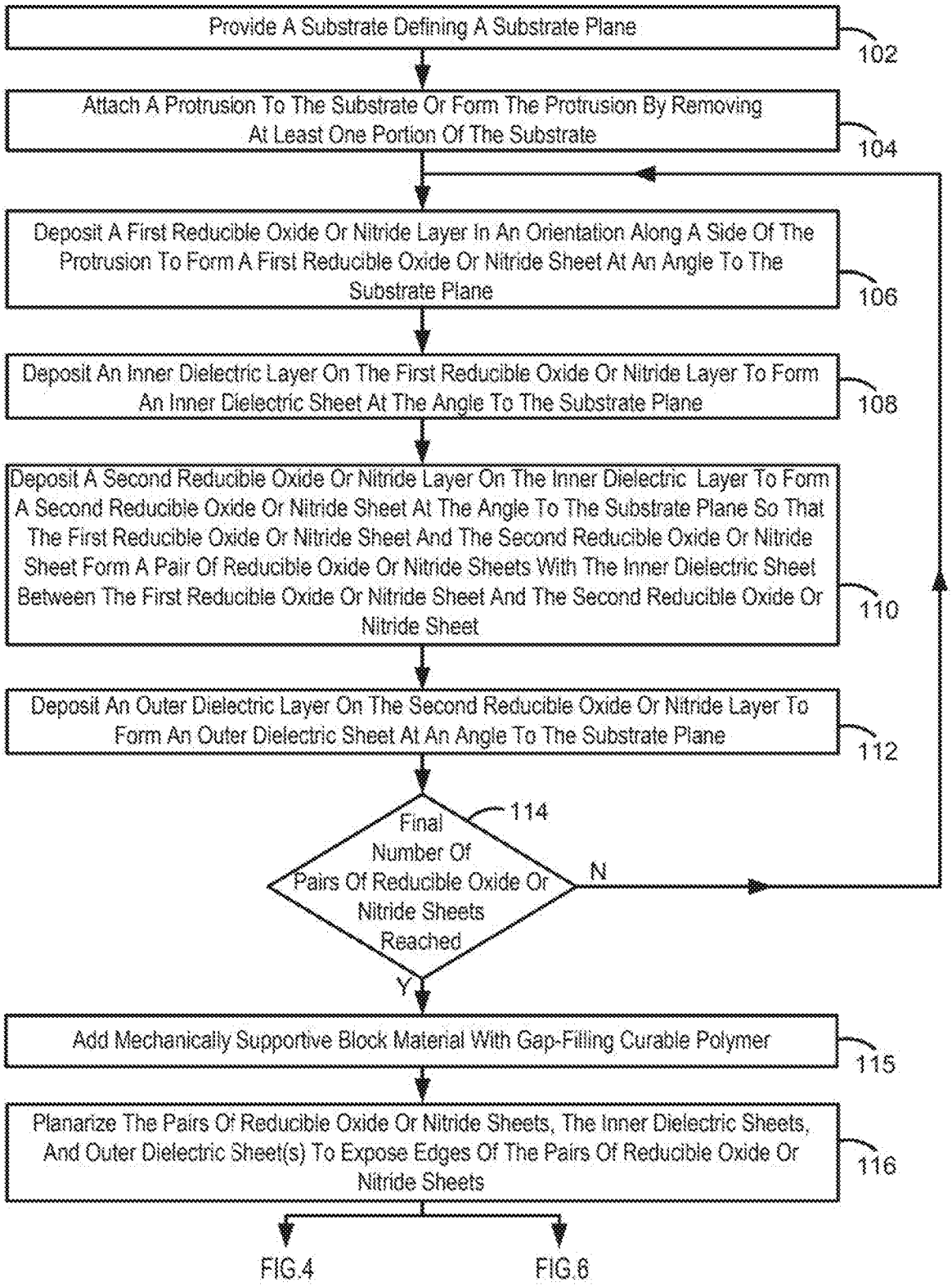

Provide A Substrate Defining A Substrate Plane
102
Attach A Protrusion To The Substrate Or Form The Protrusion By Removing At Least One Portion Of The Substrate
104
Deposit A First Reducible Oxide Or Nitride Layer In An Orientation Along A Side Of The Protrusion To Form A First Reducible Oxide Or Nitride Sheet At An Angle To The Substrate Plane
106
Deposit An Inner Dielectric Layer On The First Reducible Oxide Or Nitride Layer To Form An Inner Dielectric Sheet At The Angle To The Substrate Plane
108
Deposit A Second Reducible Oxide Or Nitride Layer On The Inner Dielectric Layer To Form A Second Reducible Oxide Or Nitride Sheet At The Angle To The Substrate Plane So That The First Reducible Oxide Or Nitride Sheet And The Second Reducible Oxide Or Nitride Sheet Form A Pair Of Reducible Oxide Or Nitride Sheets With The Inner Dielectric Sheet Between The First Reducible Oxide Or Nitride Sheet And The Second Reducible Oxide Or Nitride Sheet
110
Deposit An Outer Dielectric Layer On The Second Reducible Oxide Or Nitride Layer To Form An Outer Dielectric Sheet At An Angle To The Substrate Plane
112
Final Number Of Pairs Of Reducible Oxide Or Nitride Sheets Reached
114
N
Y
Add Mechanically Supportive Block Material With Gap-Filling Curable Polymer
115
Planarize The Pairs Of Reducible Oxide Or Nitride Sheets, The Inner Dielectric Sheets, And Outer Dielectric Sheet(s) To Expose Edges Of The Pairs Of Reducible Oxide Or Nitride Sheets
116
FIG.4
FIG.6

FIG.1

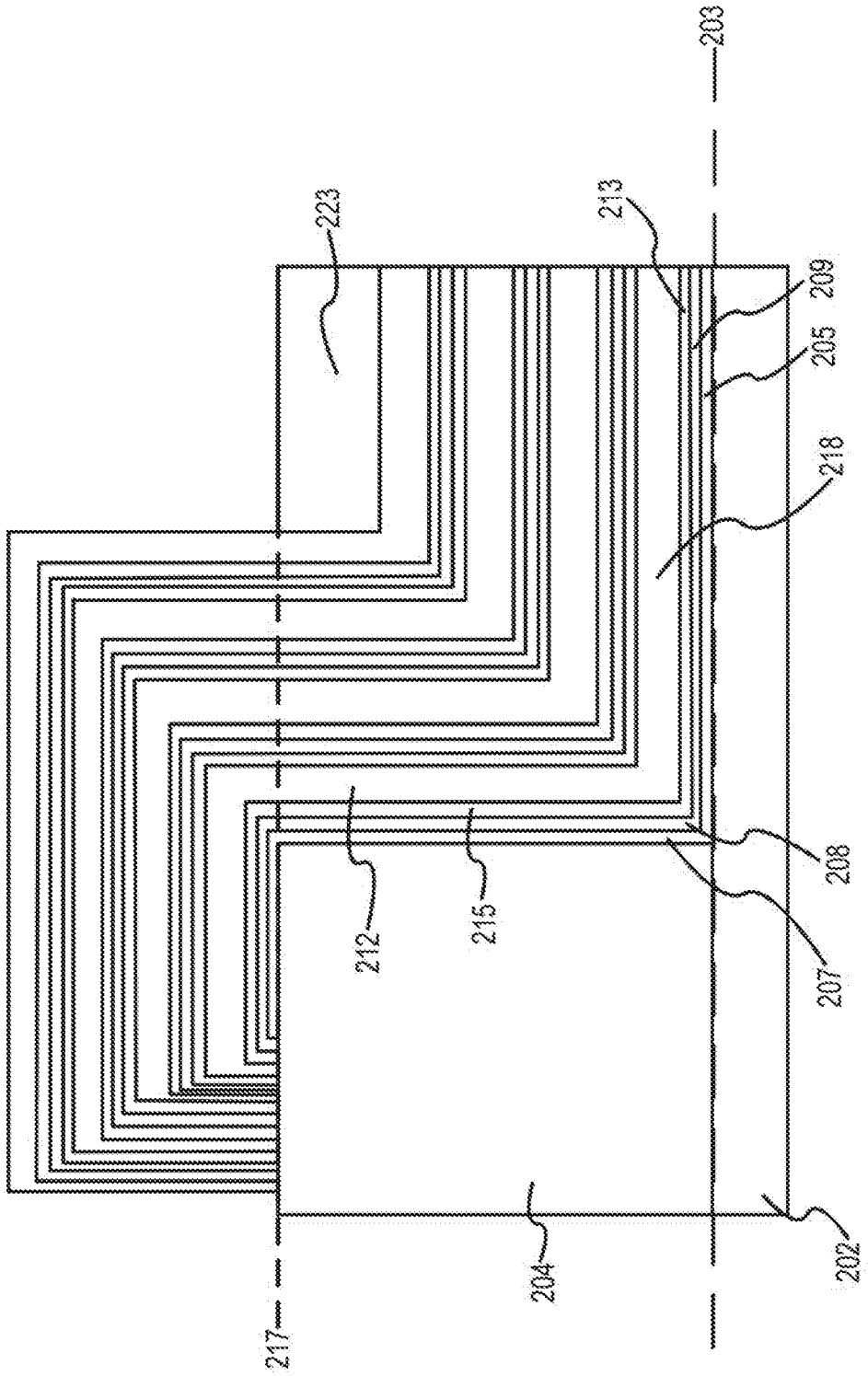


FIG.2

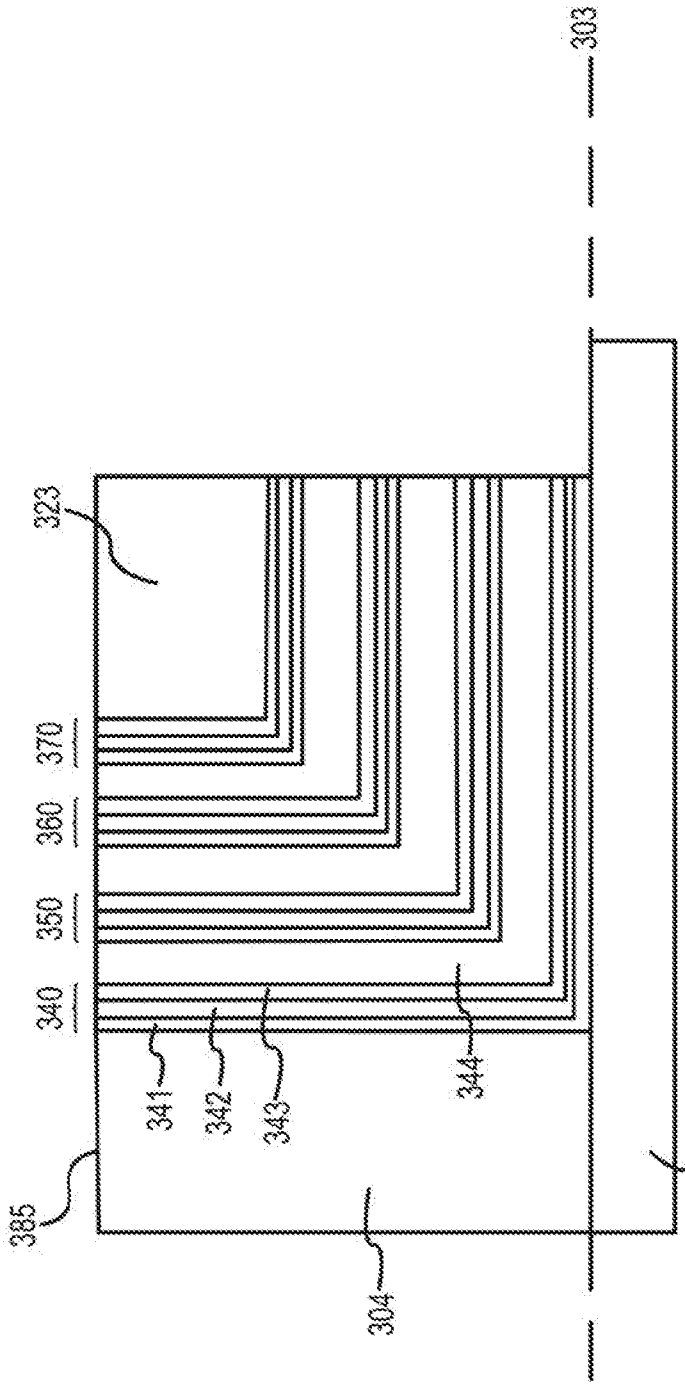


FIG.3

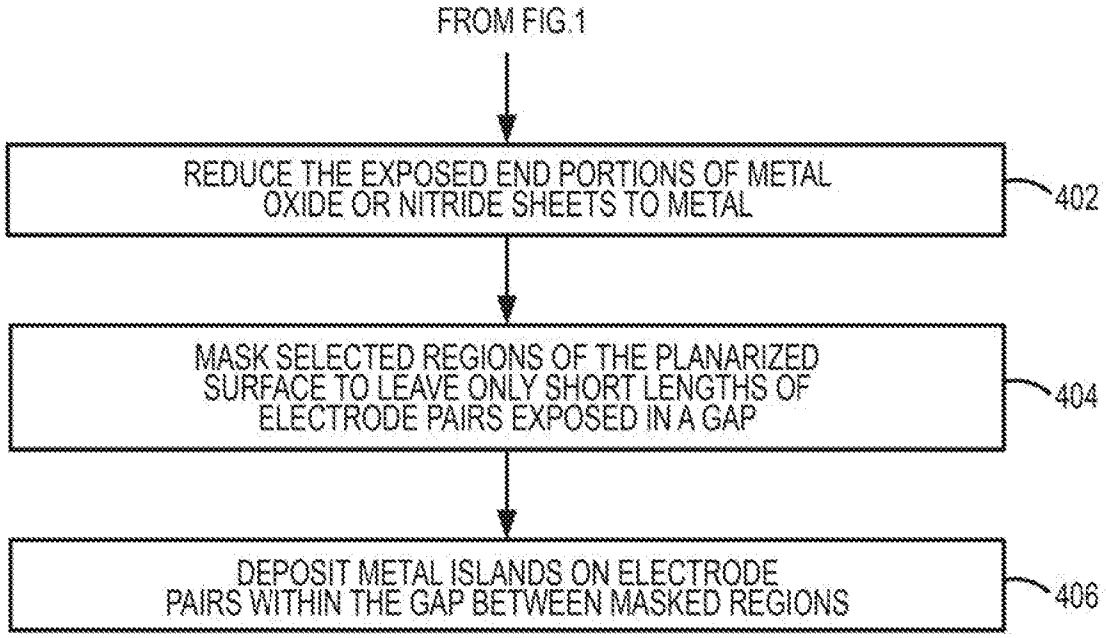
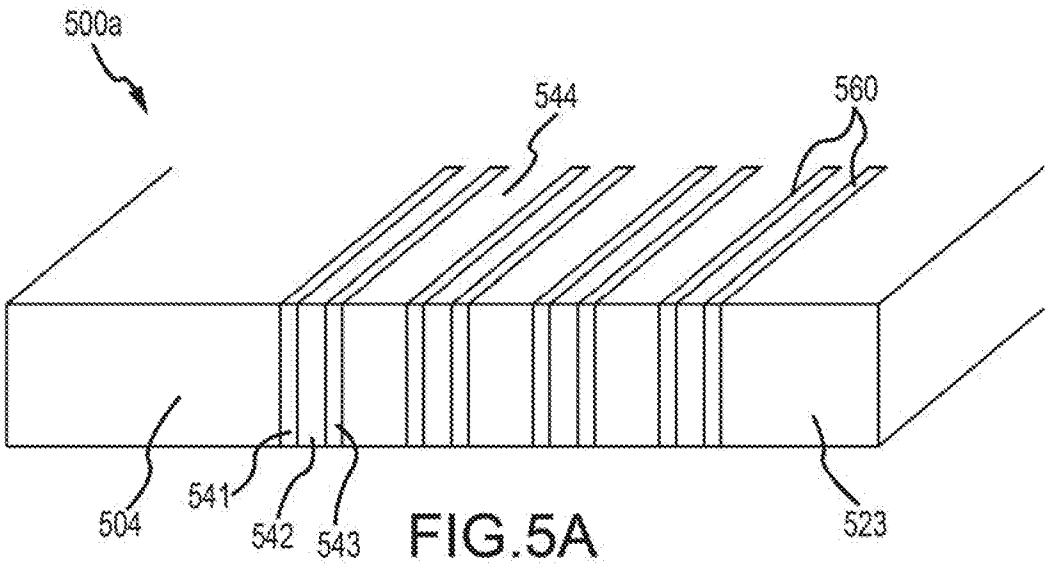

FROM FIG.1
REDUCE THE EXPOSED END PORTIONS OF METAL OXIDE OR NITRIDE SHEETS TO METAL
402
MASK SELECTED REGIONS OF THE PLANARIZED SURFACE TO LEAVE ONLY SHORT LENGTHS OF ELECTRODE PAIRS EXPOSED IN A GAP
404
DEPOSIT METAL ISLANDS ON ELECTRODE PAIRS WITHIN THE GAP BETWEEN MASKED REGIONS
406

FIG.4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541
542
543
523

FIG.5A

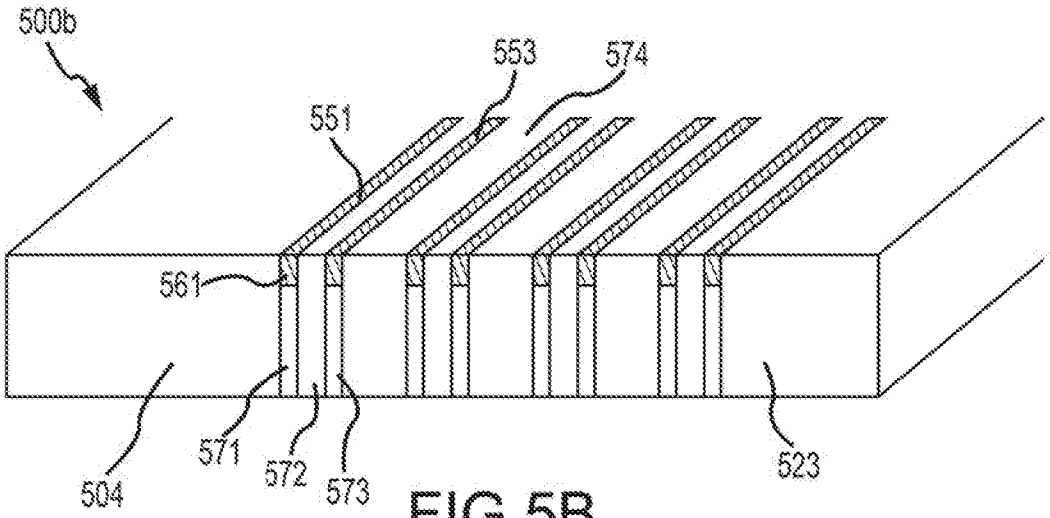
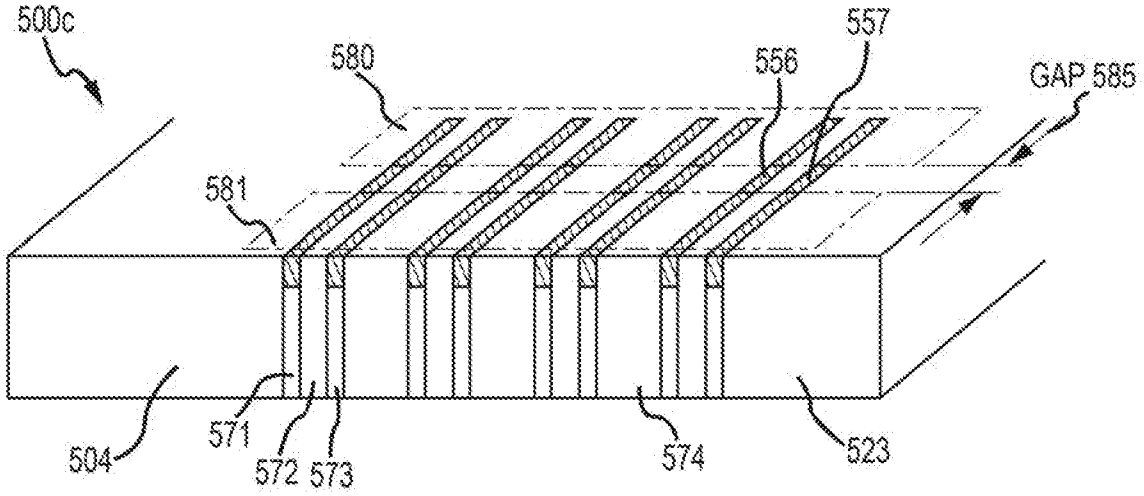

500b
553
574
551
561
504
571
572
573
523

FIG.5B


500c
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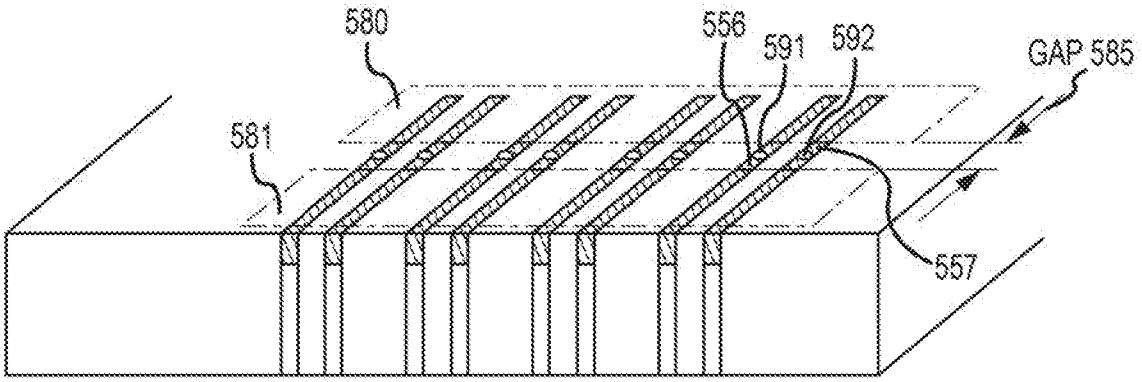
557
556
GAP 585
581
504
571
572
573
574
523

FIG.5C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GAP 585
581
557

FIG.5D

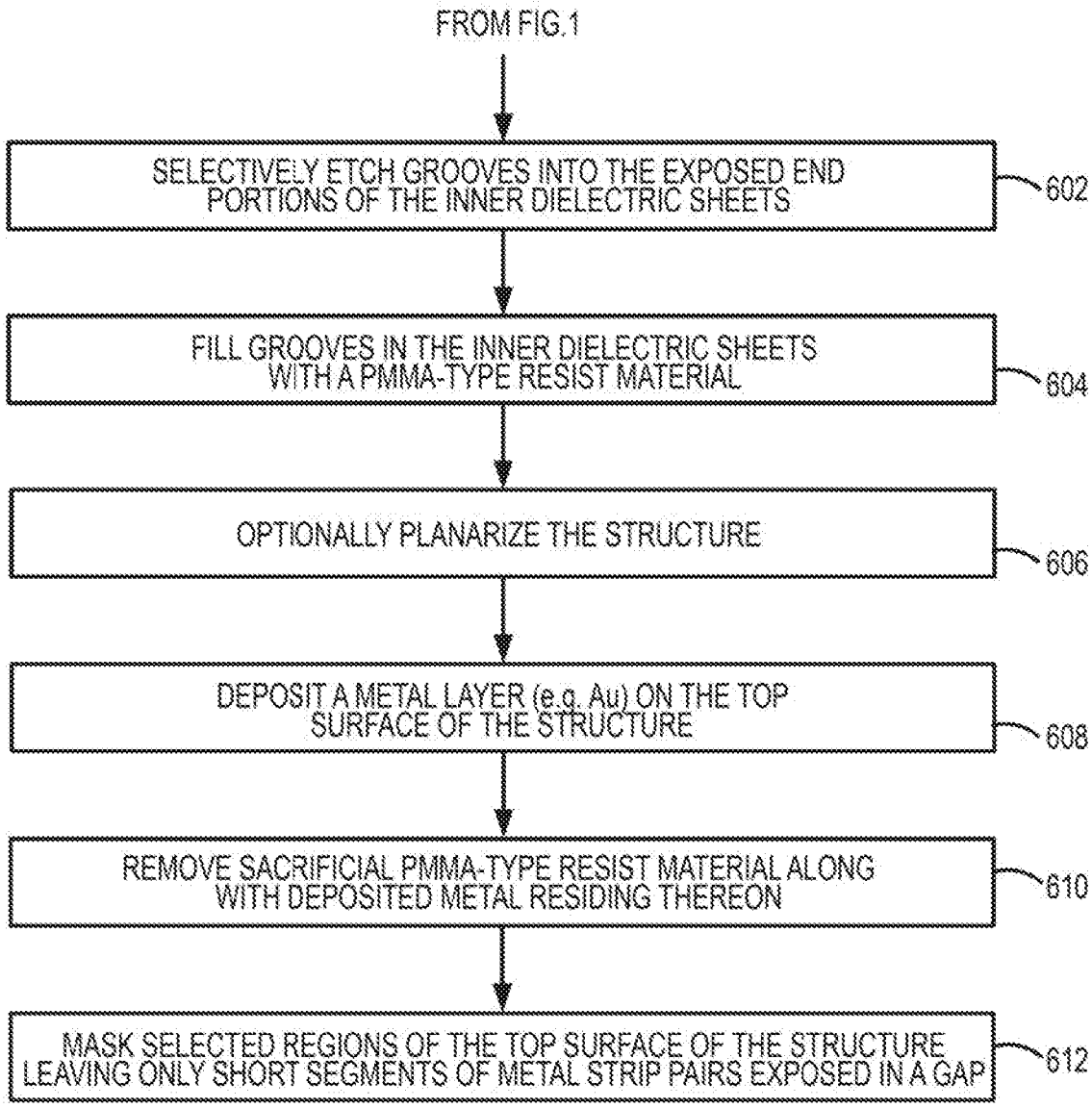

FROM FIG.1
SELECTIVELY ETCH GROOVES INTO THE EXPOSED END PORTIONS OF THE INNER DIELECTRIC SHEETS
602
FILL GROOVES IN THE INNER DIELECTRIC SHEETS WITH A PMMA-TYPE RESIST MATERIAL
604
OPTIONALLY PLANARIZE THE STRUCTURE
606
DEPOSIT A METAL LAYER (e.g. Au) ON THE TOP SURFACE OF THE STRUCTURE
608
REMOVE SACRIFICIAL PMMA-TYPE RESIST MATERIAL ALONG WITH DEPOSITED METAL RESIDING THEREON
610
MASK SELECTED REGIONS OF THE TOP SURFACE OF THE STRUCTURE LEAVING ONLY SHORT SEGMENTS OF METAL STRIP PAIRS EXPOSED IN A GAP
612

FIG.6

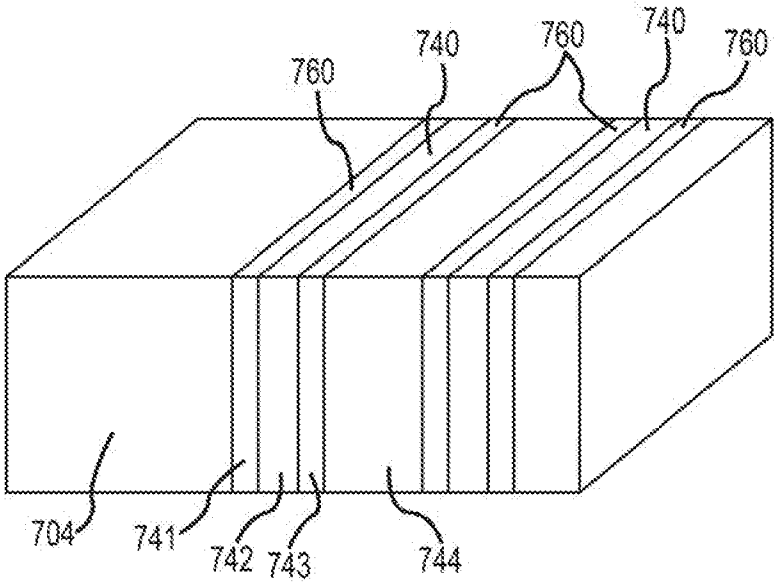
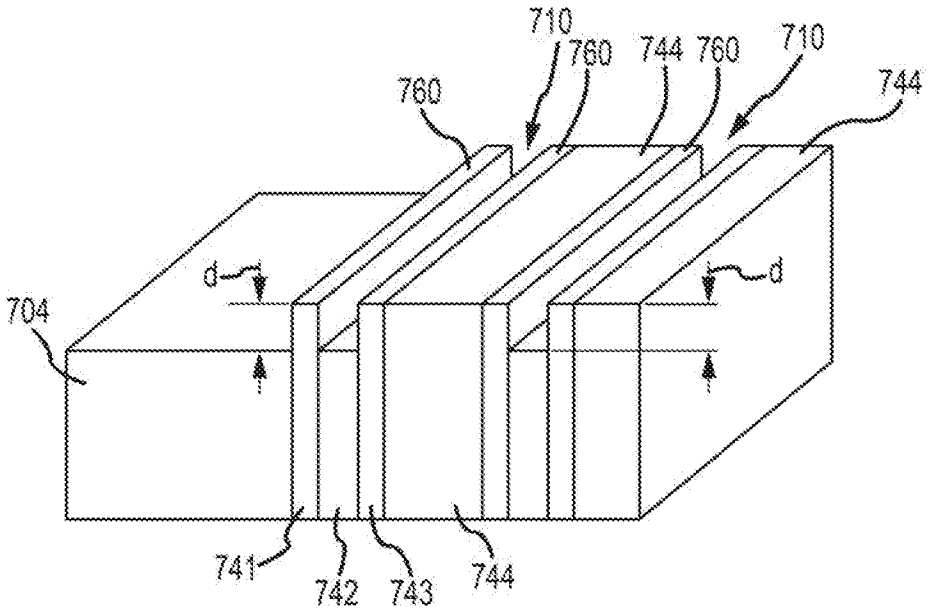

760
740
760
740
760
704
741
742
743
744

FIG.7A


710
760
744
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760
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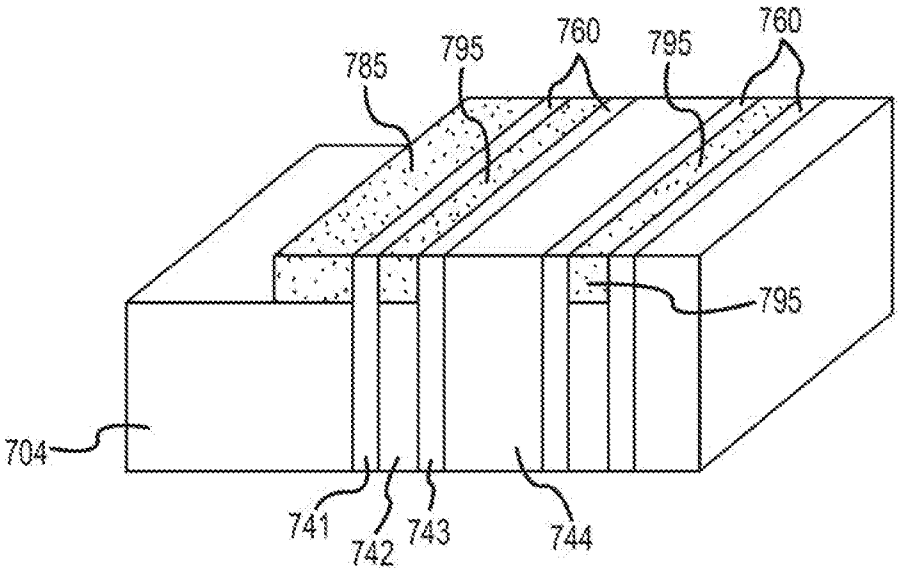
d
704
741
742
743
744

FIG.7B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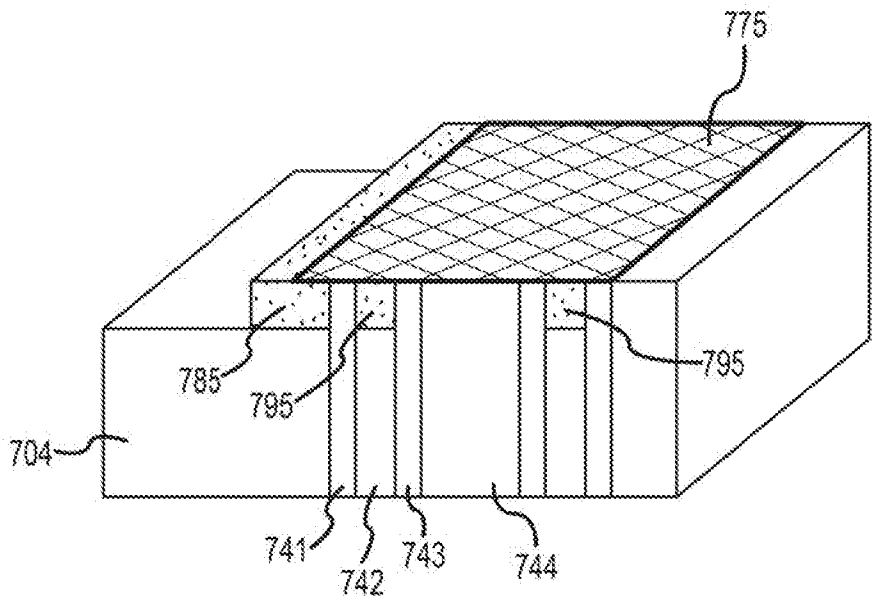
795
760
795
760
795
704
741
742
743
744

FIG7C


775
785
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744

FIG.7D

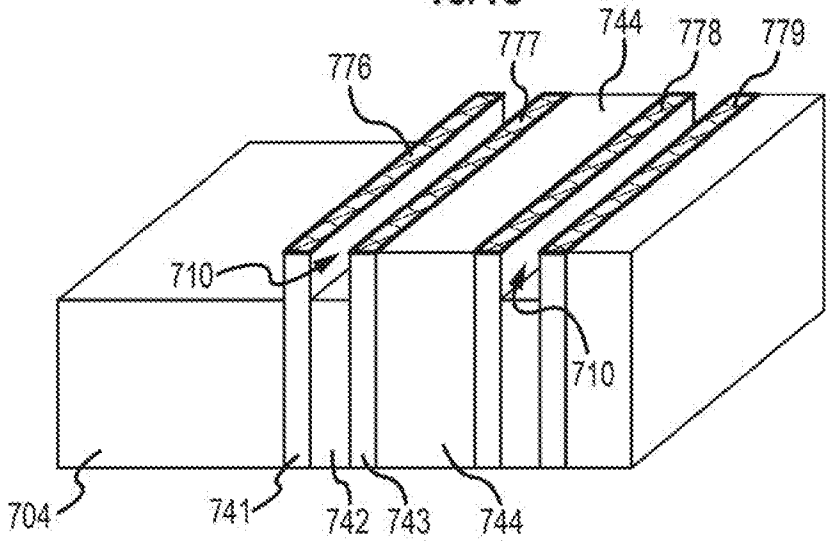
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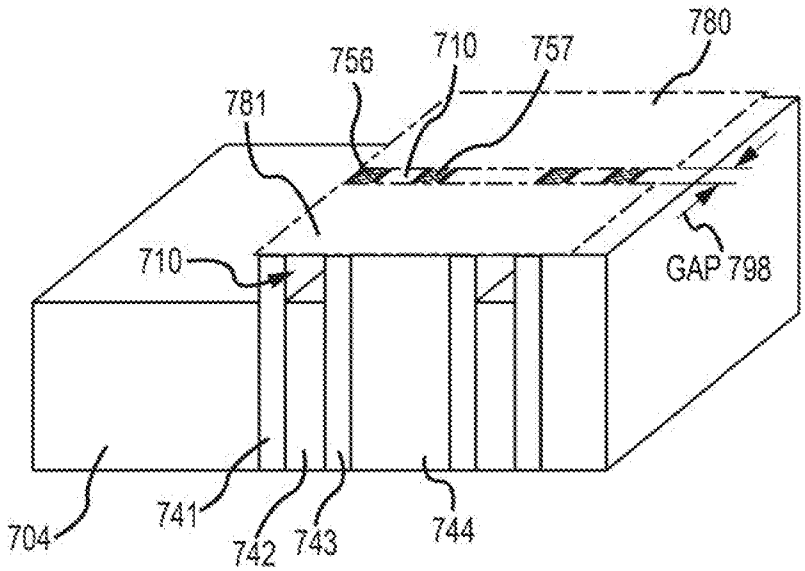
FIG.7E


780
756
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GAP 798
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742
743
744

FIG.7F

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2020/046792

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G01N 27/00; G01N 27/02; G01N 27/327 (2020.01)
CPC - G01N 27/00; B81B 2201/0214; B81B 2203/04 (2020.08)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
see Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
see Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
see Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2019/0194801 A1 (ROSWELL BIOTECHNOLOGIES, INC.) 27 June 2019 (27.06.2019) entire document	1-20
A	US 2014/0018262 A1 (REDA et al) 16 January 2014 (16.01.2014) entire document	1-20
A	US 2011/0223065 A1 (KIM et al) 15 September 2011 (15.09.2011) entire document	1-20
A	US 6,440,662 B1 (GERWEN et al) 27 August 2002 (27.08.2002) entire document	1-20
A	US 2019/0041355 A1 (ROSWELL BIOTECHNOLOGIES, INC.) 07 February 2019 (07.02.2019) entire document	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 October 2020	04 NOV 2020
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300	Authorized officer Blaine R. Copenheaver Telephone No. PCT Helpdesk: 571-272-4300