PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 :		(11) International Publication Number:
H04B 5/04, E05B 47/00	A1	WO 90/06024
		(43) International Publication Date: 31 May 1990 (31.05.90)

(21) International Application Number: PCT/AU89/00489

(22) International Filing Date: 16 November 1989 (16.11.89)

(30) Priority data:
PJ 1514 16 November 1988 (16.11.88) AU

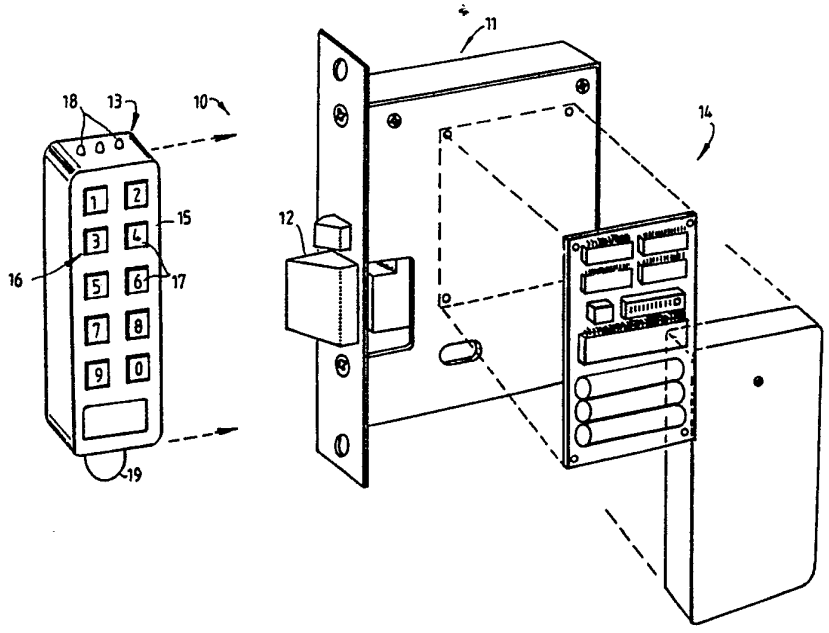
(71)(72) Applicant and Inventor: GUTH, Roland, Anton, Winston [AU/AU]; Lot 315, Ebling Court, Mudgeeraba, QLD 4213 (AU).

(74) Agent: GARDNER, John, R.,G.; P.O. Box 443, Mudgeeraba, QLD 4213 (AU).

(81) Designated States: AT (European patent), AU, BE (European patent), CH (European patent), DE (European patent), ES (European patent), FR (European patent), GB, IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent), US.

Published
With international search report.

(54) Title: A COMMUNICATION SYSTEM



(57) Abstract

A communication system (10) including a transmitting unit (13) and a receiving unit (14), the transmitting unit (13) having a keypad (16) and a signal generator (21) which generates signals for transmission as a coded message in accordance with actuation of particular keys (17) of the keypad (16). The receiving unit (14) includes a memory which stores a coded message and a comparator which compares the transmitted message with the stored message so that an output from the receiving unit (14) is generated when the stored message compares correctly with the transmitted message. In a second mode of the receiving unit (14), the memory can be reprogrammed with the message transmitted by the transmitting unit so that the transmitted message required to generate the receiving unit output can be varied. The output of the receiving unit (14) can be used to actuate a solenoid of a lock (11) or any other device.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	ES	Spain	MG	Madagascar
AU	Australia	FI	Finland	ML	Mali
BB	Barbados	FR	France	MR	Mauritania
BE	Belgium	GA	Gabon	MW	Malawi
BF	Burkina Fasso	GB	United Kingdom	NL	Netherlands
BG	Bulgaria	HU	Hungary	NO	Norway
BJ	Benin	IT	Italy	RO	Romania
BR	Brazil	JP	Japan	SD	Sudan
CA	Canada	KP	Democratic People's Republic of Korea	SE	Sweden
CF	Central African Republic			SN	Senegal
CG	Congo	KR	Republic of Korea	SU	Soviet Union
CH	Switzerland	LI	Liechtenstein	TD	Chad
CM	Cameroon	LK	Sri Lanka	TG	Togo
DE	Germany, Federal Republic of	LU	Luxembourg	US	United States of America
DK	Denmark	MC	Monaco		

A COMMUNICATION SYSTEM

Technical Field

This invention relates to a communication system and in particular to a system suited to the remote actuation of apparatus or a device. The system of the present invention is particularly suited to use in a security system for the control of locking devices such as a door locks of a building or vehicle, however, it may be readily adapted for use for the remote control of other devices such as for security lighting or other mechanisms.

Background Art

The increasing number of house burglaries has resulted in the need for improved locking systems for the doors and/or windows of buildings such as dwellings. Whilst a number of different types of deadlocks are available for use in conjunction with a normal door lock and whilst such deadlocks do have a deterrent effect, security provided by such systems is not absolute. Furthermore, keys for conventional locking systems are often lost necessitating in many cases the services of a locksmith to cut substitute keys. Similar theft problems are associated with vehicles and many different alarm and locking systems have been proposed to reduce the risks of theft. Again, however, whilst theft reduction is possible by using known procedures, theft of vehicles and/or their contents still is a common occurrence.

A number of remote control systems for locks for use with vehicles or with buildings are presently available and usually comprise a hand held transmitter which may be activated to send a signal to a receiver located adjacent a lock with the receiver on sensing of the signal causing the lock to open and/or close. An example of such a system is shown in U.S. Patent No. 4258352. In this system, however,

loss or theft of the transmitting unit can result in security problems as the locks may still be opened by an intruder using the transmitter.

Disclosure of the Invention

The present invention aims to overcome or alleviate the above disadvantages by providing a communication system which is particularly but not exclusively suited to the remote actuation of locking devices and which eliminates or substantially reduces risks associated with the loss of the transmitting unit of known systems. The system of the present invention also incorporates means which enable simple remote reprogramming with different control codes for actuation of the system so as to further increase the security of the system and to reduce the risks associated with loss or theft of the transmitting unit. The system of the invention also permits a large number of digits to be used in the control code in numerous different combinations.

The present invention accordingly in a first preferred aspect provides a communication system including transmitting means for transmitting a message in coded form and receiving means for receiving said transmitted coded message, said receiving means including memory means for storing a coded message, said receiving means being operative in a first mode to provide a first output when said transmitted coded message agrees with said coded message in said memory means and wherein said receiving means in a second mode is adapted to receive said transmitted coded message and reprogram said memory means with a coded message corresponding to said transmitted coded message whereby to permit variation of the transmitted coded message required to provide said first output from said receiving means.

Preferably the transmitting means includes signal generating means and a plurality of switch means corresponding to respective digits or parts of the coded

message to be transmitted and actuation of respective switch means causes the signal generating means to generate a corresponding coded signal. Preferably also the transmitting means includes infra-red light emitting means for emitting an infra-red light signal corresponding to the coded signal generated by the signal generating means and the receiving means includes infra-red light detecting mean for receiving the emitted infra-red light signal.

Preferably also, the receiving means includes means for identifying the last digit or part of the transmitted coded message and for producing said first output upon agreement between the last digits or parts of the transmitted coded message and stored coded message. Suitably the identifying means comprises the memory means, the memory means providing an output to cause actuation of the device subsequent to correct comparison between the last digits or parts of the transmitted and stored coded messages.

Suitably, the receiving means includes comparator means for comparing respective individual digits or parts of the stored coded message in turn with the corresponding digits or parts of the transmitted coded message in the first mode of the receiving means. The receiving means also preferably includes control pulse generating means for generating control pulses upon receipt of the transmitted coded message, the control pulses causing the coded digits or parts of the stored coded message at respective addresses in the memory means to be applied to the comparator means for comparison with corresponding coded digits or parts of the transmitted coded message.

The memory means also preferably includes a plurality of addresses at which respective coded digits or parts of the stored coded message are stored and there is suitably provided address setting means associated with the memory means, the address setting means being responsive to

the control pulse generating means to change the address of the memory means. In one form, the control pulse generating means includes means for generating respective first pulses upon receipt of respective coded digits or parts of the coded message by the receiving means, the first pulses causing said address setting means to change the address of the memory means. Preferably also the control pulse generating means is further operative to generate respective pairs of pulses upon receipt of respective coded digits or parts of the transmitted coded message by the receiving means, the pairs of pulses being operative to apply respective coded digits or parts of the coded message at respective addresses set by the address setting means to the comparator means. Suitably, the respective first pulses terminate between the pulses of the respective pairs of pulses whereby the leading pulse of the pair is operative to apply the coded digit or part at an address set by the address setting means to the comparator means and wherein the trailing pulse of the pair causes the coded digit or part at the subsequent address of the memory, set by the trailing edge of the first pulse clocking the address setting means, to be applied to the comparator means and wherein means are provided to suppress the comparison between the coded digit or part at the address set by the address setting means of the transmitted code and the coded digit or part of the stored coded message at the subsequent address.

Suitably in the second mode of the control means, respective coded digits or parts of the transmitted coded message are written into said the memory means at respective addresses set by the address setting means. In this mode, the address setting means is controlled by the control pulse generating means, the latter also being operative to cause a device actuating signal to be written into the memory means after receipt of the last coded digit or part of the

transmitted code.

In one preferred form, the coded message is a coded multi-digit number and the stored coded message is a stored coded number.

Brief Description of the Drawings

In order that the invention may be more readily understood and put into practical effect reference will now be made to the accompanying drawings which illustrate a preferred embodiment of the invention and wherein:-

Fig. 1 illustrates the system of the invention as applied to the control of a door lock;

Fig. 2 is a circuit diagram of the transmitting unit for the system of Fig. 1;

Fig. 3 is a circuit diagram of the receiver unit for receipt of control signals from the transmitting unit;

Fig. 4 is a circuit diagram of the comparing and actuating circuit of the system;

Fig. 5 is a timing diagram depicting the signals at points A,B,C,E, and F of the circuit of Fig.4 in the operational mode;

Fig. 6 is a timing diagram depicting the signals at points I and H of the circuit of Fig. 4 when an incorrect number is detected;

Fig. 7 is a timing diagram depicting the signal at data terminal (D5) of the memory during the programming mode;

Fig. 8 is a circuit diagram of the preferred power supply for the receiving and actuating circuit; and

Fig. 9 is a circuit diagram of a memory backup power supply.

Best Mode for Carrying Out the Invention

In the following description, the numerals and or letters shown in brackets indicate particular terminals of semi-conductor devices including integrated circuits used in the circuits. Referring firstly to Fig. 1 there is

illustrated a communication system 10 according to the present invention adapted for the control of a door lock 11 which may be associated with the door of any building such as a dwelling and which includes a solenoid actuated lock latch 12. The system 10 includes a hand held portable transmitting unit 13 and a receiving and actuating unit 14 which is fitted to the lock 11 and which is electrically connected to the lock solenoid so as to actuate same upon receipt of a predetermined coded signal from the transmitting unit 13.

The transmitting unit 13 includes a casing 15 which supports a key pad 16 provided with respective keys 17, bearing in this instance the numerals 1 to 0 and which are associated with respective switches which when actuated cause the transmitting unit 13 to generate and transmit various coded signals in accordance with selected keys 17 depressed. The casing 15 also supports a pair of infra-red light emitters 18 which are arranged to transmit an infra-red light beam encoded in accordance with the code signal generated by the particular key pad input. If desired the casing 15 may be provided with a key ring 19 so that conventional keys may be connected thereto.

As shown in the circuit diagram of the transmitting unit 13 of Fig. 2 the key pad switches 20 associated with the respective keys 17 are connected to a key pad scanner unit 21 in this instance an integrated circuit type UAA4000 which is adapted to generate different digital codes in accordance with the key pad switches 20 which are actuated by the manually actuable keys 17. The frequency of the pulse output of the scanner 21 and the pulse width of the pulses is controlled by the adjustable R-C circuit 22 so as to be variable if desired. The digital coded output from pin (2) of the scanner 21 is amplified in the Darlington pair amplifier circuit 23 with this circuit driving the infra-red light emitters 18 so that a modulated coded signal is

transmitted therefrom with each transmitted pulse comprising a burst of modulation.

The receiving circuit of the unit 14 as shown in Fig. 3 includes an infra-red receiving diode 24 which is adapted to receive the transmitted signal from the infra-red light emitters 18 of the transmitting unit 13 and this signal when received is filtered in the R-C filter circuit 25, amplified in the series transistor amplifier circuit 26 and passed to a pair of Schmitt trigger inverters 27 where the pulse signals are squared off. The signal output from the Schmitt triggers 27 is demodulated in the diode R-C circuit 28 to produce an output signal in pulse code modulated form to the comparator/actuator circuit of the unit 14.

The latter circuit as shown in Fig. 4 comprises a decoder 29 in this case an integrated circuit type UAA40009 which is matched to the keypad scanner integrated circuit 21 of the transmitting unit 13 and which is tuned to the frequency of the transmitting unit by means of the adjustable R-C circuit 30. The output of the receiver circuit 14 is applied to the input terminal (13) of the decoder 29 and also to a Schmitt inverter 31 which controls a transistor switch 32, the collector of which is connected to output pin (9) of the decoder 29, the pin (9) also being tied to the 12V supply rail of the circuit through a resistor R7. This circuit maintains the pin (9) "low" except in circumstances where a valid signal is received at the input terminal (13) at which stage the pin (9) is permitted to go "high".

The transistor switch 32 is also placed in series with a further transistor switch 33 which is controlled through a further Schmitt inverter 34 by the inverter 31 and which is operative to limit current drain of the circuit by ensuring that the decoder 29 is normally switched off and only draws current when a valid signal is received at its input pin (13). For this purpose, the connection point

between the emitter of the transistor 32 and collector of the transistor 33 is connected to the zero supply terminal (5) of the decoder 29.

Thus in conditions of no signal input from the receiving circuit, the output of the inverter 31 is high causing the transistor switch 32 to be turned ON and the pin (9) of the decoder to be pulled low. The high output from the inverter 31 applied to the input of the inverter 34 results in a low output from this inverter causing the transistor switch 33 to be maintained in an OFF state so that the decoder supply terminal (5) is high. When a valid signal is received and applied to the terminal (13) of the decoder 29, that signal will provide a low output from the inverter 31 causing the transistor switch 32 to be turned OFF thus permitting the decoder pin (9) to go high. The low output of the inverter 31 results in a high output of the inverter 34 so that the transistor switch 33 is turned ON thus pulling its collector low so that the decoder pin (5) is pulled to zero voltage and the decoder 29 thus turned ON. The high state of pin (9) and thus at point A which is connected through resistor (R8) to pin (9) will remain as long as the finger of the user is maintained on one of the keypad keys 17.

The decoder 29 converts the incoming signal at terminal (13) into decimal form and this decimal signal is converted into binary form by a binary converter 35 which in this instance is an integrated circuit type 74HC147. The output from the binary converter 35 is in binary coded form on the four output lines 36 which are connected to one set of inputs terminals (11,1,9,14) of a comparator 37 in this instance a type 74C85. The other set of comparator input terminals (10,7,2,15) are connected to data output terminals (D1-D4) of a memory 38 in this case a type 6816 2K x 8 bit CMOS integrated circuit which stores the coded number, the

input of which into the keypad 16 will result in actuation of the lock solenoid. Respective resistors R1, R2, R3 and R4 are connected across the corresponding input terminals of the comparator 37 for a purpose which will hereinafter become apparent. The coded number stored in the memory 38 is applied via the data output terminals (D1-D4) to the comparator inputs (10,7,2,15) under the control of a control circuit 39 and counter 40 which is connected to the address terminals (A0-A4) of the memory 38.

The control circuit 39 derives a control signal from the point A where as stated above a signal occurs at any time when a valid signal is applied to decoder terminal (13) and for as long as one of the transmitter key pad keys 17 remains depressed. This point A is connected to a Schmitt inverter 41 which is connected through a R-C timing circuit 42 to a further inverter 43 which is in series with two further identical inverter/R-C circuits 44 and 45. A further similar inverter/R-C circuit 46 is connected to the output of the inverter 41, the circuit 46 being connected to the clock terminal (CLK) of the counter 40 and providing at point B a pulse for incrementing or clocking the counter 40. As shown also, the outputs of the inverter 43 at point C and circuit 45 at point E are interconnected through a connecting line 47 so as to provide at the point F a control signal comprising the summation of the signals at points C and E. The R-C circuits of each inverter circuit 42, 44, 45 and 46 determine the length of the pulse signal as well as the time delay between the pulses at points B, C, and E as described more clearly below.

The point F is connected to the two inputs of a NAND gate 48 which has its output connected to the chip select terminal (S) of the memory 38 for causing the application of the stored digits in the memory to the data output terminals (D1-D4) of the memory 38. The point F is

also connected to one of the inputs of a further NAND gate 49 which is connected to the write terminal (W) of the memory 38. The other terminal of the gate 49 is connected to a manually actuable switch 50 connected to a positive rail, the switch 50 being used for programming the memory 38 in the manner described below.

A further line 51 connects the output of the inverter circuit 45 at point E, to the output of the comparator 37 at point I which through further series Schmitt inverter R-C circuits 52 and 53 and Schmitt inverter 54 is connected to the reset terminal (MR) of the counter 40. The R-C circuit R20/C10 of the circuit 52 filters out any spikes or other spurious signals at the point I whilst the circuit R31/C16 lengthens the reset pulse to be applied via the inverter 54 the reset terminal (MR) of the counter 40 so that the reset pulse is longer than the clock pulse provided at B.

A further clock reset line 55 is connected from the output of the inverter 41 to the input of a further Schmitt inverter 56, the output of which is also connected to the input of the inverter 54. The R-C circuit R16/C7 across the input of the inverter 56 is arranged so that for no signal input to the decoder 29, the capacitor C7 is charged up to hold through the inverters 54 and 56 the master reset terminal (MR) of the counter 40 high and thus the counter 40 reset. When a signal is received however, the output of the inverter 41 goes low so that the capacitor C7 discharges thus causing the reset signal to be removed thereby permitting the counter 40 to count. At the end of signal transmission, the capacitor C7 will again charge up to reset the counter 40. The time constant of the R16/C7 circuit is chosen so that if excessive delay occurs before entering respective numbers of the code into the keypad, the capacitor C7 will charge up to reset the counter so as to necessitate recommencement of the code input. This time constant in the present embodiment is

2.2 seconds however, this time may be varied simply by changing the capacitance of the capacitor C7 or resistance of the resistor R16.

A further data output terminal (D5) of the memory 38 is connected to one input of a NAND gate 57 and the memory 38 is programmed in the manner described below to give a low output at terminal (D5) for all numbers of the code punched into the keypad 16 other than the final number so that the final number of the code can be sensed to cause lock solenoid actuation. The other input of the NAND gate 57 is connected to the output E of the inverter circuit 45. The output of the gate 57 is connected to the input of a Schmitt inverter 58 across which is connected a series R/C circuit, R24/C11 which determines the opening time of the lock solenoid. The output of the inverter 58 is connected to the base of a Darlington pair drive transistor 59 which has its collector circuit connected to the lock solenoid. A further NAND gate 60 has its inputs paralleled and connected to the clock terminal (CLK) of the counter 40 and its output connected to the memory data output terminal (D5) so that the latter is tied to the clock input. A diode D33 is connected between the input of the inverter 58 and the switch 50 so as to prevent solenoid actuation in the program mode.

In use and assuming that a coded multi digit number to actuate the lock solenoid is stored in the memory 38, actuation of one of the transmitter keypad keys 17 will cause a corresponding digital coded signal to be generated and transmitted from the infra-red light emitters 18. If the emitters 18 are directed towards the sensing infra-red diode 24 of the receiving unit 14, the emitted signal will be sensed, amplified, squared off and demodulated in the circuit of Fig. 2 as described above before passing to the terminal (13) of the decoder 29. At the same time, this "high" signal will be applied to the inverter 31 to cause the transistor 32

to be switched off thus permitting the terminal (9) of the decoder to go high. The transistor 33 is also turned on via the inverter 34 thus pulling the terminal (5) to earth so that current is supplied to the decoder 29. The decoder 29 will thus function to convert the coded input signal at terminal (13) into decimal form. The decimal form of the signal is converted into binary form by the converter 35 which applies same to the input terminals (11,1,9,14) of the comparator 37 through the lines 36.

As shown in the timing diagram of Fig. 5, the signal appearing at A consequent upon signal input at consequent upon signal input at terminal 13 will comprise a long pulse of a duration corresponding substantially to the time that the selected transmitter keypad key 16 is maintained depressed. The signal appearing at points B and C will commence at the same time however the length of the pulse at C will be shorter than that at B due to the differing time constants of the R-C networks of the respective inverter circuits 42 and 46. In each case a "low: signal at the output of the respective inverters of the circuits 42 and 46 permits the series capacitors C3 and CN in the R-C circuits to charge up at a rate depending upon their capacitance and the resistor of their associated resistors R10 and R11. In this case, the capacitors C3 and CN have the same capacitance, however, the resistor R11 associated with the inverter circuit 46 has a higher resistance than that of the resistor R10 of the circuit 42 so that the capacitor C 3 takes a longer time to charge than the capacitor CN. When, however, the respective capacitors have charged up, the inputs to the inverters go "high" and the output of the inverter circuits 43 and 46 at B and C respectively will go "low" thus terminating the output pulses from the respective inverter circuits 42 and 46.

The pulse output at point C is applied to the two

further R-C inverter circuits 44 and 45 which function in a manner similar to the above to provide a delayed pulse output at the point E as shown in Fig. 5. As stated above, the pulse outputs at the points C and E are summed through the connecting line 47 to provide a double pulse signal at point F. As shown, however, the timing is such that the pulse at point B terminates in the time span between the pulses appearing at point F. Furthermore the trailing edge of the pulse at B causes clocking of the counter 40 when its master reset terminal (MR) is low to change the address of the memory 38.

The first pulse at the point F causes through the NAND gate 48 the first coded number stored in the memory 38 at the first address initially set by the address counter 40 to be applied via the data output lines (D1-D4) to the other inputs (10,7,2,15) of the comparator 37 and if the coded numbers at the respective comparator inputs match, the comparator 37 provides a high output at point I. Between the next pulse at terminal F, the counter 40 is clocked by the trailing edge of the pulse at point B to set the next address of the memory 38 and the next pulse of the pair of pulses at terminal F causes the coded number at that address to be applied to the terminals (D1-D4) and thus to the comparator 37. This coded number, however, will not normally match the coded number applied to the other inputs of the comparator 37 via the decoder 29 unless the first and second numbers of the code are the same. If the numbers are not the same, the output of the comparator 37 at point I will try to go low. However, at the same time, the line 51 applies the pulse signal at E to the point I so that point I will be prevented from going low. Thus in effect, the comparison provided by the comparator 37 is suppressed. This will also occur if it happens that the second number is the same as the first with the signal at E overriding the comparison. Appearance of a

"high" at I will maintain through the respective inverter circuits 52, 53 and 54 the reset terminal (MR) of the counter 40 "low" so that the counter 40 can continue to count upwardly and change the addresses of the memory 38 upon receipt of clock signals from the point B.

This procedure continues for each number keyed into the keypad up to the last number. For the last number keyed into the key pad, the first pulse of the pair of pulses at point F will cause comparison between the numbers as above. The next clock pulse at B will cause the counter 40 to set the next address which comprises the address after the address of the final number of the code. The next pulse of the pair at F will cause the memory 38 to apply a high output at the terminal D5. This high is applied to the NAND gate 57 and at the same time, the high at point E is applied to the gate 57 so that a low output appears at the output of the gate 57. This low causes the previously charged capacitor C11 to discharge so that the output of the inverter 58 will go high and the Darlington pair transistor 59 to switch on and thus cause actuation of the solenoid and the lock to open. After the key 17 corresponding to the last number of the code is released, the pin (9) of the decoder 29 will again go low as no signal is at the input terminal (13). This low causes through the inverter 41, line 55, and inverters 56 and 54, a high to be applied to the master reset (MR) terminal of the counter 40 so that the counter is reset to the first address of the memory 38.

In the event that an incorrect number is keyed into the transmitter key pad, the comparator 37 at the first pulse of the pulse pair at point F will provide a low output at point I due to incorrect comparison between the stored number and the keyed in number. In this case, however, the output at I is not suppressed as no signal is applied at this time through the line 51 from the point E as will be apparent from

the timing diagram of Fig. 5. This low signal will cause at the reset terminal (MR) of the counter 40 via the inverters 52, 53 and 54, a high signal so that the counter 40 will be reset and the address of the memory 38 to be changed back to the original set address necessitating recommencement of the correct code input. If as stated above, the keys are not pressed in the correct sequence and within a certain time between key depressions, the R/C circuit R16/C7 will also reset the counter 40.

Where it is desired to reprogram the memory 38 with a different coded number or multi-digit coded number, the program switch 50 which is preferably key actuated is operated to apply a high to one of the terminals of the inverter 49 which is connected to the memory write line (W). The numbers of the code are then simply keyed into the transmitter keypad 16 sequentially whilst the transmitter is directed towards the infra-red receiving diode 24. Each key of the keypad which is depressed corresponding to a particular number will result in a corresponding digital coded signal to be transmitted by the transmitter, received by the receiving unit and applied to the decoder 29 and via the converter 35, the resistors, R1 to R4, which are connected across corresponding pairs of input terminals of the comparator 37 so as to bypass same, to the data terminals (D1-D4) of the memory 38. As with the operational mode, pairs of pulses are generated at the point F with the first pulse causing a low to appear at the select terminal (S) and write terminal (W) of the memory 38 and the coded number appearing at the data terminals (D1-D4) to be read into the memory 38 at the first address set by the counter 40. The trailing edge of the pulse at point B will then clock the counter 40 so as to cause the address of the memory to be changed. The second pulse of the pair at point F then causes the preceding number to be written into the next address as

set by the counter 40. For the next keypad input, the address stays the same and the previously written in number is overwritten by the number keyed into the keypad and appearing at the data terminals (D1-D4) of the memory 38. The above procedure is continued for each number or digit of the code.

At the same time, the respective pulses of each pulse pair appearing at the point F cause corresponding lows and highs to be written into the data output terminal (D5). As will be apparent from the timing diagram of Figs. 6 and 8, the first pulse at F applied to the write terminal (W) causes the signal at terminal (D5) to be written into the first address in the memory 38, this signal being an inverse of the clock pulse at B inverted by the inverter 60. The trailing edge of the pulse at B clocks the counter 40 to the next address and the next pulse at F causes the signal at (D5) which is now a high being an inverse of the signal at B to be written into that next address. The first pulse of the next pair at F again causes the (low) signal at terminal D5 to be written into the previously set address overwriting the high written in by the last pulse of the previous pair. This procedure continues so that a series of lows are written into the address for (D5) except for the last set of F pulses corresponding to the last number in the code where the last pulse of the pair maintains a high in the last address plus one.

Referring now to Fig. 8 there is illustrated a power supply 61 for the receiving/actuating unit and lock actuating solenoid. The supply 61 includes a lead acid battery 62 and charging circuit 63 including a bridge rectifier 64 and a silicon controlled rectifier (SCR) 65 which has its anode/cathode terminals arranged in series with the battery 62 with its gate receiving a fixed bias through the biasing circuit 66 comprising the diode D28, resistor

R25, zener diode ZD1 and diode D29 which are connected across the rectifier 64. A current limiting resistor R26 is arranged in parallel across the anode and cathode of the rectifier 65. In normal conditions, the circuit acts as a trickle charger of the battery 62 via the resistor R26 with the SCR 65 turned off due to the fact that the gate terminal of the SCR 65 is maintained high by the biasing circuit 66. If the voltage of the battery 62 falls due to loss of charge, the potential difference between the gate and cathode of the SCR 65 will fall until the SCR 65 is switched on so that full current is applied from the rectifier 64 to the battery 62 to allow rapid charging thereof and the resistor R26 is bypassed. When the battery 62 is again charged up, the potential difference between the gate and cathode of the SCR 65 falls so that the SCR 65 will again be switched off and trickle charging through the resistor R26 recommenced.

As shown, the supply 61 supplies 12 volts to the solenoid as well as to the receiving circuit 14 where required and a voltage regulator 67 also supplies a regulated 5 volts to the circuit 14. Alternatively, the regulator 67 may be replaced by a resistor/zener diode to reduce current drain of the circuit.

Fig. 9 is a circuit diagram of a backup power supply 68 for the memory 38 which provides supply to the memory 38 so that the coded number in the memory is retained in the event of loss of power. In this arrangement, the pins (22,23,1,2,3,12,19, and 20) of the memory 38 are connected to the collector of a transistor switch 69 which is also connected via a capacitor C15 to the 5 volt power supply rail. The base of this transistor is also connected to the volt rail via a resistor R28 and indicating light emitting diodes (LED1, LED2). In normal operating conditions, the transistor 68 is turned on via the resistor (R28) so that the capacitor (C15) becomes fully charged and the connected zero

pins pulled to 0 volts. In the event of loss of power for example where the battery 62 is removed, the transistor 68 is turned off as bias is removed form the base circuit. The charge on the capacitor is available to pull the normally zero pins of the memory 38 below 0 volts so that the memory 38 will receive supply for a time until the capacitor C15 discharges thereby ensuring that the coded number remains stored in memory 38.

Whilst the remote actuating system of the invention is particularly suited to use for the remote actuation of locks, for example vehicle locks, or household locks it may also be readily applied to use with window locks, gates or any other remote controlled device. For example, the system may be used to control the solenoid or solenoids of a security lighting system or alternatively be used for the remote control of electronic equipment such as computers, video recorder, or televisions by only allowing access thereto upon insertion of the particular code into the keyboard. The system of the invention may be readily applied to electronic funds transfer systems with maximum security or to other systems which require insertion of a personal code to enable operation of a device such as a funds withdrawal device such as those associated with banks.

Whilst the above system uses as a transmission media, infra-red waves, it will be readily apparent that other forms of transmission media may be employed such as micro-waves or ultrasonics.

When applied to a locking system for doors of a dwelling or building, the receiver and actuating unit may be mounted within a door adjacent to the lock or alternatively, the receiver may be mounted in a fixed position adjacent the door lock or striker plate and hard wired to the actuating unit which may be disposed adjacent the lock solenoid. The system of course may also be applied to striker lock devices

and in this arrangement, the receiver and actuating unit may be mounted in a wall adjacent to the striker plate.

Whilst the system described above uses transmitted and stored message comprising a series of numbers, it will be readily apparent that the message may comprise a series of letters which for example may form words or any other indicia which may be represented on the keypad.

CLAIMS

1. A communication system including transmitting means for transmitting a message in coded form and receiving means for receiving said transmitted coded message, said receiving means including memory means for storing a coded message, said receiving means being operative in a first mode to provide a first output when said transmitted coded message agrees with said coded message stored in said memory means and wherein said receiving means in a second mode is adapted to receive said transmitted coded message and reprogram said memory means with a coded message corresponding to said transmitted coded message whereby to permit variation of the transmitted coded message required to provide said first output from said receiving means.

2. A system according to claim 1 wherein said transmitting means includes signal generating means and a plurality of switch means corresponding to respective parts of said coded message to be transmitted and wherein actuation of respective said switch means causes said signal generating means to generate a coded signal corresponding to a part of said coded message.

3. A system according to claim 2 wherein said transmitting means includes infra-red light emitting means for emitting an infra-red light signal corresponding to said coded signal generated by said signal generating means and wherein said receiving means includes infra-red light detecting mean for receiving said emitted infra-red light signal.

4. A system according to claim 1 wherein said receiving means in said second mode includes means for identifying the last part of said transmitted coded message and for generating said first output upon agreement between said last

parts of said transmitted coded message and stored coded message.

5. A system according to claim 4 wherein said identifying means comprises said memory means, said memory means providing said first output subsequent to correct comparison between said last parts of said messages.

6. A system according to claim 1 and including comparator means for comparing respective parts of said stored coded message in turn with the corresponding parts of said transmitted coded message in said first mode of said receiving means.

7. A system according to claim 6 wherein said receiving means includes means for preventing continued comparison between said parts of said transmitted coded message and stored coded message in the event of no agreement between the previously compared parts of said messages.

8. A system according to claim 7 wherein said receiving means includes control pulse generating means for generating control pulses upon receipt of said transmitted coded message, said control pulses causing the parts of said stored coded message at respective addresses in said memory means to be applied to said comparator means for comparison with corresponding parts of said transmitted coded message.

9. A system according to claim 8 wherein said memory means includes a plurality of addresses at which respective parts of said stored coded message are stored and there being provided address setting means associated with said memory means, said address setting means being responsive to said control pulse generating means to change the address of said

memory means.

10. A system according to claim 9 wherein said control pulse generating means includes means for generating respective first pulses upon receipt of respective parts of said transmitted coded message by said receiving means, said first pulses causing said address setting means to change the address of said memory means.

11. A system according to claim 10 wherein said control pulse generating means is further operative to generate respective pairs of pulses upon receipt of respective parts of said transmitted coded message by said receiving means, said pairs of pulses being operative to apply respective parts of said stored coded message at respective addresses as set by said address setting means to said comparator means.

12. A system according to claim 11 wherein said respective first pulses occur between said pulses of said respective pairs of pulses whereby the leading pulse of said pair is operative to apply the message part at an address set by said address setting means to said comparator means and wherein the trailing pulse of said pair causes the message part at the subsequent address of said memory set by said address setting means consequent upon receipt of a said first pulse to be applied to said comparator means and wherein means are provided to override the comparison between said part of said transmitted coded message and the part of said stored coded message at said subsequent address.

13. A system according to claim 9 wherein in said second mode of said receiving means, respective parts of said transmitted coded message are written into said memory means at respective addresses set by said address setting means.

14. A system according to claim 13 wherein said address setting means is controlled by said control pulse generating means to set the addresses of said memory means for respective said parts of said transmitted coded message, said control pulse generating means further being operative to cause an output message to be written into said memory means after receipt of the last part of the transmitted coded message, said output message comprising said first output.

15. A system according to claim 1 wherein said receiving means is connected to a device to be actuated and wherein said device is actuated when said first output is generated by said receiving means consequent upon agreement between said transmitted coded message and stored coded message.

16. A system according to claim 15 wherein said device comprises a solenoid actuated lock and wherein said first output is operative to cause actuation of said lock solenoid.

17. A system according to claim 1 wherein said message comprises a multi-digit number and wherein said parts of said message comprise digits of said multi-digit number.

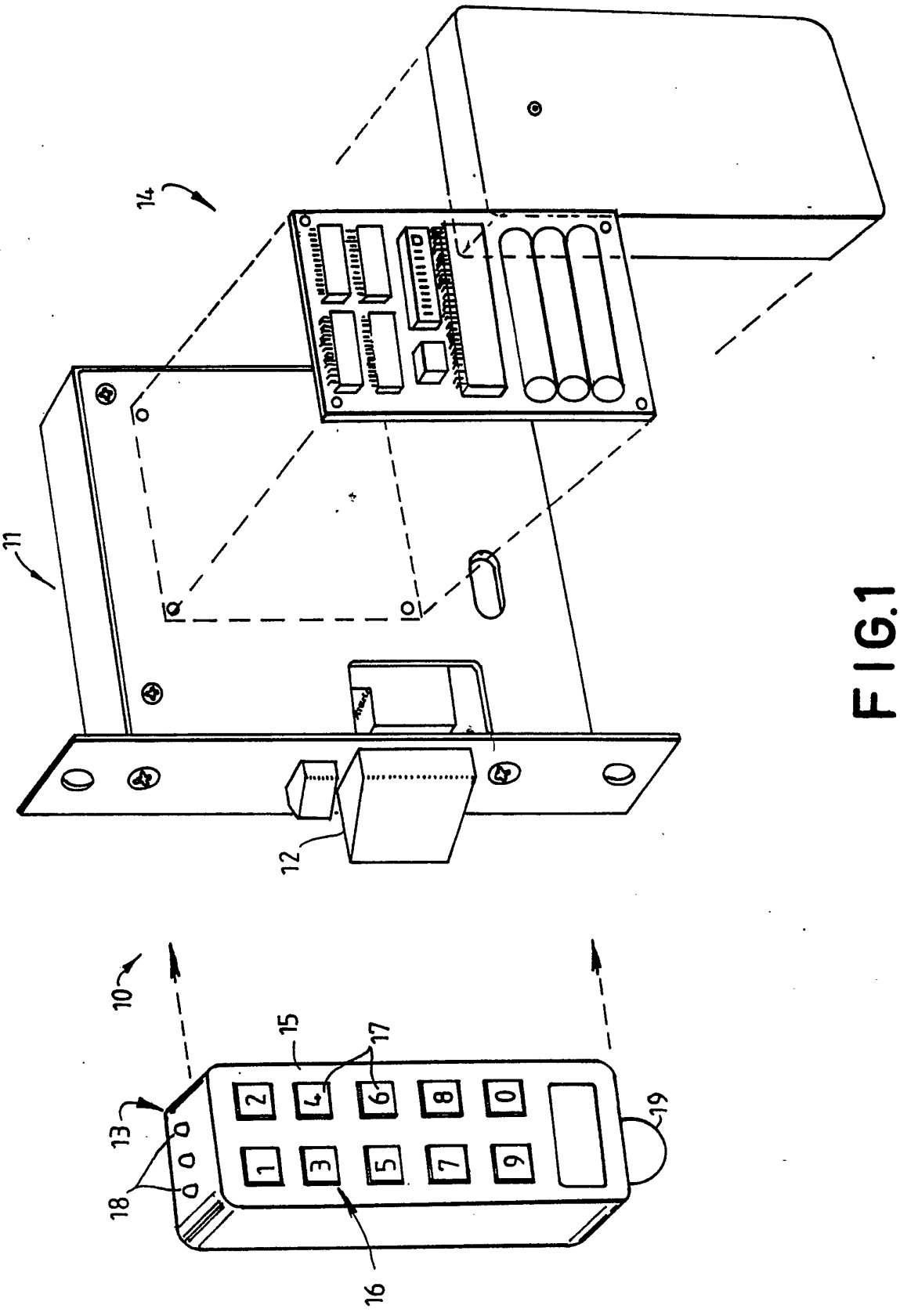
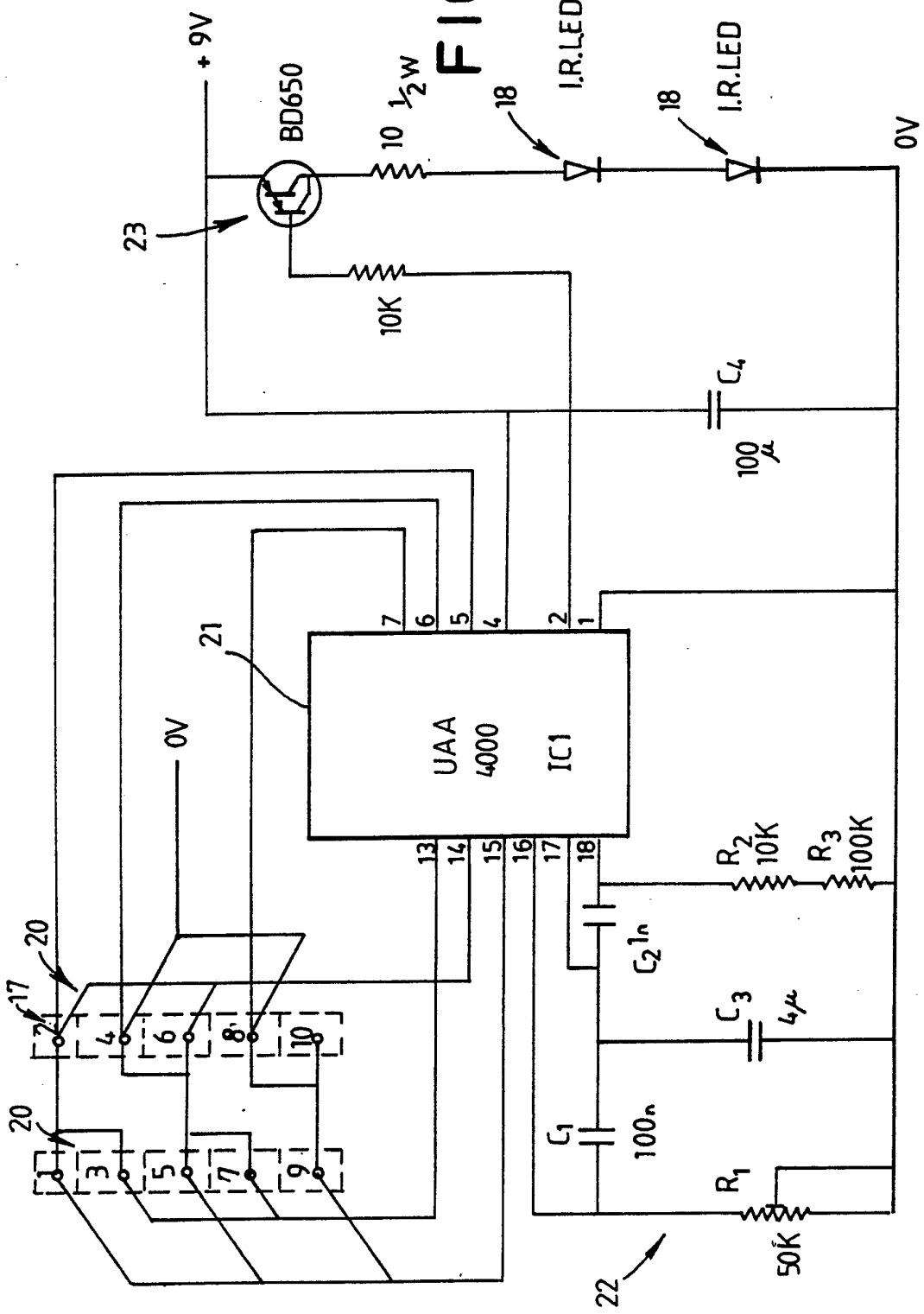


FIG.1

FIG.2



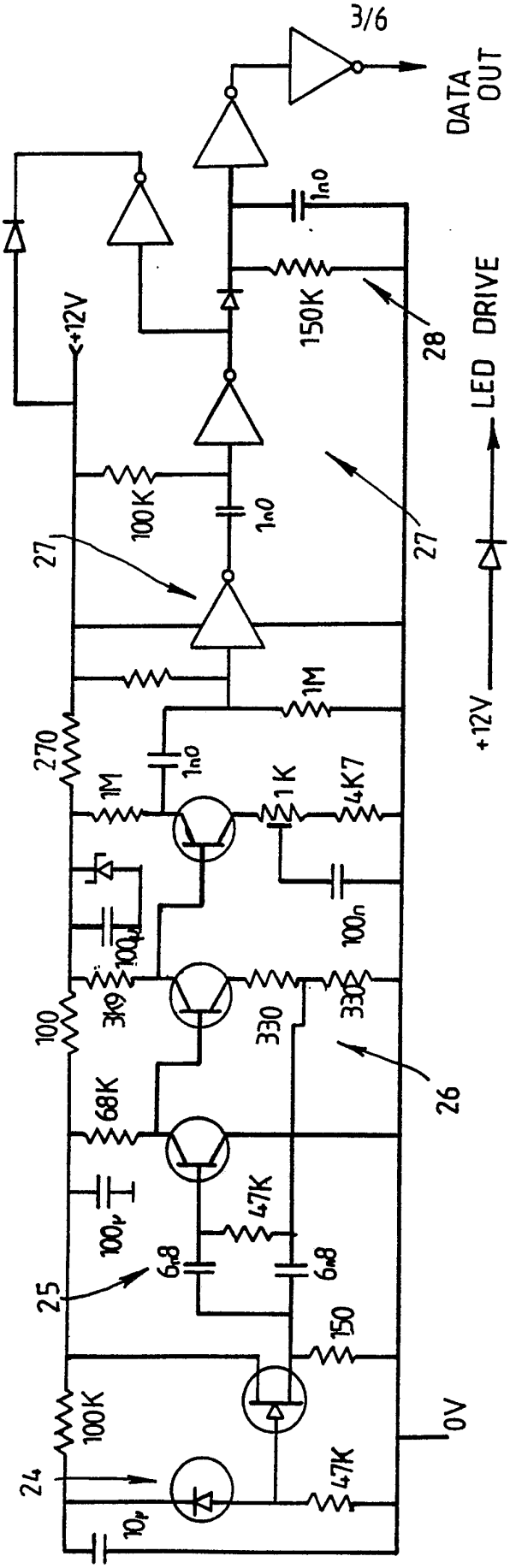

DATA OUT
1n0
150K
28
+12V
LED DRIVE
100K
1n0
27
27
1M
270
1M
1n0
1K
4K7
100n
100µ
100
330
330
330
68K
26
47K
100µ
6n8
6n8
25
150
100K
24
47K
10µ
0V

FIG.3

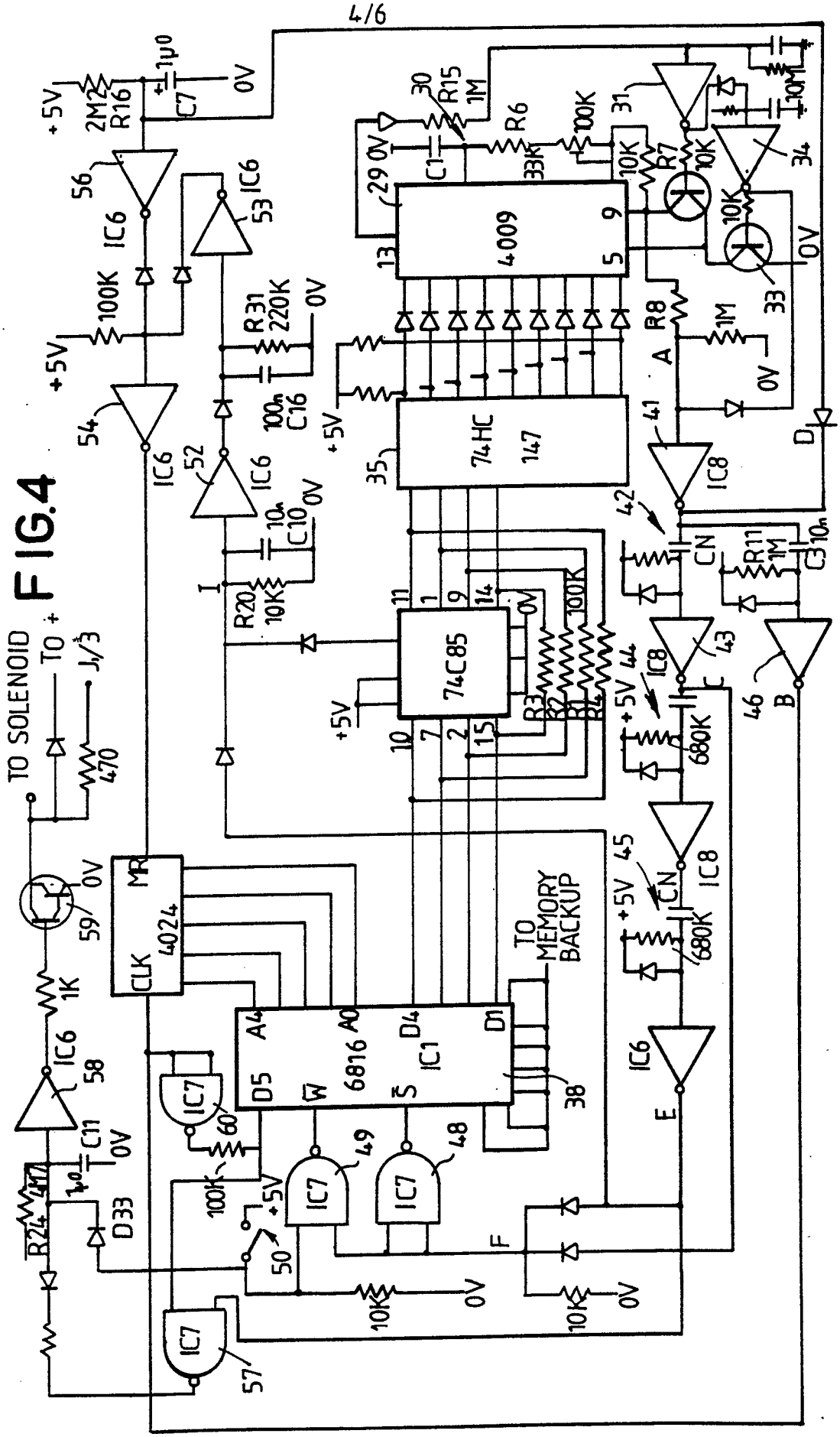

TO SOLENOID
TO +
J1/3
470
+5V
2M2
R16
1µ0
C7
0V
56
IC6
53
100K
R31
220K
54
52
100n
C16
10n
C10
R20
10K
59
MR
4024
CLK
1K
58
C11
R24
47K
D33
IC7
60
100K
50
49
48
A4
A0
D4
D1
D5
W
S
6816
IC1
38
TO MEMORY BACKUP
29
C1
30
R15
1M
R6
33K
100K
31
10K
R7
34
4009
13
9
5
33
R8
1M
A
41
D1
IC8
35
74HC
147
42
CN
R11
C3
43
74C85
11
1
9
14
10
7
2
15
R3
R2
R1
R4
44
680K
46
B
45
E
F
10K
57

FIG.4

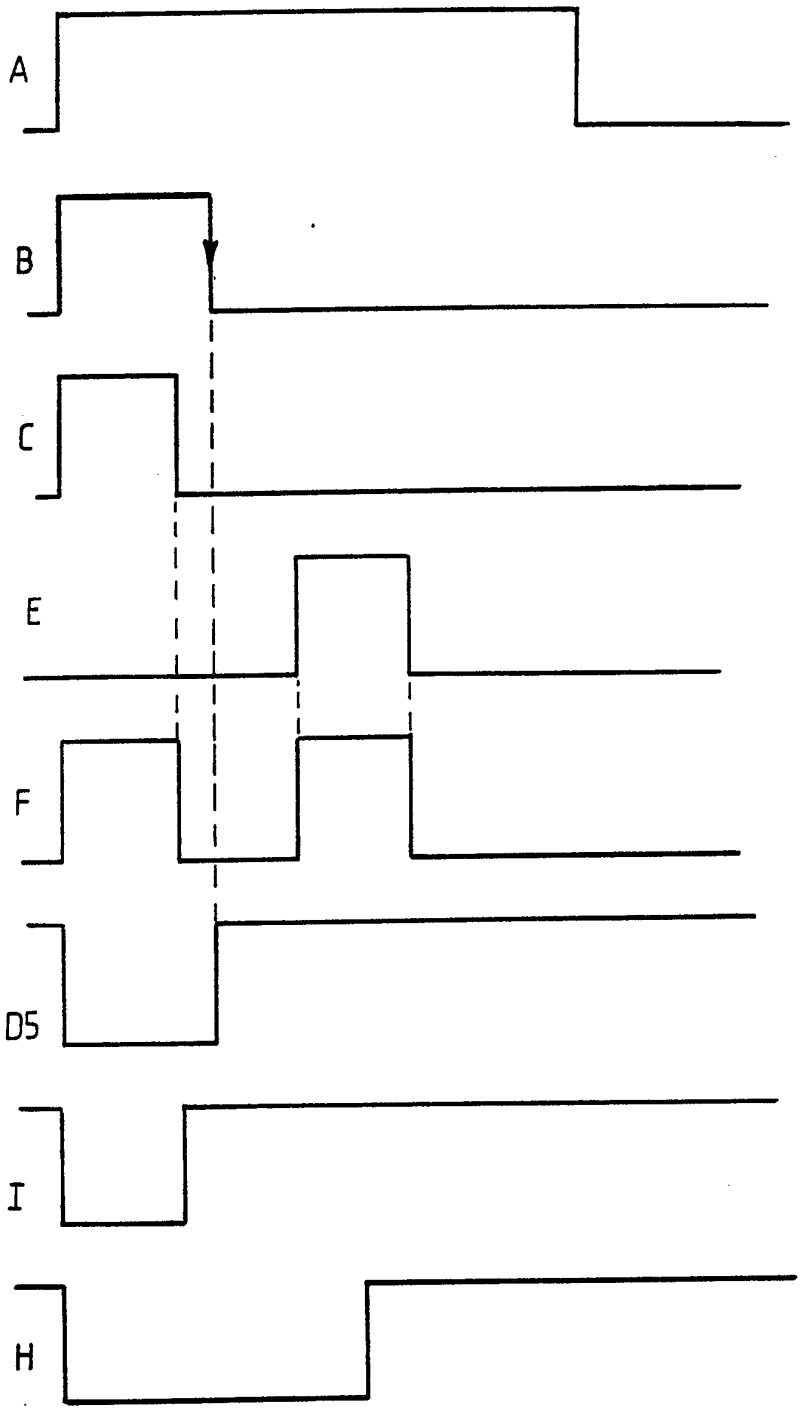


FIG.5

FIG.6

FIG.7

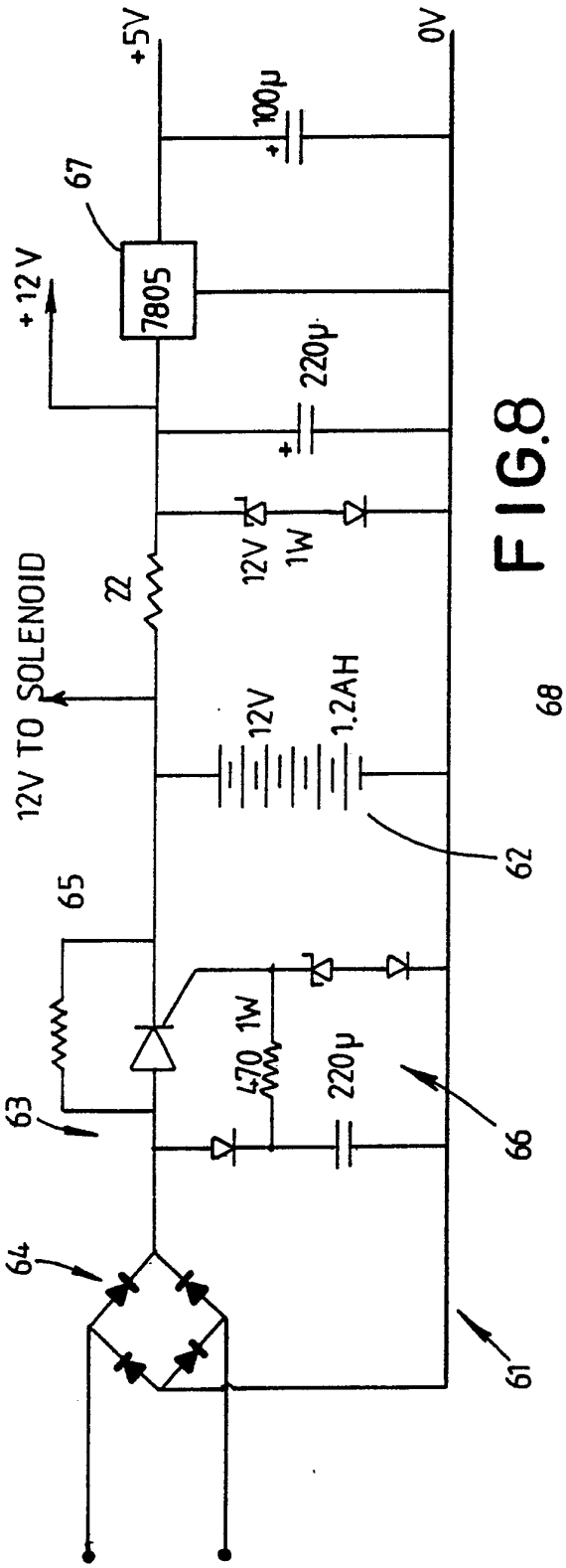

+5V
0V
100µ
67
7805
+12V
220µ
12V 1W
22
12V TO SOLENOID
12V
1.2AH
62
65
470 1W
220µ
66
63
64
61

FIG.8

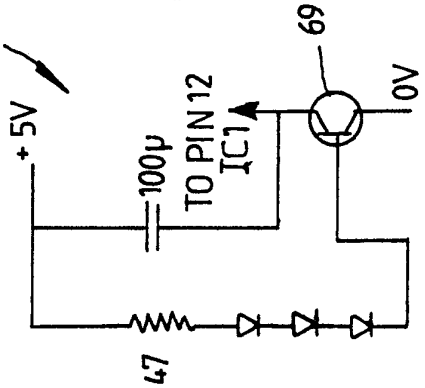

68
+5V
100µ
TO PIN 12 IC1
69
0V
47

FIG.9

INTERNATIONAL SEARCH REPORT

International Application No. PCT/AU 89/00489

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) 6

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl.[4] H04B 5/04, E05B 47/00

II. FIELDS SEARCHED

Minimum Documentation Searched 7

Classification System	Classification Symbols
IPC	H04B 5/04, E05B 47/00

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched 8

AU : IPC as above, Australian Classification 05.50

III. DOCUMENTS CONSIDERED TO BE RELEVANT 9

Category*	Citation of Document, [11] with indication, where appropriate, of the relevant passages 12	Relevant to Claim No 13
X Y	US,A, 4385296 (TSUBAKI et al) 24 May 1983 (24.05.83)	(1) (2-17)
X Y	US,A, 4422071 (de GRAAF) 20 December 1983 (20.12.83)	(1) (2-17)
X Y	WO,A, 88/05247 (MOTOROLA INC.) 14 July 1988 (14.07.88)	(1) (2-17)
P,Y	GB,A, 2206718 (CHINESE COMPUTERS LTD) 11 January 1989 (11.01.89)	(1-17)
A	US,A, 4392133 (LUNDGREN) 5 July 1985 (05.07.85)	
A	US,A, 4396914 (ASTON) 2 August 1983 (02.08.83)	

(continued)

* Special categories of cited documents: 10

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
15 February 1990 (15.02.90)	20/02/90
International Searching Authority	Signature of Authorized Officer
Australian Patent Office	R. TOLHURST

Form PCT/ISA/210 (second sheet) (January 1985)

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A	GB,A, 2119548 (CARTER et al) 16 November 1983 (16.11.83)	
A	US,A, 4519228 (SORNES) 28 May 1985 (28.05.85)	

V. [<>] OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE 1

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.[<>] Claim numbers ...<>, because they relate to subject matter not required to be searched by this Authority, namely:
<>

2.[<>] Claim numbers <>, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
<>

3.[<>] Claim numbers ...<>, because they are dependent claims and are not drafted in accordance with the second and third sentences of PCT Rule 6.4 (a):

VI. [<>] OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING 2

This International Searching Authority found multiple inventions in this international application as follows:
<>

1.[<>] As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2.[<>] As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:
<>

3.[<>] No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:
<>

4.[<>] As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

[<>] The additional search fees were accompanied by applicant's protest.

[<>] No protest accompanied the payment of additional search fees.

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL APPLICATION NO. PCT/AU 89/00489

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report	Patent Family Members		
US 4385296	CA 1115385	DE 2923962	GB 2023899
	JP 54163288	JP 55045944	
US 4422071	CH 660269	DE 3102423	FR 2474724
	GB 2068616	IT 1135224	JP 56131236
	NL 176889	SE 449038	US 4422071
GB 2206718	AU 18769/88	CN 87107896	
US 4392133	AU 59895/80	BR 8008703	DE 3065670
	EP 29441	JP 56500616	SE 429884
	WO 8002711		
GB 2119548	EP 800604		
US 4519228			
WO 88/05247	AU 75869/87	EP 344149	
US 4396914	AU 545929	BR 8104174	CA 1167131
	DE 3162790	DK 153805	EP 44630
	ES 503604	FI 79741	HK 643/85
	HU 191033	IL 63201	JP 57081573
	MX 150089	NO 812237	RO 88736

END OF ANNEX