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US 5365094 A

(58) Field of Search
UK CL (Edition) **H1K KDEG**
INT CL[6] **H01L 27/108 27/115 29/78 29/792**
On-line: WPI, JAPIO, INSPEC

(54) **Ferroelectric memory structure**

(57) A ferroelectric memory device having a MFIS FET structure, uses a yttrium oxide (Y_2O_3) film (11a) as a buffer film and comprises a p-type silicon substrate (1), a field oxide film (2) formed in a device isolation region of the substrate (1), a gate yttrium oxide film (11a), a gate ferroelectric film (12a), a gate TiN electrode (13a), and an n-type source/drain region (3) on both sides of the gate electrode (13a). In another embodiment, (Figure 3) an LDD structure is provided with a spacer SiON film (18a) over the gate structure and an impurity region (9a) above the source/drain region. The yttrium oxide film is readily formed as single crystals; and its lattice constant and thermal expansion coefficient matches those of the silicon substrate. Thus a good-quality ferroelectric film can be formed thereon. The devices are made by masking, etching and ion implantation, (Figures 4A to 4C, and 5A to 5E).

FIG.2

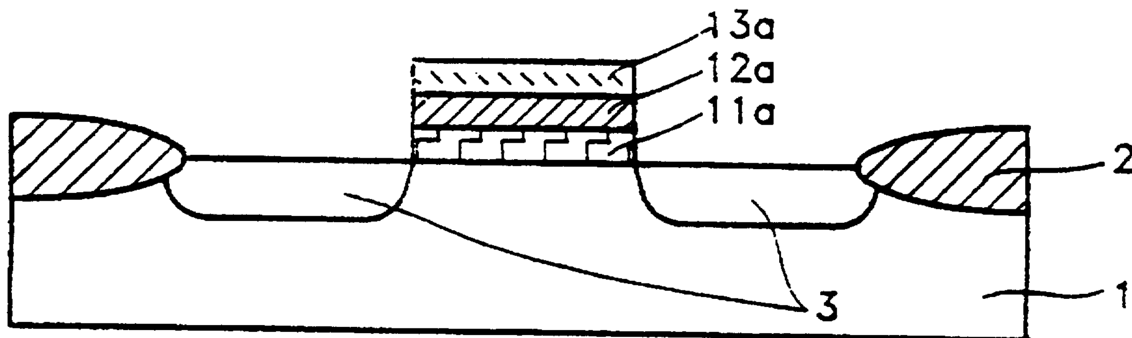

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FIG.1(PRIOR ART)

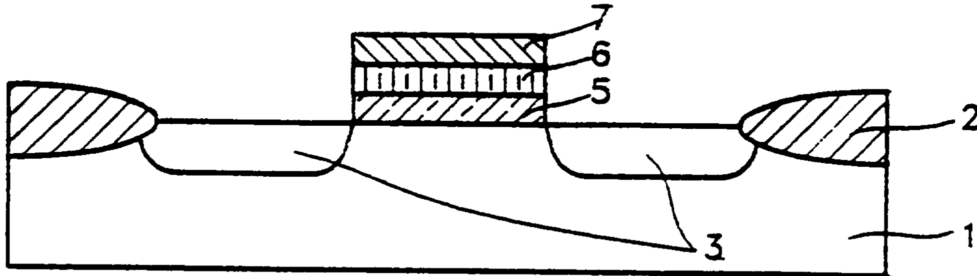


FIG.2

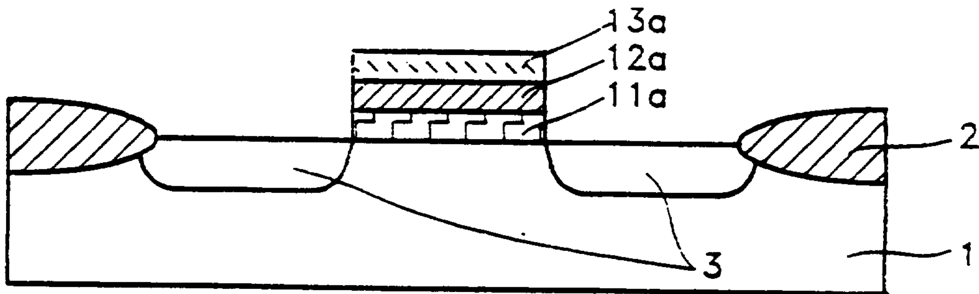


FIG.3

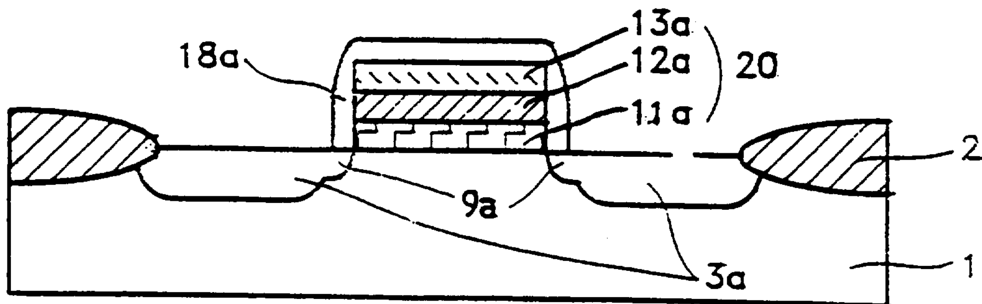


FIG.4A

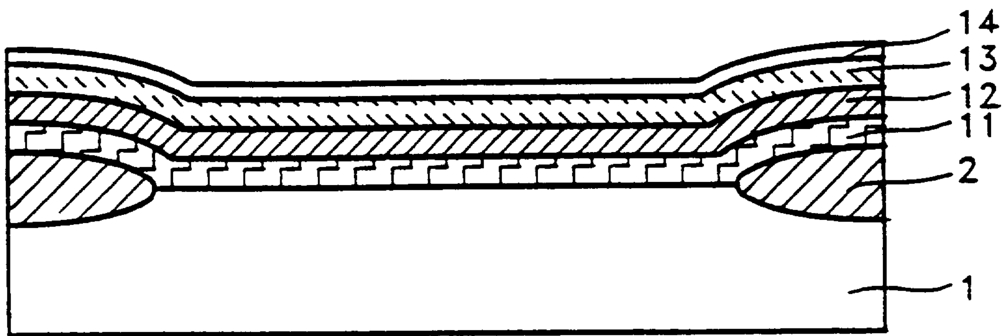


FIG.4B

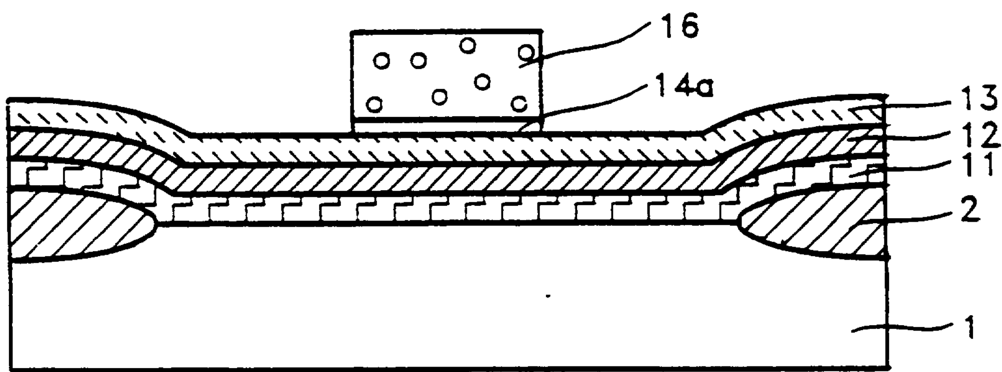


FIG.4C

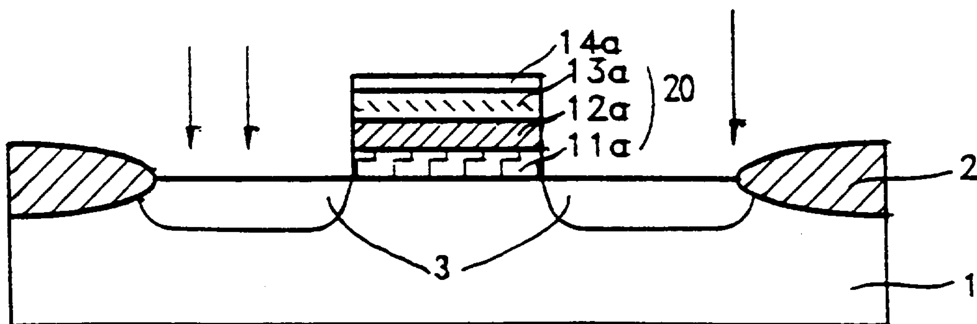


FIG.5A

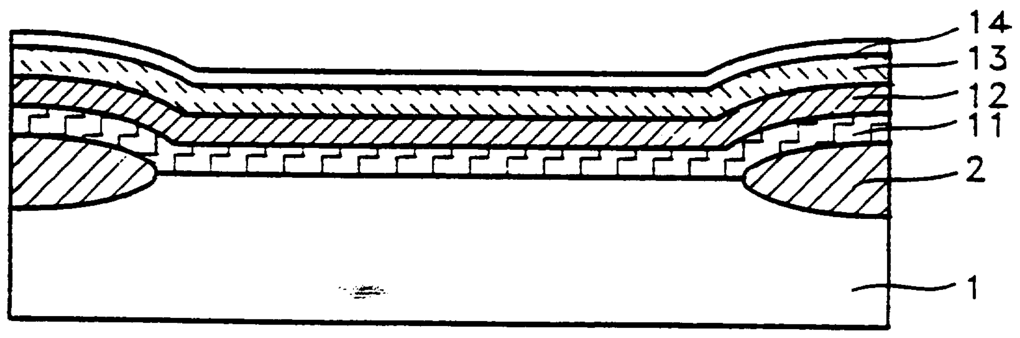


FIG.5B

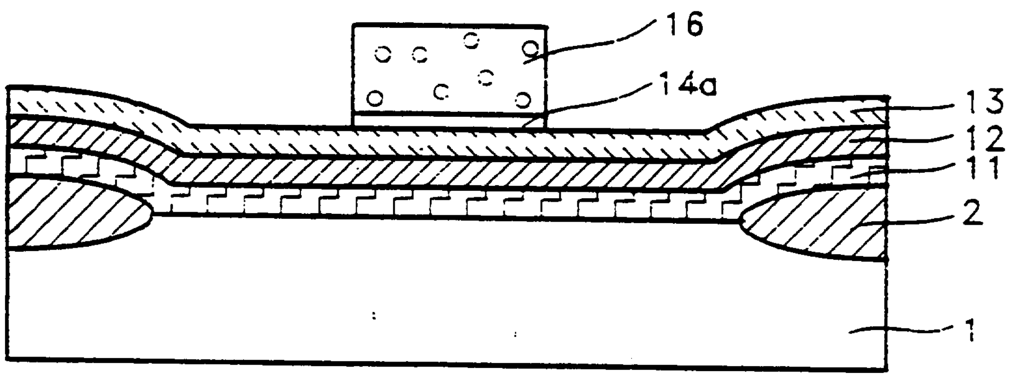


FIG.5C

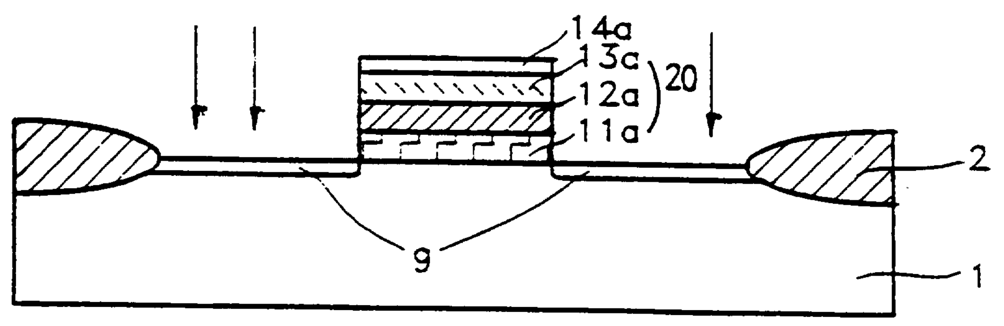


FIG.5D

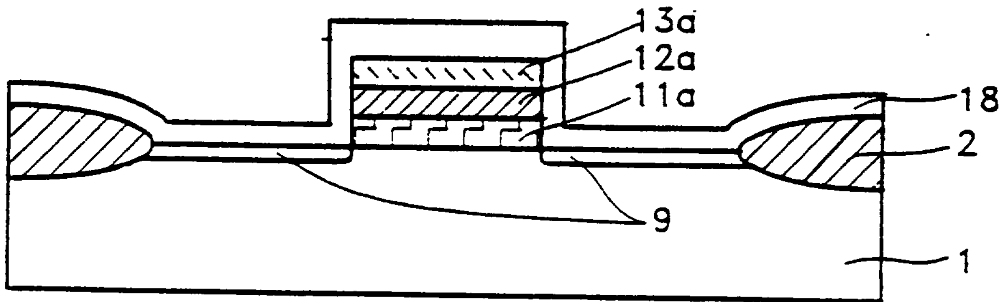
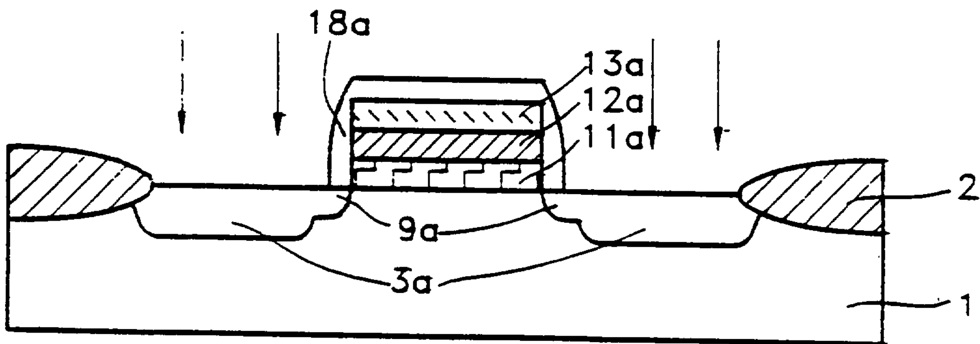


FIG.5E



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FERROELECTRIC MEMORY DEVICE AND MANUFACTURING METHOD THEREOF

The present invention relates to a semiconductor memory device and a manufacturing method thereof, and, more 5 particularly, to a ferroelectric memory device in which a ferroelectric film is used for a gate insulating film and a manufacturing method thereof.

Recent advances in thin-film technology have led to the prduction of nonvolatile memory devices using 10 ferroelectric films (i.e., ferroelectric memory devices), which can perform high-speed read/write operations by using the polarization reversal and retention characteristics of these films. Since the polarization reversal of a ferroelectric film is caused by a transition at the atomic 15 level, a ferroelectric memory device operates 10^4-10^5 times faster than other types of nonvolatile memories (e.g., EEPROM or flash memory devices) and thus can achieve read-cycle speeds comparable to those of a DRAM device, i.e., in the hundreds of nanoseconds. Also, since polarization 20 reversal needs only a low supply voltage of, say, two to five volts, the higher supply voltage (10-12V) necessary for EEPROM or flash memory read operations is not required.

Broadly speaking, there are two types of conventional ferroelectric memory devices: ones which detect the amount 25 of charge stored in a capacitor, and ones which detect a change in the resistance caused by the spontaneous polarization of a ferroelectric.

The first type is constructed either of two

transistors and two capacitors or of a single transistor-capacitor pair. Memory devices of this type are widely used in DRAM devices and are generally formed of CMOS transistors, with a thick interlayer insulating film separating the transistors from a ferroelectric capacitor formed on top. With this structure, even though the impact of the ferroelectric electrode material on the underlying CMOS device can be reduced, there is a persisting destructive read-out problem (i.e., the stored data is destroyed by merely reading it). Destructive read-out becomes a concern if the number of read/write operations in a memory device is to be increased.

One of the ferroelectric memory devices of the second type is called a metal-ferroelectric insulator semiconductor field-effect transistor (MFIS FET). Such a device provides for nondestructive read-out, which makes it appropriate for increased read/write operations. In principle, in using this type of memory device, which has just one transistor as compared to a DRAM which has one transistor and one capacitor, the cell area can be reduced without altering the cell structure in accordance with typical MOS FET scaling rules. Moreover, its read time need not be as long as that of a flash memory, which is a nonvolatile memory, and data can be retained after a read-out operation. The memory device employs a metal-insulator semiconductor (MIS) structure utilizing a ferroelectric film as a gate insulating film, in which a read-out operation is performed by forming an inversion layer in a

channel region of a transistor. Here, the inversion layer is formed by controlling the potential on a silicon interface depending on the polarization retention of a ferroelectric.

5 However, there are many problems encountered in the utilization of the MFIS FET. The major problem derives from the fact that a ferroelectric film is formed directly on a silicon semiconductor substrate.

This problem is that when a film of an oxide 10 ferroelectric such as PZT ($PbZr_xTi_{1-x}O_3$) is formed directly on the silicon substrate, oxygen atoms are injected from the oxygen-rich ferroelectric film into its interface with the silicon substrate, thereby resulting in the formation of a superfluous thin film of, for example, SiO_2. As a 15 result, the composition ratio of the ferroelectric film is locally destroyed, or a higher operating voltage is required. Furthermore, charged particles are injected into the film by trap levels resulting from stress of the ferroelectric film, thereby erasing the charge produced by 20 polarization retention. If the film is formed at high temperature, constituents of the ferroelectric are also apt to diffuse into the silicon substrate and alter the characteristics of the field effect transistor. Although a non-oxide ferroelectric (e.g., $BaMgF_4$) could be used instead 25 of an oxide ferroelectric such as indicated above, fluorine ions then penetrate into the gate insulating film, resulting in the elimination of the polarization characteristics.

Accordingly, since a ferroelectric film is not compatible with a silicon substrate in terms of lattice constant and thermal expansion coefficient, it is very difficult to form a high-quality ferroelectric film on the silicon substrate. Moreover, in order to form the source/ drain regions by self-alignment, a film showing tolerance to a thermal process at approximately 1,000°C is required.

To solve the above problems, an MFIS FET in which $PbTiO_3$ film is deposited on a CeO_2 film and aluminum is used for the electrodes has recently been reported (55th Applied Physics Society, Japan).

FIG. 1 is a sectional view showing a conventional MFIS FET using a CeO_2 film.

Referring to FIG. 1, reference numeral 1 denotes a p-type silicon substrate, reference numeral 2 denotes a field oxide film, reference numeral 3 denotes a source/drain region, reference numeral 5 denotes a CeO_2 film, reference numeral 6 denotes a $PbTiO_3$ ferroelectric film, and reference numeral 7 denotes an aluminum gate electrode. Here, the hetero-epitaxial growth of $PbTiO_3$ ferroelectric film 6 is achieved by utilizing CeO_2 film 5 as a gate insulating film. Since, in this structure, the gate electrode is formed after forming the ferroelectric film at high temperature, aluminum can be used as the electrode material and the structure is suitable for integration. The MFIS FET can in this way be applied in a memory device.

However, though the CeO_2 film of FIG. 1 exhibits little lattice mismatching (0.35%) with a (111) substrate, it has

no great advantage with respect to a (100) substrate. Further, the electrical characteristics of the MFIS FET are not completely verified.

It is an object of the present invention to provide a ferroelectric memory device having an insulating film which is matched well with silicon in terms of lattice constant and thermal expansion coefficient.

It is another object of the present invention to provide a method for manufacturing the above ferroelectric memory device.

To achieve the above object, there is provided a ferroelectric memory device comprising: a first conductive semiconductor substrate; a gate yttrium oxide (Y_2O_3) film formed on the semiconductor substrate; a gate ferroelectric film formed on the gate yttrium oxide film; a gate electrode formed on the gate ferroelectric film; and a source/drain region of a second conductive type contrary to the first conductive type, formed in the semiconductor substrate of both sides of the gate electrode.

Preferably, the gate ferroelectric film is formed of PZT, PT, or Y1 family materials, and the gate electrode is formed of one of a TiN film and a double-layered film having a TiN film and tungsten.

To achieve the above subject, there is also provided a ferroelectric memory device comprising: a first conductive semiconductor substrate; a gate yttrium oxide film formed on the semiconductor substrate; a gate ferroelectric film formed on the gate yttrium oxide film;

a gate electrode formed on the gate ferroelectric film; a spacer formed on each sidewall of a gate having the gate yttrium oxide film, the gate ferroelectric film, and the gate electrode; a first-concentration impurity region of a second conductive type contrary to the first conductive type, formed below the spacer in the semiconductor substrate; and a second-concentration source/drain region of the second conductive type, formed in the semiconductor substrate of both sides of the gate and connected to the first-concentration impurity region, the second concentration being higher than the first concentration.

Preferably, the gate ferroelectric film is formed of one of PZT, PT, and Y1 family materials, and the gate electrode is formed of one of a TiN film and a double-layered film having a TiN film and tungsten. In addition, the spacer is formed of one of SiO_2, Si_3N_4, SiON, and Y_2O_3.

To achieve another object, there is provided a method for manufacturing a ferroelectric memory device, the method comprising the steps of: forming a device isolation region in a predetermined area of a first conductive type semiconductor substrate; sequentially depositing a yttrium oxide film, a ferroelectric film, and a gate conductive film on the whole surface of the semiconductor substrate; forming a mask pattern; forming a gate electrode, a gate ferroelectric film and a gate yttrium oxide film by sequentially etching the gate conductive film, the ferroelectric film, and the yttrium oxide film, while using the mask pattern as an etching mask; and forming a source/

drain region by ion-implanting an impurity of a second conductive type contrary to the first conductive type into the semiconductor substrate.

Preferably, the mask pattern is formed of one of SiON, SiO_2, and Si_3N_4.

To achieve another object, there is also provided a method for manufacturing a ferroelectric memory device, the method comprising the steps of: forming a device isolation region in a predetermined area of a first conductive type semiconductor substrate; sequentially depositing a yttrium oxide film, a ferroelectric film, a gate conductive film and a mask material layer; forming a mask material layer pattern by patterning the mask material layer; forming a gate comprised of a gate electrode, a gate ferroelectric film and a gate yttrium oxide film by sequentially etching the gate conductive film, the ferroelectric film and the yttrium oxide film while using the mask material layer pattern as an etching mask; ion-implanting a first concentration impurity of a second conductive type contrary to the first conductive type into the semiconductor substrate at a first concentration; forming a spacer on each sidewall of the gate by depositing a material layer on the whole surface of the semiconductor substrate and dry-etching the material layer; and forming a source/drain region by ion-implanting a second-concentration impurity of the second conductive type contrary to the first conductive type into the semiconductor substrate, the second concentration being higher than the first concentration.

It is desirable that the mask material layer is formed of one of SiON, SiO_2, Si_3N_4, and Y_2O_3, and the material layer is formed of the same material as that of the mask material layer.

5 In the present invention, the yttrium oxide film is used as a buffer dielectric film between the silicon semiconductor substrate and the ferroelectric film. The present invention has an advantage in that it is easy to form single crystals (heteroepitaxy) of the yttrium oxide
10 film on the semiconductor substrate. Another advantage is that when a PZT or a PT ferroelectric film is formed on the yttrium oxide film, it is possible to form a ferroelectric film being an epitaxial layer well-arranged along the C-axis, thereby enhancing the polarization characteristics of
15 the films. Therefore, a good-quality ferroelectric film can be formed on a silicon semiconductor substrate.

Specific embodiments of the present invention are described in detail below, with reference to the attached drawings, in which:

20 FIG. 1 is a sectional view of a conventional MFIS FET using a CeO_2 film;

FIG. 2 is a sectional view of an MFIS FET according to an embodiment of the present invention;

FIG. 3 is a sectional view of an MFIS FET of an LDD
25 structure according to an embodiment the present invention;

FIGS. 4A-4C are sectional views of sequential steps in a process for manufacturing the device of FIG. 2; and

FIGS. 5A-5E are cross-sectional views of sequential

steps in a process for manufacturing the device of FIG. 3.

The present invention will be described in detail, referring to the attached drawings. First, the structure of a ferroelectric memory device according to an emodiment of the present invention will be described.

Embodiment 1

FIG. 2 is a sectional view of an MFIS FET according to a first embodiment of the present invention.

Referring to FIG. 2, the ferroelectric memory device is an MFIS FET having a p-type silicon substrate 1, a field oxide film 2 formed in a device isolation area of p-type silicon substrate 1, a gate yttrium oxide (Y_2O_3) film 11a of a predetermined size formed on the surface of p-type silicon substrate 1, a gate ferroelectric film 12a formed on gate yttrium oxide film 11a, a gate TiN electrode 13a formed on gate ferroelectric film 12a, and an n-type source/drain region 3 formed in p-type silicon substrate 1 on both sides of gate TiN electrode 13a.

Embodiment 2

FIG. 3 is a cross-sectional view schematically showing an MFIS FET of an LDD structure according to a second embodiment of the present invention.

Referring to FIG 3, the ferroelectric memory device according to the present invention is an LDD MFIS FET having a p-type silicon substrate 1, a field oxide film 2 formed in a device isolation area of p-type silicon substrate 1, a gate yttrium oxide film 11a of a predetermined size formed on p-silicon substrate 1, a gate

ferroelectric film 12a formed on gate yttrium oxide film 11a, a gate TiN electrode 13a formed on gate ferroelectric film 12a, a spacer SiON film 18a formed of an insulating film on the entire surface of a gate 20 comprising gate yttrium oxide film 11a, gate ferroelectric film 12a and gate TiN film 13a, a first concentration impurity region 9a which contains an n-type impurity and is formed below spacer SiON film 18a in p-type silicon substrate 1, and a second concentration source/drain region 3a formed in p-type silicon substrate 1 on both sides of gate 20, and connected to first concentration impurity region 9a, the second concentration being higher than the first concentration. As shown in FIG. 3, the LDD structure has first concentration impurity region 9a and second concentration source/drain region 3a, the second concentration being higher than the first concentration.

A method for manufacturing a ferroelectric memory device according to an embodiment of the present invention will be described.

FIGS. 4A-4C are cross-sectional views sequentially showing the steps in a process for manufacturing the MFIS FET shown in FIG. 2.

FIG. 4A shows the step of sequentially depositing a yttrium oxide film 11, a ferroelectric film 12, a TiN film 13 and an SiON film 14 on the whole surface of p-type silicon substrate 1. Referring to FIG. 4A, field oxide film 2 is formed on p-type silicon substrate 1 by a general device isolation method such as a LOCOS, SEPOX or STI

method. After the surface of p-type silicon substrate 1 is cleaned, the epitaxial layer of yttrium oxide film 11 is formed on the whole surface of p-type silicon substrate 1. Here, yttrium oxide film 11 is formed by, for example, sputtering, reactive ionized cluster beam deposition, or metal organic chemical vapor deposition. Thereafter, a ferroelectric film 12 of, for example, PZT, PT ($PbTiO_3$), or Y1 family materials is formed on yttrium oxide film 11, and then a TiN film 13 is formed for use as a gate conductive film. The TiN film 13 can be replaced with a double-layered film of TiN and tungsten. Thereafter, SiON film 14 is deposited for use as a mask material layer. SiO_2, Si_3N_4, or Y_2O_3 can be used instead of the SiON film 14.

FIG. 4B shows the step of forming an SiON film pattern 14a by photolithography. Referring to FIG. 4B, a photoresist pattern 16 is formed on SiON film 14 by photolithography, and SiON film 14 is then dry-etched by using the photoresist pattern 16 as an etching mask, thereby forming SiON film pattern 14a.

FIG. 4C shows the step of forming gate yttrium oxide film 11a, gate ferroelectric film 12a and gate TiN electrode 13a. Referring to FIG. 4C, the photoresist pattern 16 is removed, and thereafter, TiN film 13, ferroelectric film 12 and yttrium oxide film 11 are anisotropically etched, sequentially, while using the SiON film pattern 14a as a mask, thereby forming gate 20 having gate yttrium oxide film 11a, gate ferroelectric film 12a and gate TiN film 13a. Thereafter, arsenic, i.e., an n-type

impurity, is ion-implanted into the whole surface of p-type silicon substrate 1 while using SiON film pattern 14a and gate 20 as a mask, and the ion-implanted n-type impurity is activated, thereby forming source/drain region 3. Thereafter, the SiON film pattern 14a is removed. Thus, the MFIS FET shown in FIG. 2 is completed.

FIGS. 5A-5E are cross-sectional views sequentially showing the steps of a process for manufacturing the LDD MFIS FET shown in FIG. 3.

The steps shown in FIGS. 5A and 5B are performed in the same manner as those of FIGS. 4A and 4B.

FIG. 5C shows the step of sequentially forming gate yttrium oxide film 11a, gate ferroelectric film 12a, and gate TiN electrode 13a. Referring to FIG. 5C, photoresist pattern 16 is removed and TiN film 13, ferroelectric film 12 and yttrium oxide film 11 are anisotropically etched, sequentially, while using SiON film pattern 14a as a mask, thereby forming a gate 20 having gate yttrium oxide film 11a, gate ferroelectric film 12a and gate TiN electrode 13a. Thereafter, phosphorous, i.e., an n-type impurity, is ion-implanted into the whole surface of p-type silicon substrate 1 at a low concentration while using SiON film pattern 14a and gate 20 as a mask, thereby forming an impurity region 9.

FIG. 5D shows the step of depositing a material SiON film 18, providing a material layer on the whole surface of p-type silicon substrate 1, to form a spacer. Here, the material SiON film 18 can be replaced with SiO_2 or Si_3N_4.

Material SiON film 18 is formed of the same insulating film as that of the mask material layer, gate 20 is surrounded by one material, and material SiON film 18 can act sufficiently as a gate insulating material in a subsequent process.

FIG. 5E shows the step of forming a spacer SiON film 18a on each sidewall of gate 20. Referring to FIG. 5E, spacer SiON film 18a is formed on the sidewalls of gate 20 by anisotropically etching SiON film 18a. Arsenic, i.e., an n-type impurity, is ion-implanted into the whole surface at a high concentration while using gate 20 and spacer SiON film 18a as a mask, and the ion-implanted impurity is activated, thereby forming first concentration impurity region 9a and second impurity source/drain region 3a. Thus, the LDD MFIS FET shown in FIG. 3 is completed.

As described above, the yttrium oxide film is used as a buffer dielectric film between the silicon semiconductor substrate and the ferroelectric film. The present invention has an advantage in that it is easy to form the single crystals (heteroepitaxy) of the yttrium oxide film on the semiconductor substrate. Another advantage is that when a PZT or a PT ferroelectric film is formed on the yttrium oxide film, a ferroelectric film consisting of an epitaxial layer well-arranged along a C-axis can be formed, thereby enhancing the polarization characteristics of the films. Accordingly, a good-quality ferroelectric film can be formed on a silicon semiconductor substrate.

Furthermore, excellent current-voltage and

capacitance-voltage characteristics are obtained when the yttrium oxide film is used as an insulating film. A memory device using a yttrium oxide film, therefore, exhibits excellent electrical characteristics.

5 Though the present invention has been specifically described with the above embodiments, it is not restricted to these embodiments and many variations can be made within the scope of the invention by anyone skilled in the art. For example, a p-type MFIS FET can be manufactured using an
10 n-type silicon substrate, in accordance with either of the above embodiments.

CLAIMS:

1. A ferroelectric memory device comprising:

a semiconductor substrate of a first conductivity type;

5 a gate yttrium oxide (Y_2O_3) film formed on said semiconductor substrate;

a gate ferroelectric film formed on said gate yttrium oxide film;

a gate electrode formed on said gate ferroelectric

10 film; and

a source/drain region of a second conductivity type opposite to said first conductivity type, formed in said semiconductor substrate to both sides of said gate electrode.

15 2. A ferroelectric memory device comprising:

a semiconductor substrate of a first conductivity type;

a gate yttrium oxide film formed on said semiconductor substrate;

20 a gate ferroelectric film formed on said gate yttrium oxide film;

a gate electrode formed on said gate ferroelectric film;

a spacer formed on each sidewall of a gate comprising

25 said gate yttrium oxide film, said gate ferroelectric film, and said gate electrode;

a first-concentration impurity region of a second conductive type opposite to the first conductive type,

formed below said spacer; and

a second-concentration source/drain region of the second conductive type, the second concentration being higher than the first concentration, formed in said
5 semiconductor substrate to both sides of said gate and connected to said first-concentration impurity region.

3. A ferroelectric memory device as claimed in claim 2, wherein said spacer is formed of a material selected from the group consisting of SiO_2, Si_3N_4, Y_2O_3, and SiON.

10 4. A ferroelectric memory device as claimed in any preceding claim, wherein said gate ferroelectric film is formed of a material selected from the group consisting of PZT, PT, and Y1 family materials.

5. A ferroelectric memory device as claimed in any
15 preceding claim, wherein said gate electrode is formed of one selected from the group consisting of a TiN film and a double-layered film of TiN and tungsten.

6. A method of manufacturing a ferroelectric memory device, comprising the steps of:

20 forming a device isolation region in a predetermined area of a semiconductor substrate of a first conductivity type;

sequentially depositing a yttrium oxide film, a ferroelectric film, and a gate conductive film on the whole
25 surface of said semiconductor substrate;

forming a mask pattern;

forming a gate electrode, a gate ferroelectric film and a gate yttrium oxide film by etching said gate

conductive film, said ferroelectric film and said yttrium oxide film, using said mask pattern as an etching mask; and

forming a source/drain region by ion-implanting a impurity of a second conductivity tupe into said semiconductor substrate.

7. A method for manufacturing a ferroelectric memory device as claimed in claim 6, wherein said mask pattern is formed of one selected from the group consisting of SiON, SiO_2 and Si_3N_4.

8. A method for manufacturing a ferroelectric memory device, comprising the steps of:

forming a device isolation region in a predetermined area of a conductor substrate of a first conductivity type;

sequentially depositing a yttrium oxide film, a ferroelectric film, a gate conductive film and a mask material layer;

forming a mask material layer pattern by patterning said mask material layer;

forming a gate of a gate electrode, a gate ferroelectric film and a gate yttrium oxide film by etching said gate conductive film, said ferroelectric film and said yttrium oxide film, using said mask material layer pattern as an etching mask;

ion-implanting a first concentration of an impurity of a second conductive type opposite to the first conductive type into said semiconductor substrate;

forming a spacer on each sidewall of said gate by depositing a material layer on the whole surface of said

semiconductor substrate and dry-etching said material layer; and

forming a source/drain region by further ion-implanting a second concentration of an impurity of the second conductive type into said semiconductor substrate, said second concentration being higher than said first concentration.

9. A method for manufacturing a ferroelectric memory device as claimed in claim 8, wherein said mask material layer is formed of a material selected from the group consisting of SiON, SiO_2, Y_2O_3, and Si_3N_4.

10. A method for manufacturing a ferroelectric memory device as claimed in claim 9, wherein said material layer is formed of the same material as that of said mask material layer.

11. A ferroelectric memory device substantially as herein described with reference to Figure 2 or Figure 3 of the accompanying drawings.

12. A method for manufacturing a ferroelectric memory device substantially as herein described with reference to any of Figures 4A to 5E of the accompanying drawings.

The Patent Office

19

Application No: GB 9606024.9
Claims searched: 1 to 12

Examiner: J L Freeman
Date of search: 31 May 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K (KDEG)

Int Cl (Ed.6): H01L (27/115, 29/78, 29/792)

Other: On-line: WPI, JAPIO, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	US 5365094 (H Takasu) Figure 1	1

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
		E	Patent document published on or after, but with priority date earlier than, the filing date of this application.
&	Member of the same patent family		