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Dobkin

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[54] **INPUT SUPPLY INDEPENDENT CIRCUIT**

[75] Inventor: **Robert C. Dobkin,** Hillsborough, Calif.

[73] Assignee: **National Semiconductor Corporation,** Santa Clara, Calif.

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[52] **U.S. Cl.** **307/297;** 323/4; 330/199

[51] **Int. Cl.²** **G05F 1/56**

[58] **Field of Search** ..... 323/1, 4, 9, 22 T; 307/296, 297; 330/199; 328/258, 267

[56] **References Cited**

UNITED STATES PATENTS

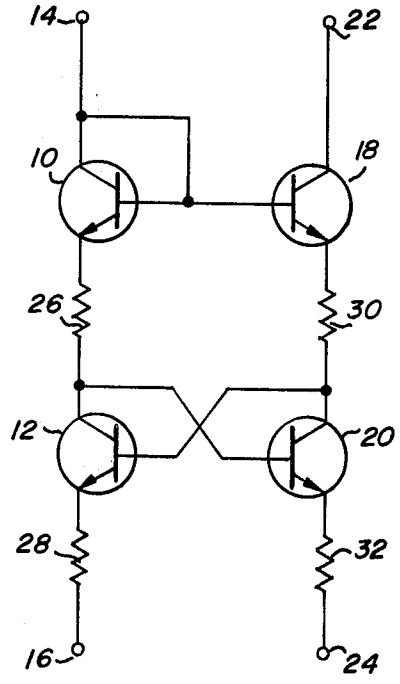
3,629,692 12/1971 Goyer ..... 307/297 X

Primary Examiner—Archie R. Borchelt
Assistant Examiner—E. R. LaRoche
Attorney, Agent, or Firm—Lowhurst & Aine

[57] **ABSTRACT**

A circuit includes a plurality of transistors which are biased by a supply to provide an output which is independent of that supply and dependent only on the summation of the base-emitter voltages of the transistors, if any. A first pair of transistors are connected in series with one another between the supply and a second pair of transistors are connected in series with one another between the supply. The base-emitter junctions of the transistors are connected in a series loop, such that a voltage is developed between the base-emitter junctions of two adjacent transistors which is equal to the base-emitter voltage summation. The base-emitter voltages of any series connected transistors oppose one another in the series loop. Since the collector currents of the series connected transistors are equal to one another and their base-emitter voltages oppose one another in the series loop, the base-emitter voltage summation will be independent of collector currents and, therefore, independent of the input supply. The circuit can be employed as either a voltage or current regulator. As a regulator circuit, the emitter area of one transistor is different than the emitter area of another transistor, such that the summation of the base-emitter voltages will be other than zero and independent of the input supply. The circuit can also be employed as a buffer amplifier by making the emitter areas of the transistors equal to one another.

16 Claims, 5 Drawing Figures



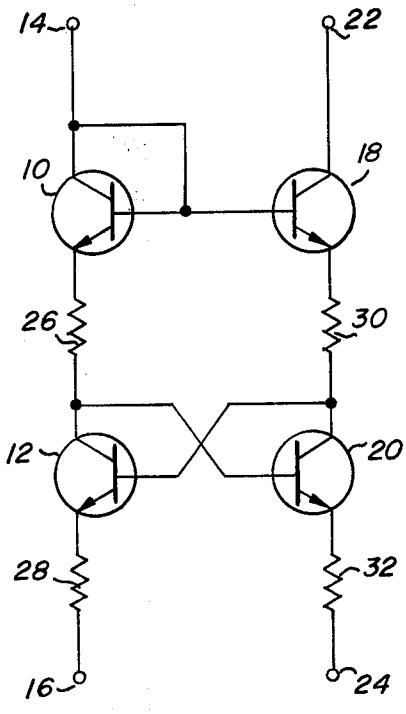


Fig_1

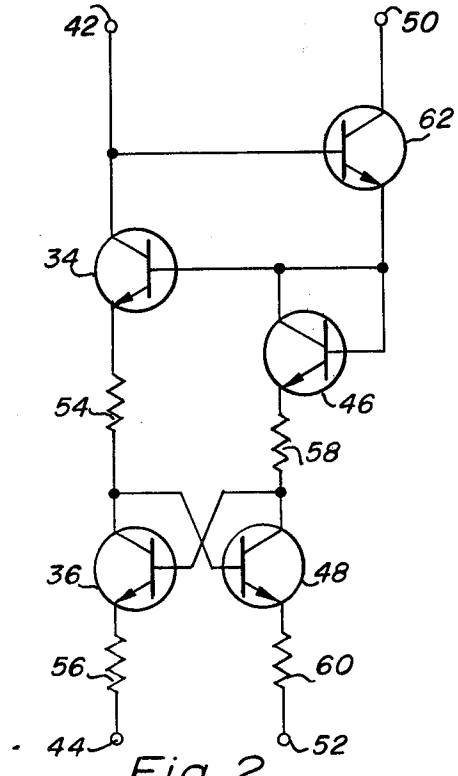


Fig_2

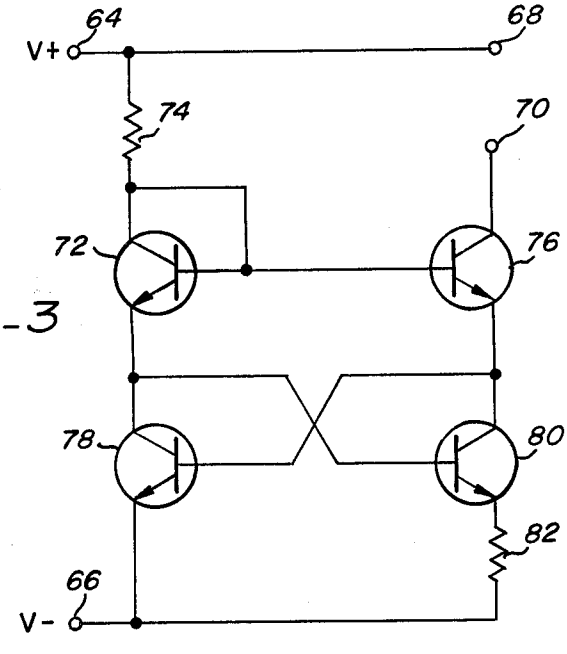


Fig_3

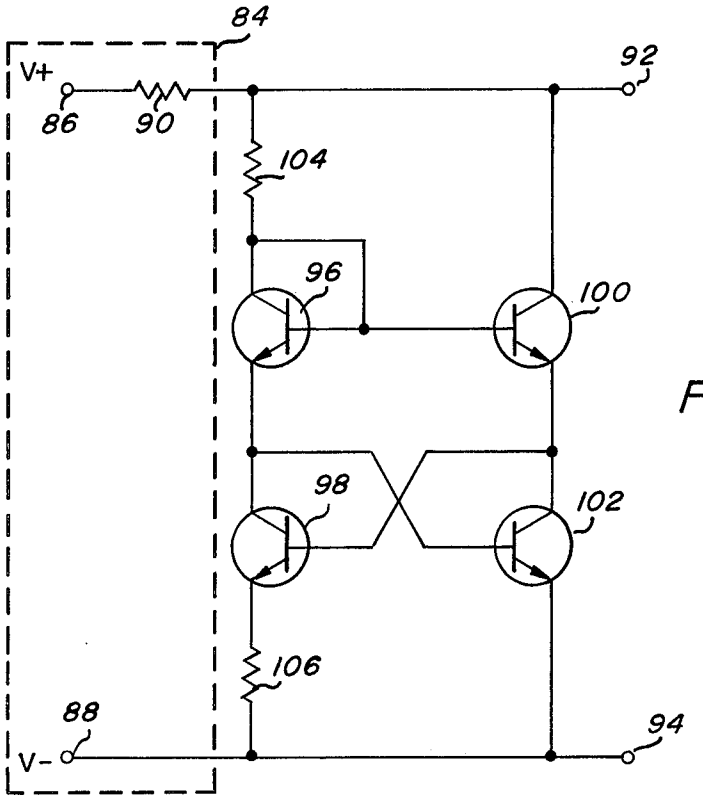

84
V+
86
90
92
104
96
100
98
102
106
88
V-
94

Fig_4

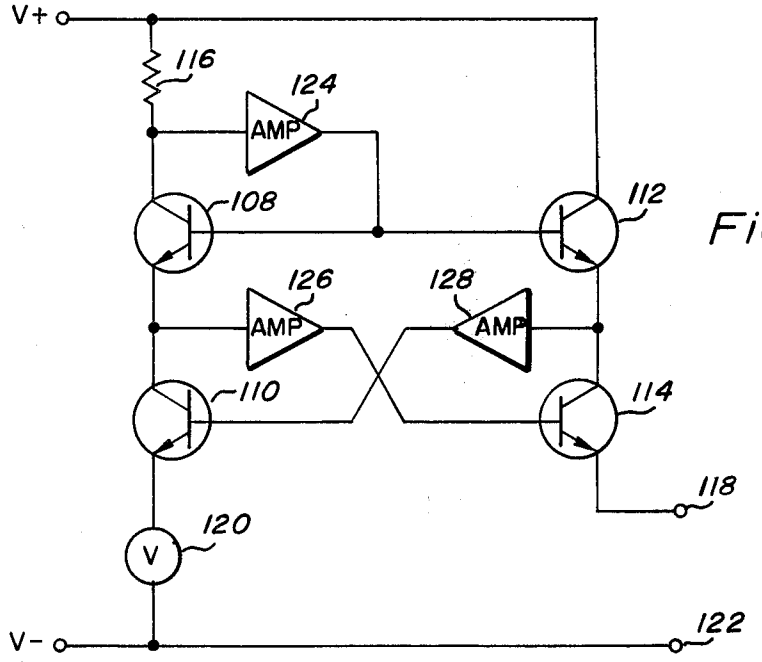

V+
116
124
AMP
108
112
126
AMP
128
AMP
110
114
118
120
V
V-
122

Fig_5

INPUT SUPPLY INDEPENDENT CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to a circuit having an output which is independent of its input supply, and more particularly to such a circuit in which a voltage related to the output voltage thereof is developed which is proportional only to the difference of the emitter areas of transistors.

2. Prior Art

Various types of circuits require an output which is independent of the input voltage or current supply. It has been the usual practice in the past to isolate the output of such circuits from the input supply with a relatively large number of components. This practice has resulted in relatively large and complex circuits. Since the cost of an integrated circuit is related to the number of components contained therein and to the complexity thereof, it is desirable to reduce the number of components required to produce a particular result to a minimum. Furthermore, the operation of such circuits is subject to processing parameters, rather than solely to basic transistor parameters, and such processing parameters are not easily controlled.

A good example of a circuit which requires its output to be independent of its input supply is a regulator circuit. A high degree of current or voltage regulation in integrated circuits has required relatively complex circuits in the past. For example, a Zener diode voltage regulator requires several stages of current amplification to reduce the dynamic impedance of the circuit to provide a well regulated voltage supply output. A relatively large number of components is required to provide the desired amount of current amplification and to decrease the dynamic impedance sufficiently to provide such a regulated supply.

Another type of circuit which requires its output to be independent of its input supply is a buffer amplifier. In a buffer amplifier, such as a voltage follower or current amplifier, it is desirable to have the voltage of the input signal source reflected exactly at the output, with a relatively high impedance input and low impedance output. If the output of such an amplifier is not independent of its input supply, variations in that supply will affect the output and the input voltage will not be reflected exactly at such output. Furthermore, if such output is dependent upon processing parameters, rather than solely on basic transistor parameters, the output cannot be well defined.

Accordingly, it can be appreciated that a need exists for a circuit which will provide an output which is independent of its voltage or current supply without being relatively complex, requiring a large number of components, and which is independent of processing parameters. More particularly, a need exists for such a circuit which is formed of relatively few components and is dependent only on basic transistor parameters for its operation, which parameters are capable of being controlled within relatively close tolerances.

SUMMARY OF THE INVENTION

Accordingly, it is a primary object of the present invention to provide a circuit having an output which is independent of its voltage or current supply.

Another object of the present invention is to provide a circuit having an output which is independent of its supply and has relatively few components.

A further object of the present invention is to provide such a circuit in which its operation is independent of processing parameters and dependent only on basic transistor parameters.

Still another object of the present invention is to provide a regulator circuit which requires relatively few components and which has a relatively high degree of regulation.

Yet another object of the present invention is to provide either a voltage or current regulator having an output which is unaffected by changes in its supply voltage or current.

A further object of the present invention is to provide such a voltage or current regulator which requires relatively few components to perform its function.

Another object of the present invention is to provide a buffer amplifier in which the voltage of an input signal source is reflected exactly at an output thereof.

Still another object of the present invention is to provide such a buffer amplifier having a relatively high impedance input and a relatively low impedance output.

A further object of the present invention is to provide such a buffer amplifier in which a relatively high current output can be provided without a current limiting resistor.

These and other objects of the present invention are attained by a transistor circuit in which an output voltage is developed which is equal to the summation of the base-emitter voltages of the transistors. This output voltage is employed to provide either a well regulated voltage or current output, or to reflect an input voltage exactly at an output of the circuit.

A feature of the present invention resides in maintaining the collector currents of any transistors connected in series equal to one another and their base-emitter voltages around a series loop opposing one another, such that the summation of the base-emitter voltages of the transistors is proportional only to the difference in emitter areas of the transistors, if any. If such a difference exists, the output voltage will be proportional thereto and other than zero. However, if such a difference does not exist, the output voltage will be zero and an input signal source can be reflected exactly at an output of the circuit.

Another feature of the present invention resides in the provision of a resistor in any one of the emitter circuits of the transistors, such that various output characteristics can be obtained.

The invention, however, as well as other objects, features and advantages thereof will be more fully realized and understood from the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a four terminal network constructed in accordance with the principles of the present invention.

FIG. 2 is a circuit diagram of an alternate embodiment of the four terminal network of the present invention.

FIG. 3 is a circuit diagram of a current regulator constructed in accordance with the principles of the present invention.

FIG. 4 is a circuit diagram of a voltage regulator constructed in accordance with the principles of the present invention.

FIG. 5 is a circuit diagram of a buffer amplifier constructed in accordance with the principles of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to FIG. 1, there is shown a four terminal network which is constructed in accordance with the principles of the present invention. A pair of transistors **10** and **12** have their collector-emitter circuits connected in series with one another between a pair of terminals **14** and **16.** A pair of transistors **18** and **20** have their collector-emitter circuits connected in series with one another between a pair of terminals **22** and **24.** Resistors **26, 28, 30** and **32** are connected in the emitter circuits of the transistors **10, 12, 18** and **20,** respectively. The value of any one or all of the resistors **26–32** may be zero. Preferrably, only one of the resistors **26–32** will have a value other than zero.

It can be appreciated from FIG. 1 that the base-emitter junctions of the transistors **10, 12, 18** and **20** are connected serially in a loop with one another. That is, beginning with the terminal **16,** the loop includes the resistor **28,** the base-emitter junction of the transistor **12,** the resistor **30,** the base-emitter junction of the transistor **18,** the base-emitter junction of the transistor **10,** the resistor **26,** the base-emitter junction of the transistor **20,** and the resistor **32.** If the terminal **16** is connected to the terminal **24** and only one of the resistors **26–32** has a value other than zero, the summation of the base-emitter voltages of the transistors will be developed on that resistor.

In the above described serial loop, the base-emitter voltage of the transistor **12** opposses the base-emitter voltage of the transistor **10** and the base-emitter voltage of the transistor **20.** Also, the base-emitter voltage of the transistor **20** opposes the base-emitter voltage of the transistor **18.** Since the transistors **10** and **12** have their collector-emitter circuits connected in series, their collector currents will be equal. It can be appreciated that the collector currents of the transistors **18** and **20** will also be equal. Accordingly, the summation of the base-emitter voltages of all of the transistors will be proportional to the difference of their emitter areas. That is, the difference of the base-emitter voltages, ΔV_{be}, which is the voltage developed across one of the resistors **26–32** having a value other than zero, is defined by the expression:

$$\Delta V_{be} = \frac{KT}{q} \ln \frac{J_{c2}}{J_{c1}} \qquad (1)$$

where J_{c_1} is the combined current density of the transistors **12** and **18** and J_{c2} is the combined current density of the transistors **10** and **20.** Accordingly, if the emitter areas of the transistors are of different values, the current density ratio of the above expression will be other than zero. It can be appreciated, therefore, that the voltage of an input source which supplies a bias to each of the transistors **10, 12, 18** and **20** will not affect the summation of the base-emitter voltages, ΔV_{be}, developed on one of the resistors **26–32** which has a value other than zero. It can also be appreciated that this summation of the base-emitter voltages, ΔV_{be}, will be zero if all of the emitter areas of the transistors are equal to one another.

An alternate embodiment of a four terminal network constructed in accordance with the principles of the present invention is illustrated in FIG. **2.** As shown therein, transistors **34** and **36** are connected in series between a pair of terminals **42** and **44** and transistors **46** and **48** are connected in series between a pair of terminals **50** and **52.** Resistors **54, 56, 58** and **60** are connected in the emitter circuits of the transistors **34, 36, 46** and **48,** respectively. It can be appreciated from the drawings and the above description that the circuit thus described in FIG. **2** is similar to the circuit illustrated in FIG. **1.** A transistor **62** has its collector-emitter circuit connected in series between the terminal **50** and the collector of the transistor **46** and has its base connected to the terminal **42.** The transistor **62** isolates the collector of the transistor **46** from any voltage changes which may occur on the terminal **50** and raises the output impedance of the circuit.

With reference to FIG. **3,** there is shown a current regulator which is constructed in accordance with the principles of the present invention. A voltage source, represented by V+ and V−, is connected to terminals **64** and **66.** The circuit of FIG. **3** is operative to provide a constant current through a load (not shown) when it is connected across terminals **68** and **70,** regardless of variations in the supply voltage on the terminals **64** and **66.**

The collector of a transistor **72** is connected through a resistor **74** to the terminal **64** and **68,** to its base, and to the base of a transistor **76** having its collector connected to the terminal **70.** The collector- emitter circuit of the transistor **72** is connected in series with the collector-emitter circuit of a transistor **78** and the collector-emitter circuit of a transistor **76** is connected in series with the collector-emitter circuit of a transistor **80.** The junction between the transistors **72** and **78** is connected to the base of the transistor **80** and the junction between the transistors **76** and **80** is connected to the base of the transistor **78.** The emitter of the transistor **78** is connected to the terminal **66** and the emitter of the transistor **80** is connected through a resistor **82** to the terminal **66.**

The current regulator illustrated in FIG. **3** is one example of a practical embodiment of the circuit illustrated in FIG. **1.** The only constraint on the circuit illustrated in FIG. **3** is that the resistor **74** must be of a value to provide a current therethrough which is greater than the output current of the transistor **72** divided by its beta. From inspection of the circuit, it will be appreciated that the voltage developed across the resistor **82** is equal to the sum of the base-emitter voltages of the transistors **76** and **78** less the sum of the base-emitter voltages of the transistors **72** and **80.** Since the summation of the base-emitter voltages of the transistors **72–80** is proportional to the difference of their emitter areas, if any, the voltage developed on the resistor **82** will also be proportional to that summation. For example, if the emitter areas of the transistors **72** and **78** are equal and, since their collector currents are equal, their base-emitter voltages will cancel one another. In such an example, the voltage developed across the resistor **82** will equal to the base-emitter voltage of the transistor **76** less the base-emitter voltage of the transistor **80.** This difference of the base-emitter voltages is defined by the above expression where J_c and J_c are current densities of the transistors **76** and **80,**

respectively. It can be appreciated that the load current, which is equal to the current through the resistor **82**, will remain constant since its value depends upon the ratio of the current densities of the transistors and such ratio will, of course, remain constant, since the collector currents of the transistors having their collector-emitter circuits in series are equal to one another.

With reference to FIG. **4**, there is shown a voltage regulator circuit which employs the principles of the circuit illustrated in FIG. **1**. A current source, represented diagrammatically by a dotted outline block which is designated with the reference numeral **84**, includes a voltage source designated by V+ and V− connected to terminals **86** and **88** and a resistor **90**. It is to be understood, of course, that any current source may be employed for supplying the circuit. The circuit of FIG. **4** supplies a regulated voltage across a pair of terminals **92** and **94**.

Transistors **96, 98, 100** and **102** are connected in the same configuration as that of FIG. **1**. The collector of the transistor **96** is connected through a resistor **104** to one side of the supply **84** and to the terminal **92**. The emitter of the transistor **98** is connected through a resistor **106** to the terminals **88** and **94**.

The voltage developed across the resistor **106** is equal to the sum of the base-emitter voltages of the transistors **96** and **102** less the sum of the base-emitter voltages of the transistors **98** and **100**. Since the voltage developed across the resistor **106** is independent of its resistance value, a low regulated voltage is developed thereon. This regulated voltage is reflected at the terminals **92** and **94** as an output voltage having a high degree of regulation. Furthermore, this voltage will be proportional to the difference of the emitter areas of the transistors and will be independent of the current supply **84** and the voltage supply on the terminals **86** and **88**.

The circuit illustrated in FIG. **4** performs such voltage regulation by controlling the current through the transistors **100** and **102** to maintain the voltage on the terminals **92** and **94** constant. The value of the voltage developed on the terminals **92** and **94** is determined by the difference of the emitter areas of the transistors. From inspection, it can be appreciated that the voltage across the terminals **92** and **94**, V_s, is defined by the expression:

$$V_s = \Delta V_{be} \frac{R_2}{R_1} + V_{be1} + V_{be2}, \qquad (2)$$

where ΔV_{be} is the difference of the base-emitter voltages of the transistors having different emitter areas, R_2 is the value of the resistor **104**, R_1 is the value of the resistor **106**, V_{be_1} is the base-emitter voltage of the transistor **96**, and V_{be_2} is the base-emitter voltage of the transistor **102**. Since the first quantity in the above expression (2) has a positive temperature coefficient and the two remaining quantities have a negative temperature coefficient, at a particular output voltage on the terminals **92** and **94**, the circuit will exhibit a zero termperature coefficient. More particularly, such a zero temperature coefficient occurs when the output voltage on the terminals **92** and **94** is equal to 2.4 volts or 2 times the extrapolated band gap of silicon.

When the supply current attempts to increase, the conduction level of the transistors **100** and **102** will increase, to shunt current therethrough so that the voltage on the resistor **106** remains constant. By maintaining the voltage on the resistor **106** constant, the voltage across the terminals **92** and **94** will also remain constant.

The circuit illustrated in FIG. **5** is a buffer amplifier which employs the principles of the circuit illustrated in FIG. **1**. It can be appreciated from the drawing that the transistors **108, 110, 112** and **114** are connected together to form the circuit illustrated in FIG. **1** when all of the resistors **26–32** have a value of zero. One side of a voltage supply, designated V+, is connected to the collector of the transistor **112** and through a resistor **116** to the collector of the transistor **108**. The emitter of the transistor **114** is connected to one output terminal **118** and the emitter of the transistor **110** is connected through an input signal source **120** to the other side of the voltage supply, designated V−, and to another output terminal **122**.

If the emitter areas of the transistors **108–114** are equal to one another, the voltage of the input signal source **120** will be reflected exactly on the terminals **118** and **122**. It can be appreciated that the input signal source **120** can be any source, including the circuit illustrated in FIG. **4**. The circuit of FIG. **5** presents a relatively high impedance to the input signal source **120** and provides a relatively low impedance output on the terminals **118** and **122**. Furthermore, a relatively high current output can be provided across the terminals **118** and **122** without a current limiting resistor in the circuit.

Since the limit of the circuit illustrated in FIG. **5** is controlled by the betas of the transistors **108–114**, the base drive to each of those transistors can be increased to permit a relatively high output current across the terminals **118** and **122**. More particularly, a current amplifier **124** supplies a base drive to each of the transistors **108** and **112**, a current amplifier **126** supplies a base drive to the transistor **114**, and a current amplifier **128** supplies a base drive to the transistor **110**. Accordingly, the base drive for all of the transistors is not derived from the voltage source designated V+ and V−, but is derived from the amplifiers **124, 126**, and **128**. Since the voltage gain of each of the amplifiers **124, 126** and **128** is unity, the voltage developed across the terminals **118** and **122** will not be affected thereby.

It can be appreciated that the circuit illustrated in FIG. **2** can also be employed as a current regulator, a voltage regulator and a buffer amplifier, Furthermore, the circuits illustrated in FIGS. **1** and **2** can be employed to provide a variety of input and output characteristics by controlling the values of the resistors **26–32** and the resistors **54–60**.

The Invention claimed is:

1. A circuit disposed for connection to an input supply for providing an output which is independent of that supply, comprising

a plurality of transistors, and

means responsive to the input supply for generating a base-emitter voltage on all of said transistors,

the base-emitter junctions of said transistors being connected serially in a loop with one another, such that the summation of the base-emitter voltages of said transistors is developed as an output voltage between the base-emitter junctions of two adjacent ones of said transistors in said loop,

the collector currents of any of said transistors having their collector-emitter circuits connected in series being equal to one another and their base-emitter

voltages opposing one another around said loop, such that said summation of the base-emitter voltages is independent of the collector currents of said transistors and only proportional to the difference of the emitter areas of said transistors.

2. The circuit of claim **1,** wherein the emitter areas of at least two of said transistors are different from one another.

3. The circuit of claim **2,** wherein said output voltage is proportional to the difference of the emitter areas of said transistors.

4. The circuit of claim **3,** further comprising a resistor connected between the base-emitter junctions of said two adjacent transistors, such that said output voltage is developed on said resistor, and wherein the current through said resistor is available at the collector of one of said transistors as an output.

5. The circuit of claim **3,** further comprising a resistor connected between the base-emitter junctions of said two adjacent transistors, such that said output voltage is developed on said resistor, and wherein the current through one of said transistors is proportional to the value of said resistor.

6. The circuit of claim **1,** wherein said plurality of transistors includes a first pair of transistors having their collector-emitter circuits connected in series and a second pair of transistors having their collector-emitter circuits connected in series, and wherein said generating means includes a first connection from the junction between said first pair of transistors to the base of a first one of said second pair of transistors, a second connection from the junction between said second pair of transistors to the base of a first one of said first pair of transistors, and a third connection between the base of a second one of said first pair of transistors to the base of a second one of said second pair of transistors.

7. The circuit of claim **6,** wherein said generating means further includes a fourth connection from the collector of one of said second transistors to its base.

8. The circuit of claim **7,** wherein said generating means further includes a plurality of current amplifiers, one in each of said first, second and third connections.

9. The circuit of claim **8,** wherein the collectors of said second transistors are disposed for connection to one side of the input supply and the emitter of one of said first transistors is disposed for connection through an input voltage source to the other side of the input supply.

10. A four terminal network, comprising a. a first pair of transistors having their collector-emitter circuits connected in series between a first pair of terminals,

b. a second pair of transistors having their collector-emitter circuits connected in series between a second pair of terminals,

c. a connection from one of the first pair of terminals to the base of a first one of said first pair of transistors and to the base of a first one of said second pair of transistors,

d. a connection from the junction of said first pair of transistors to the base of a second one of said second pair of transistors, and

e. a connection from the junction of said second pair of transistors to the base of a second one of said first pair of transistors.

11. The network of claim **10,** further comprising a resistor connected in the emitter circuit of one of said transistors.

12. The network of claim **11,** wherein said resistor is connected between said first pair of transistors.

13. The network of claim **11,** wherein said resistor is connected between said second pair of transistors.

14. The network of claim **11,** wherein said resistor is connected between the emitter of said second one of said first pair of transistors to a second one of the first pair of terminals.

15. The network of claim **11,** wherein said resistor is connected between the emitter of said second one of said second pair of transistors to one of the second pair of terminals.

16. The network of claim **10,** further comprising an amplifier in each of said connections.

* * * * *