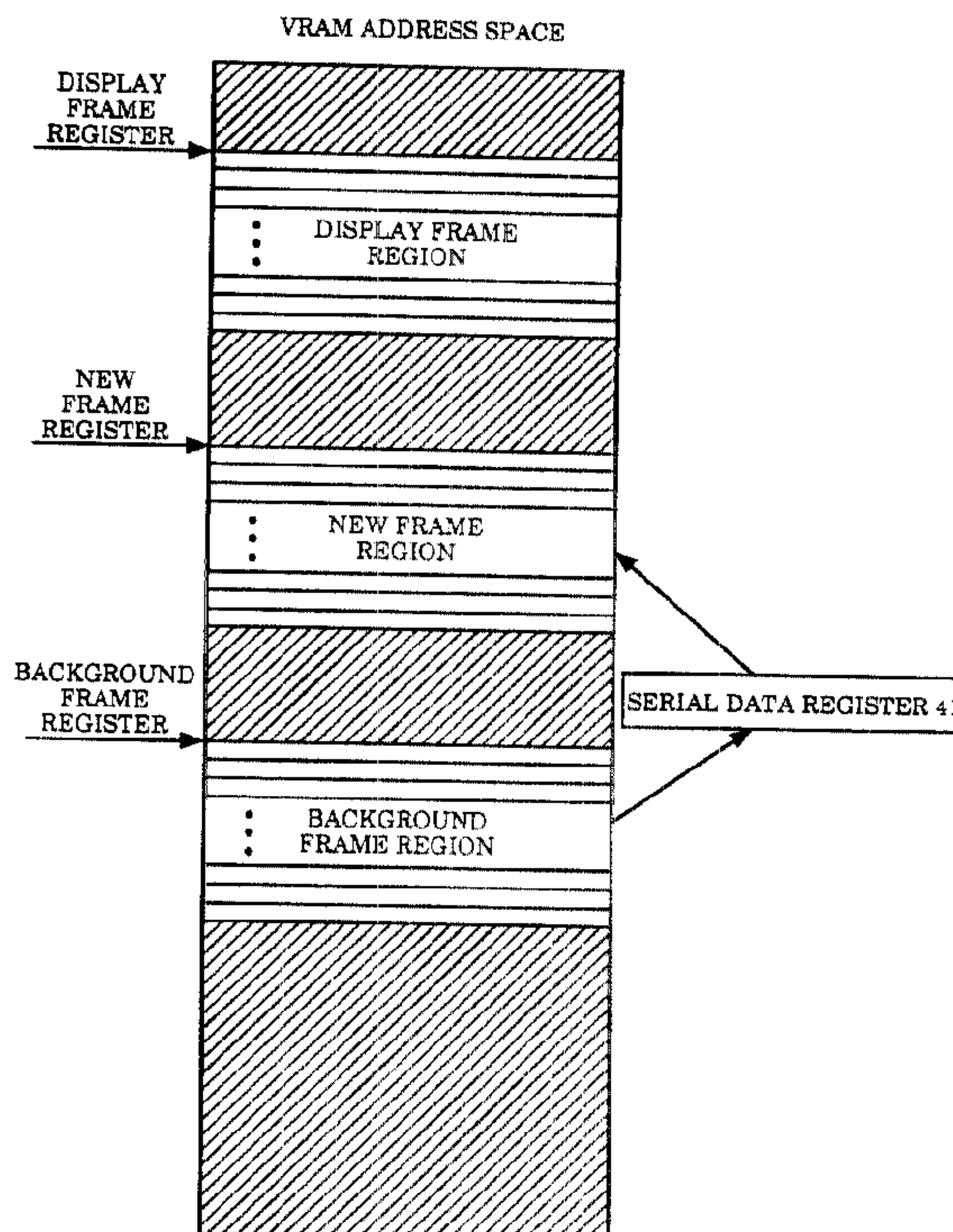




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(54) Titre : METHODE ET APPAREIL POUR CONSTRUIRE UNE MEMOIRE A IMAGES A FONCTION DE
 DUPLICATION RAPIDE
 (54) Title: METHOD AND APPARATUS FOR CONSTRUCTING A FRAME BUFFER WITH A FAST COPY MEANS



(57) **Abrégé/Abstract:**

A method and apparatus for quickly copying a first frame region into a second frame region. A video memory array comprising a plurality of video random access memory devices is divided into at least two frame regions. A background image is rendered by a central processing unit into a background frame region within the video memory array. The central processing unit then requests the background image in the background frame region to be copied into a new frame region in the video memory array. A dedicated circuit copies the entire background image in the background frame region into the new frame region. The dedicated circuit operates by using a serial data register within each video random access memory device during the vertical retrace period of a video timing signal. The dedicated circuit performs the background frame copy without requiring any processing resources from the central processing unit,

ABSTRACT OF THE INVENTION

A method and apparatus for quickly copying a first frame region into a second frame region. A video memory array comprising a plurality of video random access memory devices is divided into at least two frame regions. A background image is rendered by a central processing unit into a background frame region within the video memory array. The central processing unit then requests the background image in the background frame region to be copied into a new frame region in the video memory array. A dedicated circuit copies the entire background image in the background frame region into the new frame region. The dedicated circuit operates by using a serial data register within each video random access memory device during the vertical retrace period of a video timing signal. The dedicated circuit performs the background frame copy without requiring any processing resources from the central processing unit.

BACKGROUND OF THE INVENTION

1. Field of the Invention:

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This invention relates to the field of frame buffers for computer systems. More particularly, to a method and apparatus for quickly copying information from a first region of memory in a frame buffer to a second region of memory in the frame buffer.

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2. Art Background:

Many computer systems use a region of memory called a frame buffer for storing data that is to be displayed on a graphics display screen. A display control system reads the information in the frame buffer line-by-line, converts the information into an analog video signal using a digital to analog converter (DAC), and transmits the analog video signal to a display screen. The line-by-line scanning generally beginning at a region in the frame buffer corresponding to the upper left-hand corner of the display screen and continuing to the lower right-hand corner.

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Typically, a frame buffer is constructed of video random access memory (VRAM) devices that differ from conventional dynamic random access memory (DRAM) devices by having two access ports instead of just one access port. A first access port, called a random access port, provides conventional random access to the VRAM such that a central processing unit

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coupled to the VRAM may read or write to any memory location in the VRAM. A second port, called a serial access port, provides simultaneous serial access to the VRAM such that a device coupled to the serial port can shift data in or out of the VRAM. A display circuit usually accesses the serial port to furnish pixel data to the circuitry controlling the output display. In such a configuration, a central processing unit can write to the VRAM while a display circuit continually furnishes information to an output display.

To animate objects on a display screen coupled to a frame buffer based display system, animation software renders a series of frames with slight picture changes in each frame. To provide smooth animation, approximately 15 to 30 new frames should be displayed each second. As the picture in one frame changes to the picture in the next frame, continuous motion is presented. To accomplish this, the frame buffer must be continually updated.

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The ability of a frame buffer to both receive information and transfer that information to an output display simultaneously causes certain difficulties. If the animation software writes to frame buffer memory while the display controller is scanning the image in the frame buffer memory to a display, then the display may present information from more than one animation frame at time. This problem is referred to as frame tear. Frame tears are only important where motion from one frame to the next causes the elements presented on the display to be obviously distorted. When this occurs, the distortion caused may be extremely disconcerting to the viewer.

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To eliminate frame tears, certain computer systems utilize a system referred to as double buffering. A double buffered system provides two regions of memory in the frame buffer wherein each region of memory may furnish pixel information to the circuitry controlling the output display. A first region of memory provides a first animation frame to the output display, and no changes are made in that memory region while it provides information to the display screen. While the first memory region is displayed on the display screen, animation software renders the next animation frame in the second region of memory. When the animation software completes the next animation frame the display is changed such that the second region of memory becomes the displayed frame and the first region of memory becomes the "work" region in which the animation software renders the next animation frame. In this manner, no pixel information is ever written to the region of memory that is displayed on the display screen. The effect of writing to the non-displayed buffer is that frame tears cannot occur.

When animating objects using a double-buffered animation frame, the CPU must render every object to be displayed in the work region for each new frame of animation. If the animated objects are being rendered on top of a background scene, the entire background scene must also be redrawn by the CPU before it can render the animated objects. To provide high-quality real time animation, the rendering of the background and the animated objects for an animation frame must be done approximately 15 to 30 times per second. Real-time animation therefore usually requires a very fast computer processor.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an improved display control system that reduces the amount of processor speed required to provide real-time animation. The present invention accomplishes this object by providing a method and apparatus for copying an entire background image frame from a background region of memory in a frame buffer into a new frame region of memory in the frame buffer. The apparatus operates when requested by the central processing unit of the computer system. The central processing unit requests a background copy by setting a new frame register in the copy apparatus to point to an empty region of memory and setting a bit in a control register. The apparatus of the present invention performs the background copy without requiring any processing resources from the central processing unit.

Accordingly, in one of its aspects, the present invention provides a method for generating and displaying a sequence of animation frames, said method for use with a frame buffer apparatus comprising at least three data regions, each of the data regions having contents comprising frame data, and said frame buffer apparatus further comprising a display region pointer, a background region pointer, and a new frame region pointer, said method comprising the following steps:

displaying, on a video display device, the contents of the data region addressed by the display region pointer; copying the contents of the data region addressed by the background region pointer into the data region addressed by the new frame region
5 pointer; rendering a next frame in the sequence of animation frames; overlaying the next frame onto the data region addressed by the new frame region pointer; resetting the display region pointer to identify the data region addressed by the new frame region pointer; resetting the new frame region pointer to identify the data region previously addressed by the display region pointer; iteratively repeating the
10 foregoing steps until the sequence of animated frames has been completely displayed on the video display device.

In a further aspect, the present invention provides an apparatus for generating and displaying a sequence of animation frames, said apparatus comprising: a frame
15 buffer apparatus comprising at least three data regions, each of the data regions having contents comprising frame data, and the frame buffer apparatus further comprising a display region pointer, a background region pointer, and a new frame region pointer; means for displaying, on a video display device, the contents of the data region addressed by the display region pointer; means for copying the contents

of the data region addressed by the background region pointer into the data region addressed by the new frame region pointer; means for rendering a next frame in the sequence of animation frames; means for overlaying the next frame onto the data region addressed by the new frame region pointer; means for resetting the display
5 region pointer to identify the data region addressed by the new frame region pointer; means for resetting the new frame region pointer to identify the data region previously addressed by the display region pointer; means for iteratively repeating the foregoing steps until the sequence of animated frames has been completely displayed on the video display device.

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In a still further aspect, the present invention provides in a computer system, a frame buffer apparatus for copying video information, said frame buffer apparatus comprising: a video memory array divided into at least three frame regions including a first frame region associated with a background display image frame, a
15 second frame region associated with a future display image frame, and a third frame region associated with a current display image frame, said video memory array including at least one video random access memory device having a plurality of memory locations and a data register capable of loading and storing a row of said memory locations in said video random access memory device; and a copy
20 apparatus coupled to said video memory array including means for loading and

storing a plurality of rows of said memory locations using said data register in each video random access memory device to copy said background display image frame in said first frame region in said video memory array to said future display image frame in second frame region in said video memory array, wherein said copy apparatus does not copy data to the third frame region while associated with a current display image frame.

In a further aspect, the present invention provides in a computer system, a frame buffer apparatus for managing image frames, said frame buffer apparatus comprising: a video memory array divided into a first frame region associated with first display image frame, a second frame region associated with second display image frame, and a third frame region associated with third display image frame, said video memory array including at least one video random access memory device having a plurality of memory locations and a serial data register capable of loading and storing a row of said memory locations in said video random access memory device; a copy apparatus coupled to said video memory array, said copy apparatus including means for loading and storing a plurality of rows of said memory; a background frame register storing a pointer to one of the frame regions in said video memory array; a future frame register storing a pointer to one of the frame regions in said video memory array; locations using said data register in each video memory

device to copy contents in said frame region pointed to by the background frame register to said frame region pointed to by the future frame register; a display frame register storing a pointer to one of the frame regions in said video memory array; and a video display circuit including means for loading rows of memory from the frame region pointed to by said display frame register into said serial data register and shifting said rows of memory out through a serial access port connected to serial data register.

In a further aspect, the present invention provides in a computer system, a frame buffer apparatus for copying information, said frame buffer apparatus comprising: memory means divided into at least three frame regions, a first frame region associated with a background display image frame, a second frame region associated with a future display image frame, and a third frame region associated with a current display image frame, said memory means having a plurality of memory locations and a data register capable of loading and storing a row of said memory locations in said memory means; and copy means coupled to said memory means, said copy means including means for loading and storing a plurality of rows of said memory locations using said data register in said memory means to copy said background display image frame in first frame region in said memory means to said future display image frame in said second frame region in said memory means,

wherein said copy means does not copy data to the third frame region while associated with a current display image frame.

In a still further aspect, the present invention provides a method of copying
5 video information with a frame buffer apparatus in a computer system including a
video memory array having at least one random access memory device with a
plurality of memory locations and a serial data register, said method comprising:
dividing said video memory array into a first frame region associated with a
background display image frame, a second frame region associated with a future
10 display image frame, and a third frame region associated with a current display
image frame; copying contents in the first frame region to the second frame region
by loading and storing a plurality of rows of said memory locations in each random
access memory device using said serial data register; and changing an association of
the current display image frame from the third frame region to one of the first and
15 second frame regions.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features, and advantages of the present invention will be apparent to one skilled in the art in view of the following detailed
5 description in which:

FIGURE 1 illustrates a conventional video random access memory device (VRAM).

10 **FIGURE 2** illustrates a block diagram of a conventional computer display system that uses a frame buffer comprised of VRAM.

FIGURES 3a and 3b illustrate how a video signal scans down a display screen.

15 **FIGURE 4** illustrates a block diagram of the computer display system of the present invention.

FIGURE 5 illustrates a memory map of the VRAM address space
20 as used by the display control system of the present invention.

FIGURE 6 illustrates a flow diagram of the display logic in the display control system of the present invention.

25 **FIGURE 7** illustrates a flow diagram of the background copy logic in the display control system of the present invention.

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FIGURES 8a through 8m illustrate how the display control system of the present invention is used to produce real time animation.

NOTATION AND NOMENCLATURE

The detailed descriptions that follow are presented largely in terms of algorithms and symbolic representations of operations on data bits within a computer memory. These algorithmic descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art.

An algorithm is here, and generally, conceived to be a self-consistent sequence of steps leading to a desired result. These steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It proves convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like. It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities.

Further, the manipulations performed are often referred to in terms, such as adding or comparing, which are commonly associated with mental operations performed by a human operator. No such capability of a human operator is necessary, or desirable in most cases, in any of the operations described herein that form part of the present invention; the

operations are machine operations. Useful machines for performing the operations of the present invention include general purpose digital computers or other similar devices. In all cases there should be borne in mind the distinction between the method operations in operating a computer and the
5 method of computation itself. The present invention relates to method steps for operating a computer in processing electrical or other (e.g., mechanical, chemical) physical signals to generate other desired physical signals.

The present invention also relates to apparatus for performing
10 these operations. This apparatus may be specially constructed for the required purposes or it may comprise a general purpose computer as selectively activated or reconfigured by a computer program stored in the computer. The algorithms presented herein are not inherently related to a particular computer or other apparatus. In particular, various general purpose machines
15 may be used with programs written in accordance with the teachings herein, or it may prove more convenient to construct more specialized apparatus to perform the required method steps. The required structure for a variety of these machines will appear from the description given below.

DETAILED DESCRIPTION OF THE INVENTION

A computer display system with a fast copy means is disclosed. In the following description, for purposes of explanation, specific nomenclature such as icons, displays, cursors, reticle, etc. is set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention. In other instances, well known circuits and devices are shown in block diagram form in order not to obscure the present invention unnecessarily.

A Video Random Access Memory

Referring to Figure 1, a simplified block diagram of a typical Video Random Access Memory (VRAM) device is illustrated. In the center of the VRAM is a dynamic random access memory array 35 that is used to store data. The RAM array 35 is organized into a set of rows and columns such that each memory location in the RAM array 35 is defined by a row address and a column address. The memory in the RAM array 35 of Figure 1 can be accessed by two different access ports: a random access port 21 and a serial access port 23.

The random access port 21 is usually used by a central processing unit (CPU) (not shown) in a computer system to read and write to the video memory. The CPU generates images on a display screen by writing image patterns in the VRAM array 35 through the random access port 21. To access a specific memory location in the VRAM array 35, the CPU first generates an

address that is latched in through the address lines 49. The address is split into a row address and a column address. The row decoder 39 and column decoder 37 use the row address and column address to access a specific memory location in the RAM array 35. The CPU then either writes data to the input buffer 27 or
5 reads data from output buffer 25 depending upon if the memory access is a write access or a read access.

The serial access port 23 of the VRAM is usually used by a display control system (not shown) in a computer system to read the image in the
10 VRAM and send the image to a display. The display control system accesses the data in the video memory by first providing a row address to the address input 49 and requests the VRAM to transfer the entire memory row into the serial data register 41. The row decoder 39 selects a row in the RAM array 35 using the row address and transfers the selected row into the serial data register
15 41. The display control system then has the VRAM shift the data in the serial data register 41 out through serial output buffer 29 to the serial access port 23. A digital-to-analog converter (not shown) connected to the serial access port 23 uses the data to generate a video signal. The analog video signal drives a computer display.

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In some devices that use VRAMs, such as a video frame grabber, the serial access port 23 is used as an input port instead of an output port. Such devices shift video information that has been converted into digital data into the serial data register 41 through serial input buffer 31. The device then
25 provides a destination row address to the address input 49. The VRAM writes the digital information in the serial data register 41 into a row of the RAM

array 35 selected by the row decoder 39 using the destination row address. Thus the serial data register 41 can be used to write data into the video memory array 35 as well as read information out of the video memory array 35.

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A Conventional Display Control System

Figure 2 illustrates a typical prior art computer display system.

The computer display system comprises a central processing unit (CPU) 53, a display control system 51, a VRAM array 55, a digital to analog converter (DAC) 69, and a display screen 71. The VRAM array 55 comprises a number of individual VRAM devices, such as the VRAM device disclosed in Figure 1, as is well known in the art.

The main component of the computer display system illustrated in Figure 2 is the display control system 51. The display control system 51 is coupled to the CPU 53 such that the CPU 53 can control the display control system 51 using a set of memory-mapped control registers. The display control system 51 is comprised of two main logic units: the display logic 66 and the VRAM arbitration logic 67.

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The display logic 66 accesses a logically rectangular region of memory in the VRAM array 55 that defines an image to display on the display screen 71. The display frame register 61 contains the starting address of the frame region within the VRAM array 55. The display logic 66 generates a video timing signal 72. The display logic 66 uses the display frame register 61 to access the frame region in the VRAM array 55 in synchronization with the

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video timing signal 72. The display logic 66 shifts the data describing an image out of the VRAM array 55 through the serial access port 23 to a digital-to-analog converter (DAC) 69. The display logic 66 also provides the video timing signal 72 to the digital-to-analog converter (DAC) 69.

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The digital-to-analog converter (DAC) 69 combines the video timing signal 72 and the image data shifted out of the VRAM array 55 to generate an analog video signal. The analog video signal drives a computer display 71.

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The VRAM arbitration logic 67 in the display control system 51 arbitrates between VRAM access requests from the CPU 53 and the display logic 66. The VRAM arbitration logic 67 gives the display logic 66 priority such that if there is a conflict, the display logic 66 gets to access the VRAM array 55. Since the display logic 66 must provide information from the VRAM in synchronization with the video timing signal 72, the VRAM arbitration logic 67 gives priority to the display logic 66.

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Display Control System with Fast Frame Copy

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Figures 3a and 3b provide a simplified conceptual illustration of a video signal scanning down a video display screen. Referring to Figure 3a, a video signal scans the display screen starting from the upper left corner. The video signal scans a line of information as it moves left to right across each horizontal scan line 91. At the end of each scan line, a horizontal retrace 93 moves the video signal back to the left side of the display screen. When the

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video signal reaches the bottom of the display, a vertical retrace 95 moves the video signal back to the top of the display screen.

During the time periods that the video signal is executing a
5 horizontal retrace 93 or a vertical retrace 95 no data is displayed on the display. Therefore, during the horizontal retrace and vertical retrace periods the display logic 66 in a typical display control system 51 does not access the VRAM array 55. Since the display control system 51 does not access the VRAM during the retrace periods, another device can use the serial data register 41, as illustrated
10 Figure 1, during the retrace periods.

In the preferred embodiment, the present invention uses the serial data register 41 in each VRAM during the vertical retrace to copy the entire contents of a first memory region in the frame buffer to a second
15 memory region. The display control system performs the memory region copy without using the central processing unit. In this manner, the central processing unit can be used for other matters such as rendering animated objects. The computer display system of the present invention will be described with reference to Figures 4, 5, 6, and 7.

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Figure 4 illustrates a block diagram of computer display system utilizing the teachings of the present invention. The computer display system illustrated in Figure 4 is similar to computer display system of Figure 2, except that a new frame register 62, a background frame register 63, a control register
25 64, and background copy logic 65 have been added.

The background frame register 63 is set by the CPU 53 to point to a region of memory within the VRAM array 55 containing background scene. The new frame register 62 is set by the CPU 53 to point to a "work" region in which the next frame of animation is created by the CPU 53 when performing double buffered animation. The work region is referred to as the new frame region. When requested by the CPU 53, the background copy logic 65 copies the entire rectangular region of memory defining a background pointed to by the background frame register 63 to the new frame region pointed to by the new frame register 62 during a retrace period of the video signal.

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The control register 64 is used to perform several different functions. Within the control register 64 is a copy control bit. The copy control bit is set by the CPU 63 when the program needs a background copy performed. The control register 64 is also used to enable or disable a pair of interrupts. The first interrupt controlled by the control register 64 is the vertical retrace interrupt. If the vertical retrace interrupt is enabled, the vertical retrace interrupt generates a CPU interrupt when the vertical retrace period begins. The second interrupt controlled by the control register 64 is the copy complete interrupt. If the copy complete interrupt is enabled, the copy complete interrupt generates a CPU interrupt when a background copy performed by the background copy logic is complete. The vertical retrace interrupt and the copy complete interrupt are used by animation rendering programs such that the animation rendering programs can synchronize with the background copy operation.

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The background copy operation is best explained with the use of a flow diagram and a memory map. Referring to Figure 5, a memory map of the VRAM array 55 address space is illustrated. In the memory map of Figure 5, the display frame register 61, a new frame register 62, and a background frame register 63 each point to a display frame region, a new frame region, and a background frame region within the VRAM address space, respectively. The display frame region contains the frame that is currently being displayed on the display screen. The new frame region contains an animation frame that is currently under construction and will be displayed in the future. The background region contains the background scenery for the animation. The contents of the background region is copied into the new frame region before each animation frame is rendered. There may be more than one background region in memory such that several different background scenes may be available. The animation sets the background frame register to choose between several background scenes. The display frame region, the new frame region, and the background frame region are all aligned in memory.

Figure 6 provides a flow diagram that explains how the display logic 66 in the display control system 51 of the present invention operates. Referring to step 101 at the top of the flow diagram in Figure 6, the display logic 66 first loads the serial data pointer 45 (of Figure 1) in the VRAM with the contents of the display frame register 61 such that the serial data pointer 45 points to the first line in the display frame region. Next, in step 102, the display logic 66 loads the serial data register 41 with some or all of the first horizontal line. At step 103, the display logic 66 shifts the horizontal line data in the serial data register 41 out of the VRAM array 55 and into the digital-to-analog

converter (DAC). (As indicated by step 104, steps 102 and 103 may be repeated if the entire horizontal display line was not shifted out to the display.) At step 105, the display logic 66 tests to see if the bottom of the display frame has been reached. If the bottom of the display frame has not been reached the display logic 66 waits for the horizontal retrace to complete and then goes back to step 102. The display logic 66 repeats steps 102, 103, 105, and 107, until all the horizontal rows of data have been shifted out of the VRAM array 55 and into the digital-to-analog converter (DAC) thereby displaying a full frame.

10 After the display logic 66 reaches the bottom of the display frame, the display logic generates a vertical retrace interrupt at step 108 if the vertical retrace interrupt is enabled. Next, the display logic 66 tests the copy control bit in the control register 64 at step 109. If the copy control bit in the control register 64 is set, the display control system 51 invokes the background copy logic 65 at step 113. After the background copy has been performed, the display logic 66 generates the copy complete interrupt at step 114 if the copy complete interrupt is enabled. The copy complete interrupt informs the CPU that copy operation has completed. Finally, the display logic 66 waits at step 115 until the vertical retrace period completes and then begins shifting out another frame to the DAC 69.

The background copy at step 113 is performed by the background copy logic 65. Figure 7 provides a flow diagram that explains the operation of the background copy logic 65.

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Referring to step 131 of Figure 7, the background copy logic 65 first clears a counter 68 that will be used in the copy process. The background copy logic 65 next loads the serial data register 41 (of Figure 1) in a VRAM with a first portion of the background scene at step 135. To obtain a first portion of the background scene, the copy logic 65 creates an address that has the same upper bits of the background frame register 63 and lower bits created from the counter 68. At step 137, the background copy logic 65 then stores the background scene information in the serial data register 41 (of Figure 1) into the new frame region. To store the information in the new frame region, the copy logic 65 creates an address that has the same upper bits of the new frame register 62 and lower bits created from the counter 68. The counter 68 is thereby used as an index into both background region and the new frame region. At steps 138 and 139, the background copy logic 65 tests the counter 68 to see if the background copy logic 65 has copied the entire frame region. If background copy logic 65 has not copied the entire frame region, the counter 68 is increased at step 141 and the background copy logic 65 goes back to step 135. The background copy logic 65 continues copying information from the background region into the new frame region using the counter 68 as an index until the frame copy has completed. The background copy logic therefore copies the contents of the background region into the new frame region row by row using the serial data register 41 (of Figure 1) as illustrated in Figure 5. When the background copy logic 65 reaches the bottom of the new frame region and the background region, the background copy logic 65 is done with the background copy.

In an alternate embodiment, the background copy can be performed during the horizontal retrace periods 93 as illustrated in Figure 3a

or during both vertical and horizontal retrace periods. When using the horizontal retrace periods, the background copy logic 65 copies a small portion of the background region into the new frame region during each horizontal retrace period 93 such that the background region is copied into the new frame region piece by piece during successive horizontal retraces. After each portion is copied, the background copy logic 65 must be sure the restore state of the VRAMs in the VRAM array such that the display logic 66 is not disturbed as it scans down the display. For example, the value in the serial data register 41 and the serial data pointer 45 (in Figure 1) should be restored.

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Frame Buffer with Fast Copy Controller Used for Animation

The computer display system of the present invention is ideal for improving the performance of double-buffered animation that is rendered over background scenery. Figures 8a through 8k illustrate how an animation program can use the present invention to render fast double-buffered animation. In each figure, the contents of the display frame register 61, new frame register 62, and background frame register 63 are represented as pointers on the left side of the figure. The contents of the display frame region, new frame region, and background frame region are presented as images that are pointed to by the display frame register 61, new frame register 62, and background frame register 63 respectively.

The first step is to initialize the three sets of registers and memory regions that will be used. Referring to Figure 8a, the VRAM address space is cleared to provide a black background and the display frame register 61 and the

background frame register 63 are initialized to point to a display frame region and a background frame region respectively within the VRAM 55. The new frame register 62 is set to null since it is not yet needed. The display screen 71 always displays the display frame region pointed to by the display frame register 61. Currently, the display frame register 61 points to a cleared-out display frame region so the screen display 71 is blank.

The next step is to create the background scene that will be used as the backdrop for the animation. Figure 8b illustrates the contents of the memory regions after a background mountain scene has been rendered in the background frame region. The mountain scene in the background frame region will be used to provide a background for the animation. The display screen 71 remains blank since the display frame register 61 still points to an empty display frame region.

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To begin rendering an animation frame, the animation software requests the display control system 51 of the present invention to copy the contents of the background frame region into a new frame region by setting the new frame register 62 to point to an unused region of memory and setting the copy control bit in the control register 64. The display control system 51 then copies the image in the background frame region into the new frame region. Figure 8c illustrates the contents of the memory regions after the display control system 51 performs the background copy.

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The animation software now renders the first frame of animation over the background scene in the new frame region. Figure 8d illustrates the

contents of the memory regions after the animation software has rendered an airplane on the mountain background scene.

5 To display the first animation frame, the animation software sets the contents of the display frame register 61 to point to the memory region that contains the airplane. Figure 8e illustrates the contents of the memory regions after the display frame register 61 has been set to point to the first animation frame.

10 To generate the second animation frame, the animation software first requests the display control system 51 of the present invention to copy the background scene into an unused region of memory. The animation software performs the request by changing the new frame register 62 to point to the old (and now unused) display frame region and sets the copy control bit in the control register 64. The old display region therefore becomes the new frame
15 region. Figure 8f illustrates the contents of the memory regions after the display control system 51 copies the background scene from the background region into the new frame region.

20 The animation software now renders the second frame of animation in the new frame region on top of the background scene. In the second animation frame, the airplane should move along the mountain background scene. The animation software therefore renders the airplane moved a little to the left. Figure 8g illustrates the contents of the memory
25 regions after the animation software has rendered the second animation frame.

To display the second animation frame, the animation software sets the contents of the display frame register 61 to point to the memory region with the moved airplane. Figure 8h illustrates the contents of the frame buffers after the display frame register 61 has been set to point to the second animation frame.

To generate the third animation frame, the animation software requests the display control system 51 of the present invention to copy the background scene into an unused region of VRAM memory. The animation software performs the request by changing the new frame register 62 to point to the previous display frame region. The old display region therefore becomes the new frame region. Figure 8i illustrates the contents of the memory regions after the display control system 51 copies the background scene from the background region into the new frame region. Note that the background copy logic 65 overwrites the first frame of animation that was in that region of memory.

The animation software now renders the third frame of animation in the new frame region on top of the background scene. In the third animation frame, the airplane crashes into the mountains. The animation software therefore renders a crashed airplane on the background mountain scene. Figure 8j illustrates the contents of the memory regions after the animation software has rendered the third animation frame.

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To display the third animation frame, the animation software sets the contents of the display frame register 61 to point to the memory region with the crashed airplane. Figure 8k illustrates the contents of the memory regions after the display frame register 61 has been set to point to the third
5 animation frame.

Since it is unlikely that the crashed airplane will move in the future, the crashed airplane can become part of the background scene for future animation frames. The animation software therefore makes the airplane crash scene into the new background scene by setting the background frame register
10 63 to point to the region of memory that contains the airplane crash scene. Figure 8l illustrates the contents of the memory regions after the airplane crash scene has been made the background scene.

15 To generate a fourth animation frame, the animation software requests the display control system 51 to copy the background scene into an unused region of memory. The animation software performs the request by changing the new frame register 62 to point to an unused region of memory and then sets the copy control bit in the control register 64. Since the crashed
20 airplane will probably be a permanent fixture of the background scene, the previous mountain scene can be destroyed. Therefore the previous background region becomes the new frame region. Alternatively, the animation software could have used a new region of memory and saved the original mountain scene for future use. Figure 8m illustrates the contents of
25 the memory regions after the display control system 51 copies the background scene from the background region into the new frame region. Note that the

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background copy logic 65 overwrites the old background scene that was in that region of memory.

The animation software continues rendering successive
5 animation frames by changing the new frame register 62 to point to an unused region of memory to create a new frame in which to render an animation frame. After rendering the animation frame in that region of memory, the software changes the display frame register 61 to point to the newly rendered frame.

10

The foregoing has described a computer display system with a fast frame copy means. It is contemplated that changes and modifications may be made by one of ordinary skill in the art, to the materials and arrangements of elements of the present invention without departing from the spirit and scope
15 of the invention.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A method for generating and displaying a sequence of animation frames, said method for use with a frame buffer apparatus comprising at least three data regions, each of the data regions having contents comprising frame data, and said frame buffer apparatus further comprising a display region pointer, a background region pointer, and a new frame region pointer, said method comprising the following steps:

displaying, on a video display device, the contents of the data region addressed by the display region pointer;

copying the contents of the data region addressed by the background region pointer into the data region addressed by the new frame region pointer;

rendering a next frame in the sequence of animation frames;

overlaying the next frame onto the data region addressed by the new frame region pointer;

resetting the display region pointer to identify the data region addressed by the new frame region pointer;

resetting the new frame region pointer to identify the data region previously addressed by the display region pointer;

iteratively repeating the foregoing steps until the sequence of animated frames has been completely displayed on the video display device.

2. The method of claim 1 wherein the step of displaying includes one or more video retrace periods, and the respective steps of copying, rendering, and overlaying are performed during said video retrace periods.

3. The method of claim 2 wherein said one or more video retrace periods include a vertical video retrace period.

4. The method of claim 2 wherein said one or more video retrace periods include a horizontal video retrace period.

5. The method of claim 1, wherein the step of resetting the new frame region pointer is replaced by the following steps:

resetting the background region pointer to address the data region addressed by the display region pointer, thereby updating the contents of the region addressed by the background region pointer; and

resetting the new frame region pointer to address the data region previously addressed by the background region pointer.

6. An apparatus for generating and displaying a sequence of animation frames, said apparatus comprising:

a frame buffer apparatus comprising at least three data regions, each of the data regions having contents comprising frame data, and the frame buffer apparatus further comprising a display region pointer, a background region pointer, and a new frame region pointer;

means for displaying, on a video display device, the contents of the data region addressed by the display region pointer;

means for copying the contents of the data region addressed by the background region pointer into the data region addressed by the new frame region pointer;

means for rendering a next frame in the sequence of animation frames;

means for overlaying the next frame onto the data region addressed by the new frame region pointer;

means for resetting the display region pointer to identify the data region addressed by the new frame region pointer;

means for resetting the new frame region pointer to identify the data region previously addressed by the display region pointer;

means for iteratively repeating the foregoing steps until the sequence of animated frames has been completely displayed on the video display device.

7. The apparatus of claim 6 wherein the means for displaying include means for generating one or more video retrace periods, and the respective means for copying, rendering, and overlaying are operative during said video retrace periods.

8. The apparatus of claim 7 wherein said one or more video retrace periods include a vertical video retrace period.

9. The apparatus of claim 7 wherein said one or more video retrace periods include a horizontal video retrace period.

10. The apparatus of claim 6, wherein the means for resetting the new frame region pointer are replaced by the following means:

means for resetting the background region pointer to address the data region addressed by the display region pointer, thereby updating the contents of the region addressed by the background region pointer; and

means for resetting the new frame region pointer to address the data region previously addressed by the background region pointer.

11. In a computer system, a frame buffer apparatus for copying video information, said frame buffer apparatus comprising:

a video memory array divided into at least three frame regions including a first frame region associated with a background display image frame, a second frame region associated with a future display image frame, and a third frame region associated with a current display image frame, said video memory array including at least one video random access memory device having a plurality of memory locations and a data register capable of loading and storing a row of said memory locations in said video random access memory device; and

a copy apparatus coupled to said video memory array including means for loading and storing a plurality of rows of said memory locations using said data register in each video random access memory device to copy said background display image frame in said first frame region in said video memory array to said future display image frame in second frame region in said video memory array, wherein said copy apparatus does not copy data to the third frame region while associated with a current display image frame.

12. The frame buffer apparatus as claimed in claim 11 wherein said frame buffer apparatus generates a video timing signal, said video timing signal having a vertical

retrace period, and said copy apparatus operates only during said vertical retrace period.

13. The frame buffer apparatus as claimed in claim 11 wherein said frame buffer apparatus generates a video timing signal, said video timing signal having a horizontal retrace period, and said copy apparatus operates only during said horizontal retrace period.

14. The frame buffer apparatus as claimed in claim 11 wherein said frame buffer apparatus includes

means for generating a video timing signal having a vertical retrace period and a horizontal retrace period, and,

wherein said copy apparatus includes

means for only operating during at least one of said vertical retrace period and said horizontal retrace period.

15. The frame buffer apparatus as claimed in claim 12 wherein said data register that can load and store a row of said memory locations in said video random access memory device comprises a serial data register coupled to serial access port.

16. In a computer system, a frame buffer apparatus for managing image frames, said frame buffer apparatus comprising:

a video memory array divided into a first frame region associated with first display image frame, a second frame region associated with second display image frame, and a third frame region associated with third display image frame, said video memory array including at least one video random access memory device having a plurality of memory locations and a serial data register capable of loading and storing a row of said memory locations in said video random access memory device;

a copy apparatus coupled to said video memory array, said copy apparatus including

means for loading and storing a plurality of rows of said memory;

a background frame register storing a pointer to one of the frame regions in said video memory array;

a future frame register storing a pointer to one of the frame regions in said video memory array;

locations using said data register in each video memory device to copy contents in said frame region pointed to by the background frame register to said frame region pointed to by the future frame register;

a display frame register storing a pointer to one of the frame regions in said video memory array; and

a video display circuit including

means for loading rows of memory from the frame region pointed to by said display frame register into said serial data register and shifting said rows of memory out through a serial access port connected to serial data register.

17. The frame buffer apparatus as claimed in claim 16 wherein said frame buffer apparatus further comprises:

a background frame register, said background frame register pointing to a background frame region in said video memory array containing a background image;

a new frame register, said new frame register pointing to a new frame region in said video memory array; and

wherein said copy apparatus copies from said background frame region to said new frame region.

18. The frame buffer apparatus as claimed in claim 17 wherein said frame buffer apparatus further comprises a copy control bit and said frame buffer apparatus

copies from said background frame region to said new frame region when said copy control bit is set by a central processing unit.

19. The frame buffer apparatus as claimed in claim 18 wherein each video random access memory device in said memory array comprises a random access port such that said central processing unit can access each memory location in said video random access memory array.

20. In a computer system, a frame buffer apparatus for copying information, said frame buffer apparatus comprising:

memory means divided into at least three frame regions, a first frame region associated with a background display image frame, a second frame region associated with a future display image frame, and a third frame region associated with a current display image frame, said memory means having a plurality of memory locations and a data register capable of loading and storing a row of said memory locations in said memory means; and

copy means coupled to said memory means, said copy means including means for loading and storing a plurality of rows of said memory locations using said data register in said memory means to copy said background display image frame in first frame region in said memory means to said future display image

frame in said second frame region in said memory means, wherein said copy means does not copy data to the third frame region while associated with a current display image frame.

21. The frame buffer apparatus as claimed in claim 20 wherein said frame buffer apparatus generates a video timing signal, said video timing signal having a vertical retrace period, and said copy means operates only during said vertical retrace period.

22. The frame buffer apparatus as claimed in claim 20 wherein said frame buffer apparatus generates a video timing signal, said video timing signal having a horizontal retrace period, and said copy apparatus operates only during said horizontal retrace period.

23. The frame buffer apparatus as claimed in claim 20 wherein said frame buffer apparatus includes

means for generating a video timing signal having a vertical retrace period and a horizontal retrace period, and,

wherein said copy apparatus includes

means for operating in at least one of said vertical retrace period and said horizontal retrace period.

24. The frame buffer apparatus as claimed in claim 21 wherein said data register that can load and store a row of said memory locations in said memory means comprises a serial data register coupled to serial access port.

25. In a computer system, a frame buffer apparatus for copying video information in a first frame region, said frame buffer apparatus comprising:
memory means divided into the first frame region associated with a first display image frame, a second frame region associated with a second display image frame, and a third display frame region associated with a third display image frame, said memory means including a plurality of memory locations and a data register capable of loading and storing a row of said memory locations in said memory means;

a background frame register storing a pointer to one of the frame regions in said video memory array;

a future frame register storing a pointer to one of the frame regions in said video memory array;

copy means coupled to said memory means, said copy means loading and storing a plurality of rows of said memory locations using said data register in said memory means to copy contents in the frame region pointed to by the background frame register to said frame region pointed to by the future frame register;

display frame register storing a pointer to one of the display frame regions in said video memory array; and

video display means including

means for loading rows of memory from a display frame region pointed to by said display frame register means into said serial data register and shifting said rows of memory out through said serial access port.

26. The frame buffer apparatus as claimed in claim 25 wherein said frame buffer apparatus further comprises:

background frame register means, said background frame register means pointing to a background frame region in said video memory array containing a background image;

a new frame register means, said new frame register means pointing to a new frame region in said video memory array; and

wherein said copy means copies from said background frame region to said new frame region.

27. The frame buffer apparatus as claimed in claim 26 wherein further comprises a copy control bit and said copy means copies from said background frame region to said new frame region when a central processing unit sets said copy control bit.

28. In a graphic computer system, said graphic computer system comprising a graphics display screen and a copy apparatus for copying one frame region associated with a background display image frame to a second frame region associated with a future display image frame, a method of performing doubled buffered animation, said method comprising the steps of:

- a) painting a background scene in a background frame region;
- b) copying said background scene in said background frame region into a first frame region using said copy apparatus;
- c) rendering a frame of animation in said first frame region, said frame of animation rendered on said background scene;
- d) displaying said first frame region on said graphics display screen;
- e) copying said background scene in said background frame region into a second frame region using said copy apparatus;
- f) rendering a frame of animation in said second frame region, said frame of animation rendered on said background scene;

- g) displaying said second frame region on said graphics display screen;
and
- h) repeating steps b through g until said animation is complete.

29. The method of performing doubled buffered animation as claimed in claim 28 wherein said steps of copying are performed during a vertical retrace period of a video timing signal.

30. The method of performing doubled buffered animation as claimed in claim 28 wherein said steps of copying are performed during a horizontal retrace period of a video timing signal.

31. The method of performing doubled buffered animation as claimed in claim 28 wherein said steps of copying are performed during a vertical retrace and a horizontal retrace period of a video timing signal.

32. The method of performing doubled buffered animation as claimed in claim 28 wherein said method of performing doubled buffered animation is performed in real time.

33. A method of copying video information with a frame buffer apparatus in a computer system including a video memory array having at least one random access memory device with a plurality of memory locations and a serial data register, said method comprising:

dividing said video memory array into a first frame region associated with a background display image frame, a second frame region associated with a future display image frame, and a third frame region associated with a current display image frame;

copying contents in the first frame region to the second frame region by loading and storing a plurality of rows of said memory locations in each random access memory device using said serial data register; and

changing an association of the current display image frame from the third frame region to one of the first and second frame regions.

34. The method according to claim 33, wherein said frame buffer apparatus further comprises the step of

generating a timing signal having a vertical retrace period and a horizontal retrace period.

35. The method according to claim 34, wherein said step of copying further comprises the step of

copying contents from said first frame region to second frame region during at least one of vertical retrace period and horizontal retrace period.

36. The method according to claim 35, wherein said frame buffer apparatus further comprises the step of

pointing to a display frame region in said video memory array;

loading rows of memory from said display frame region into said serial data register; and

shifting rows of memory out through a serial access port coupled to said serial data register.

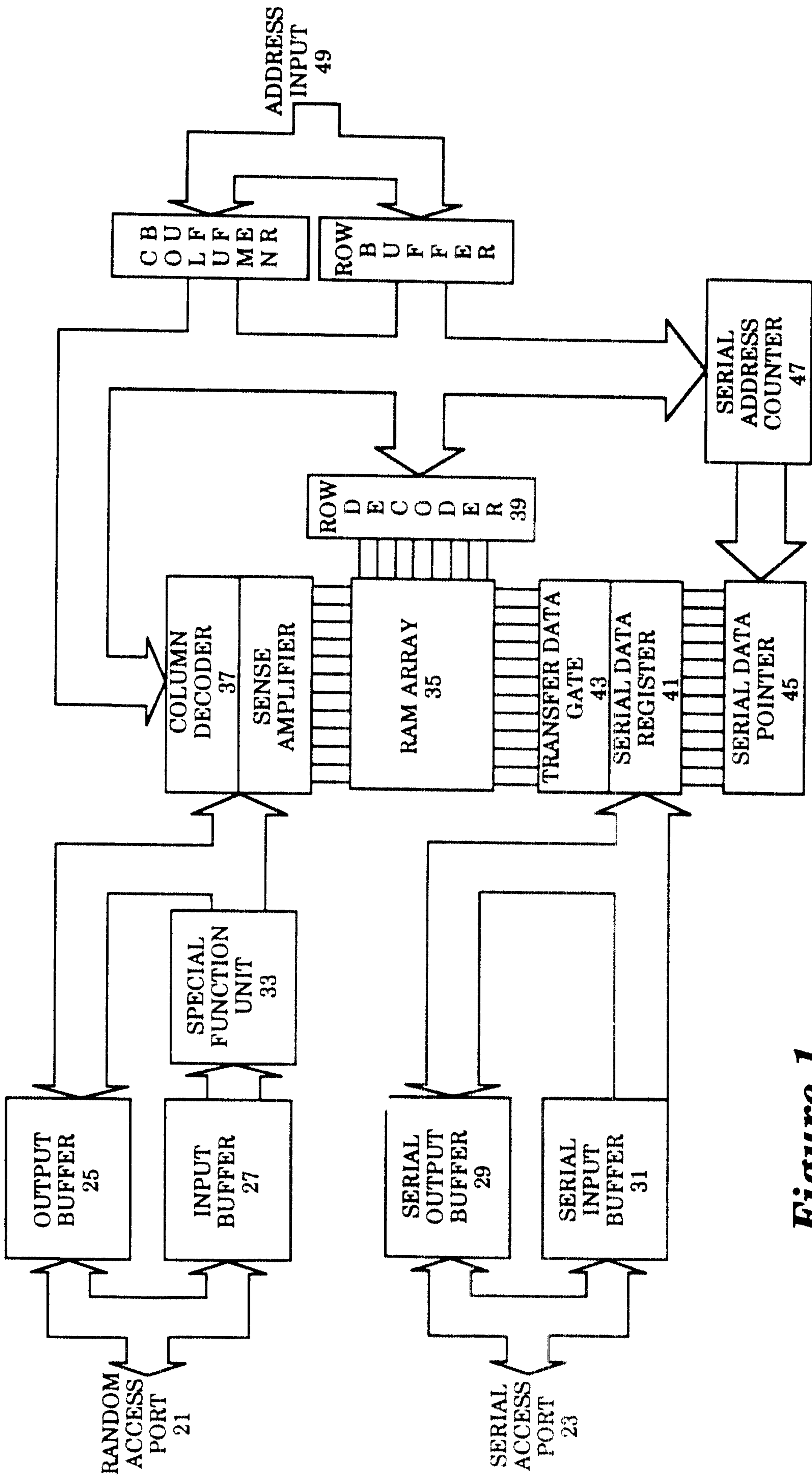


Figure 1
(Prior Art)

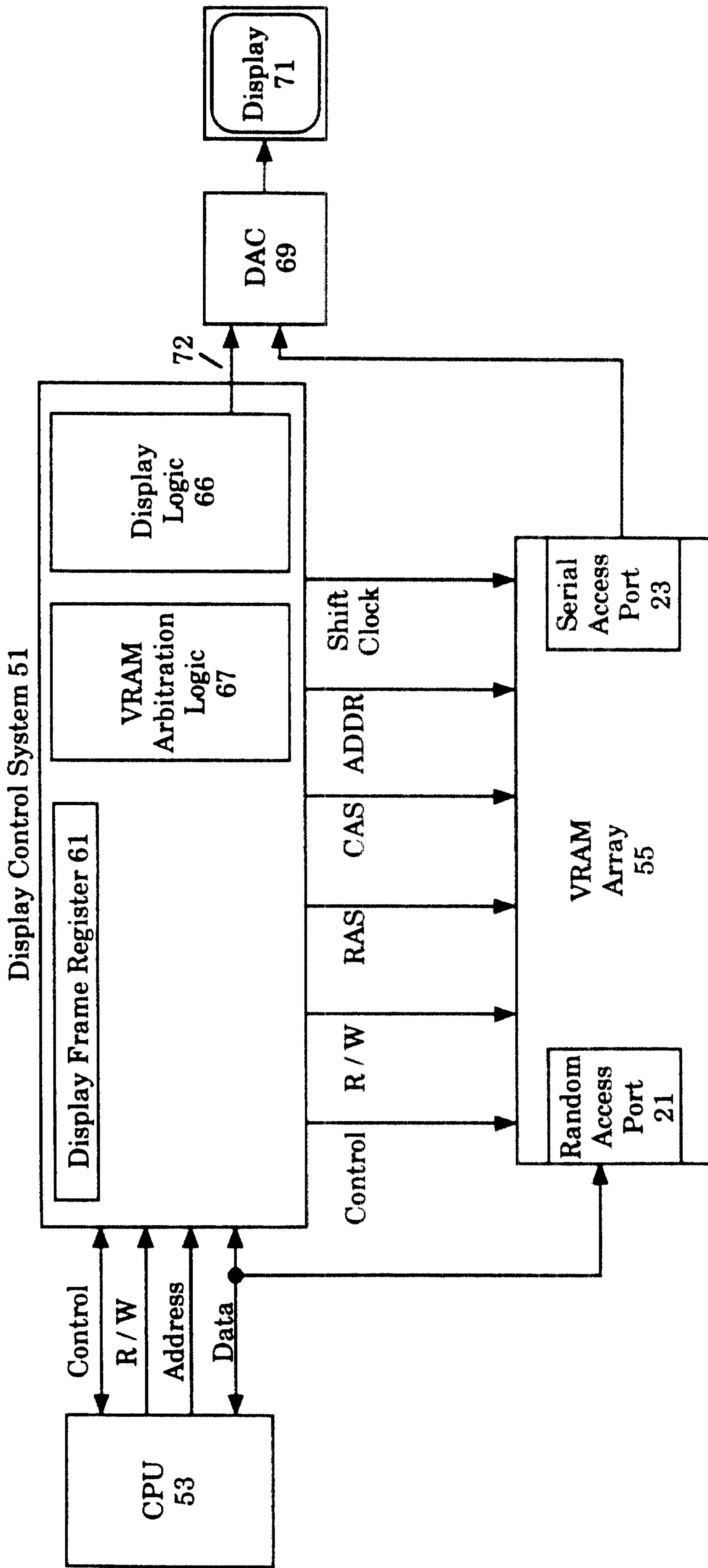


Figure 2
(Prior Art)

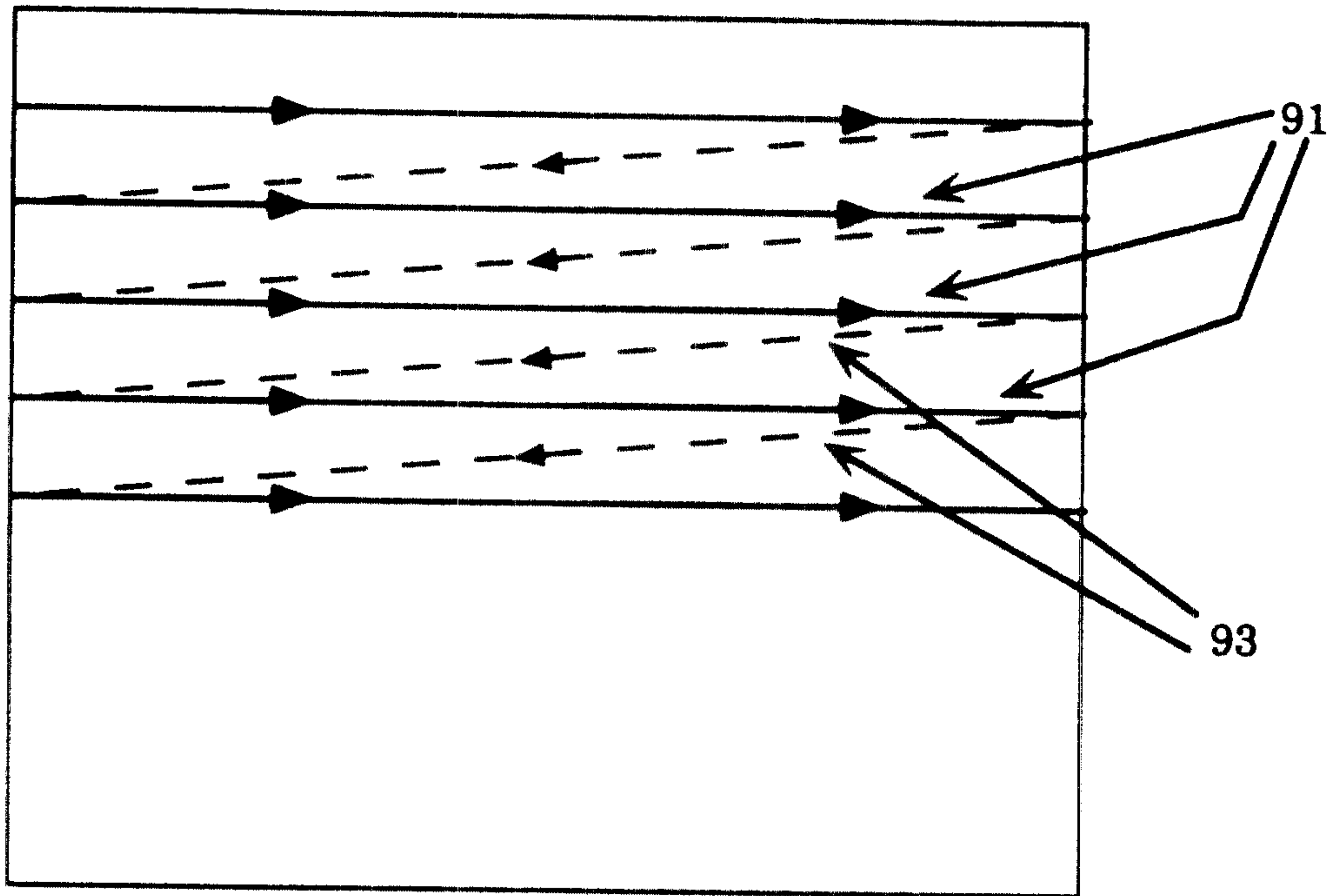


Figure 3a

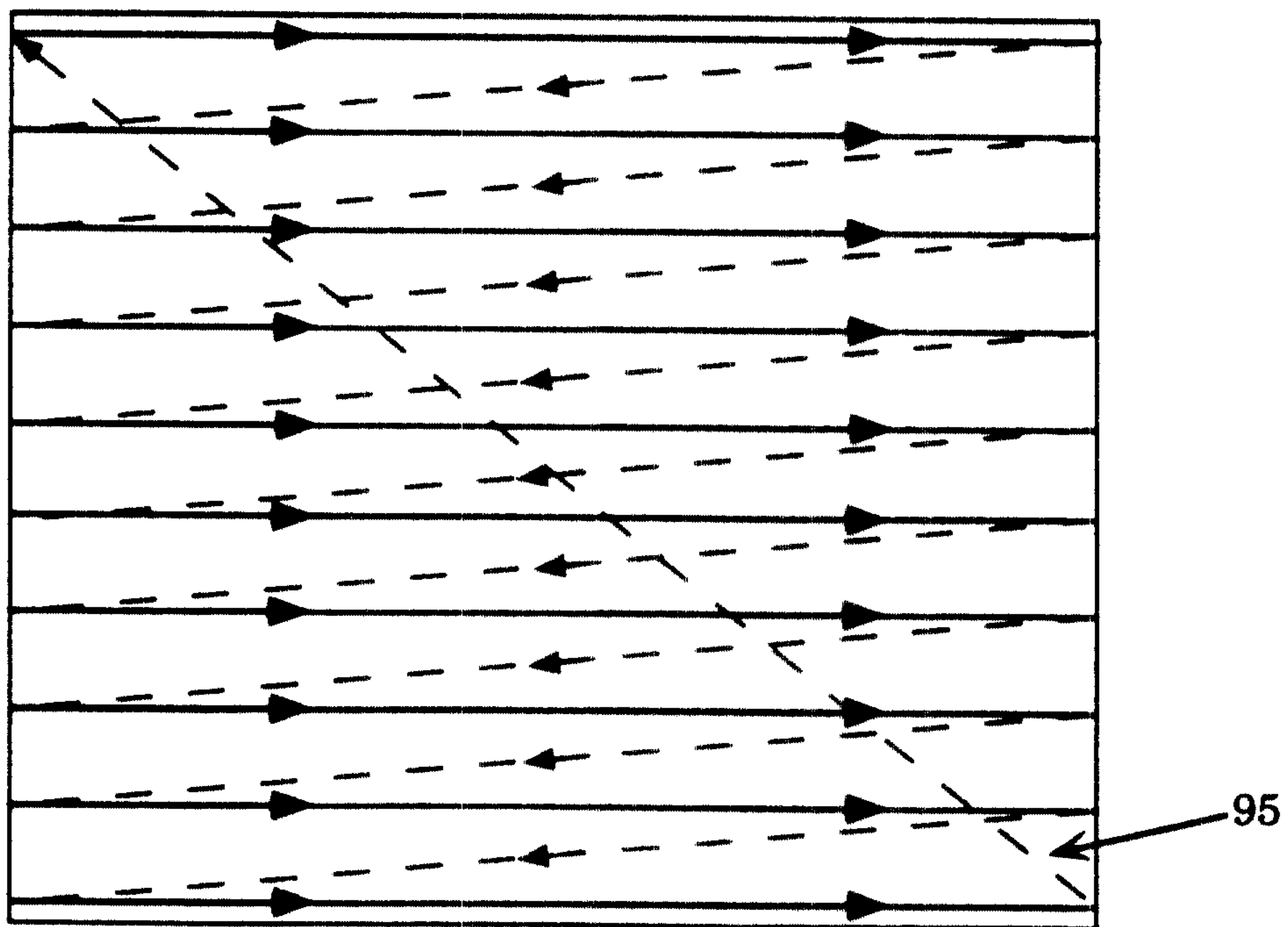


Figure 3b

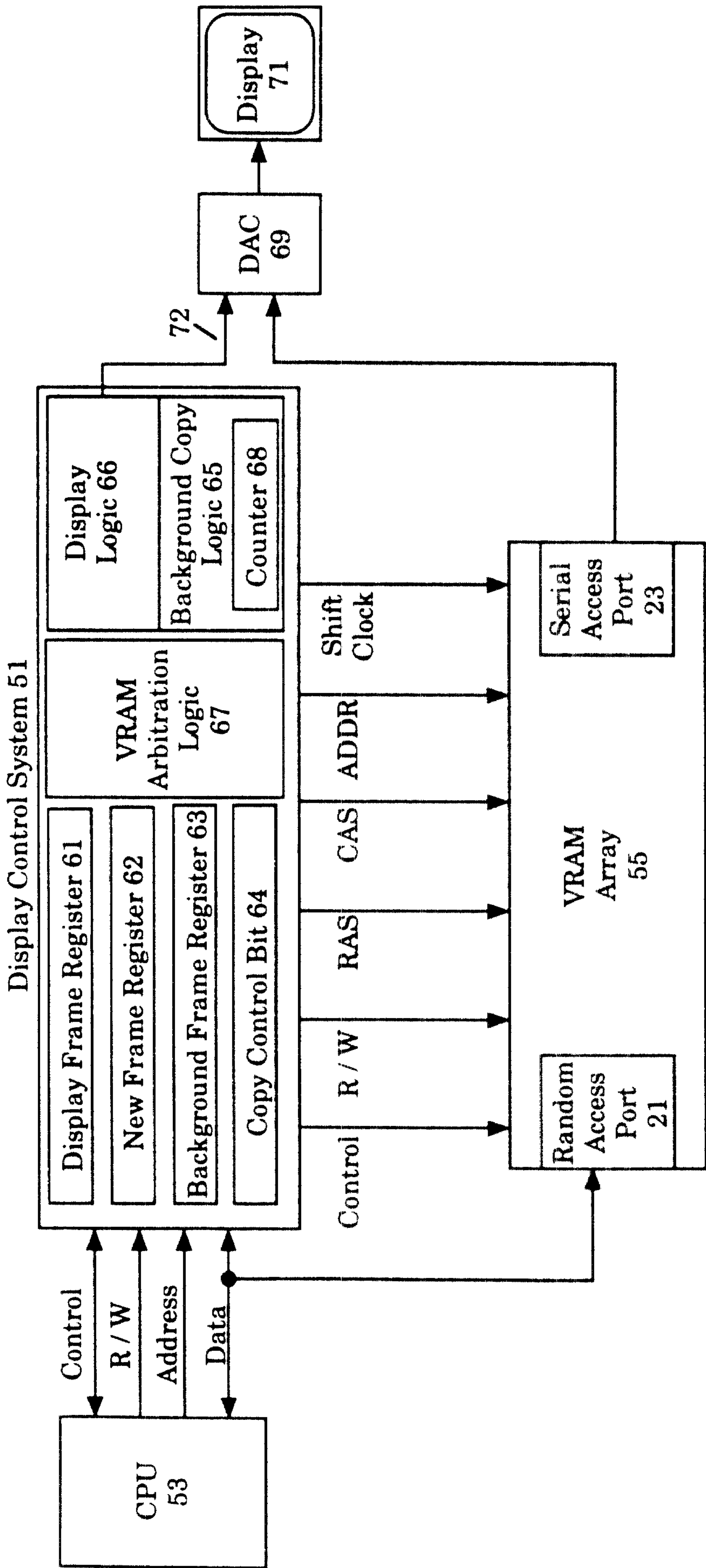


Figure 4

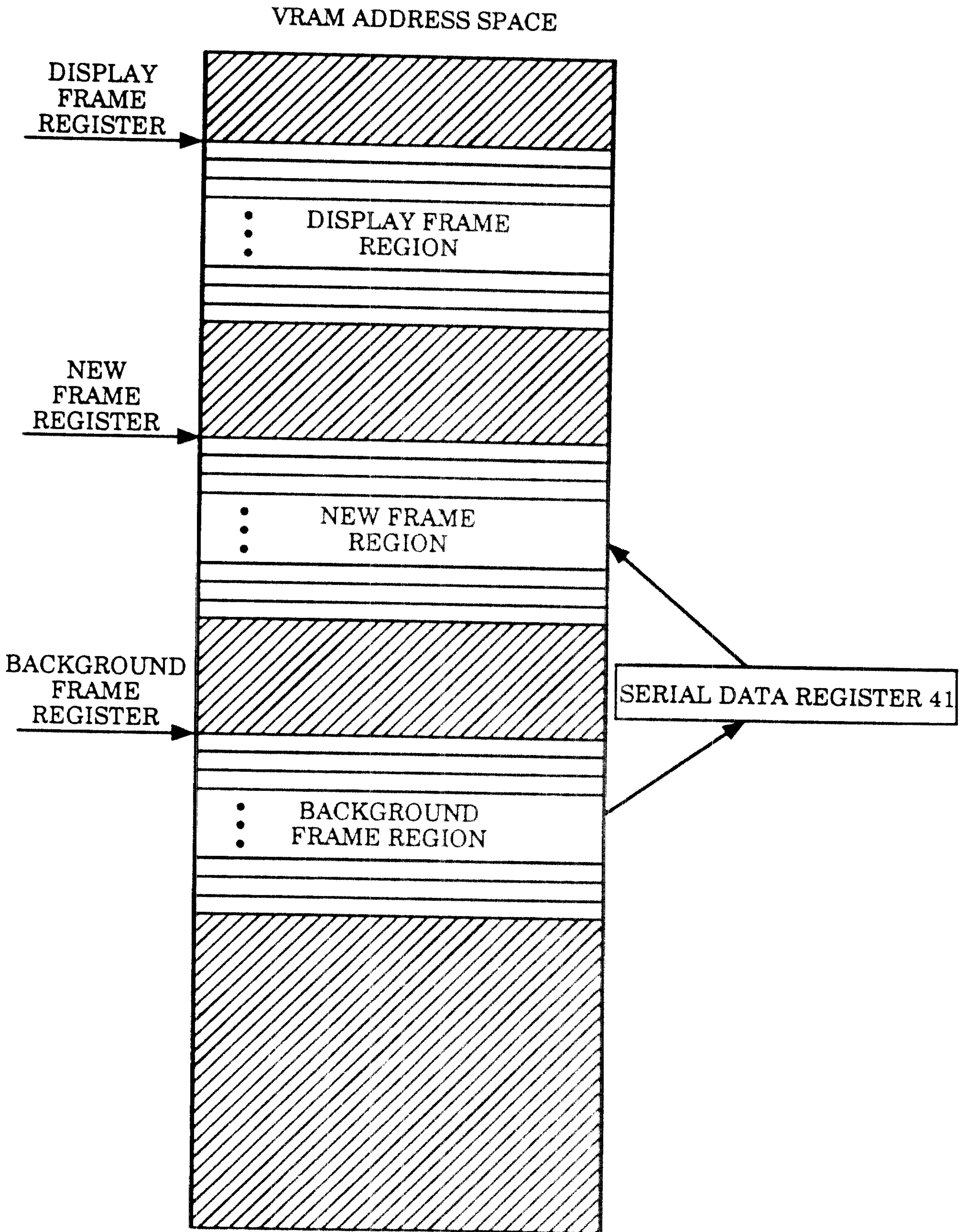
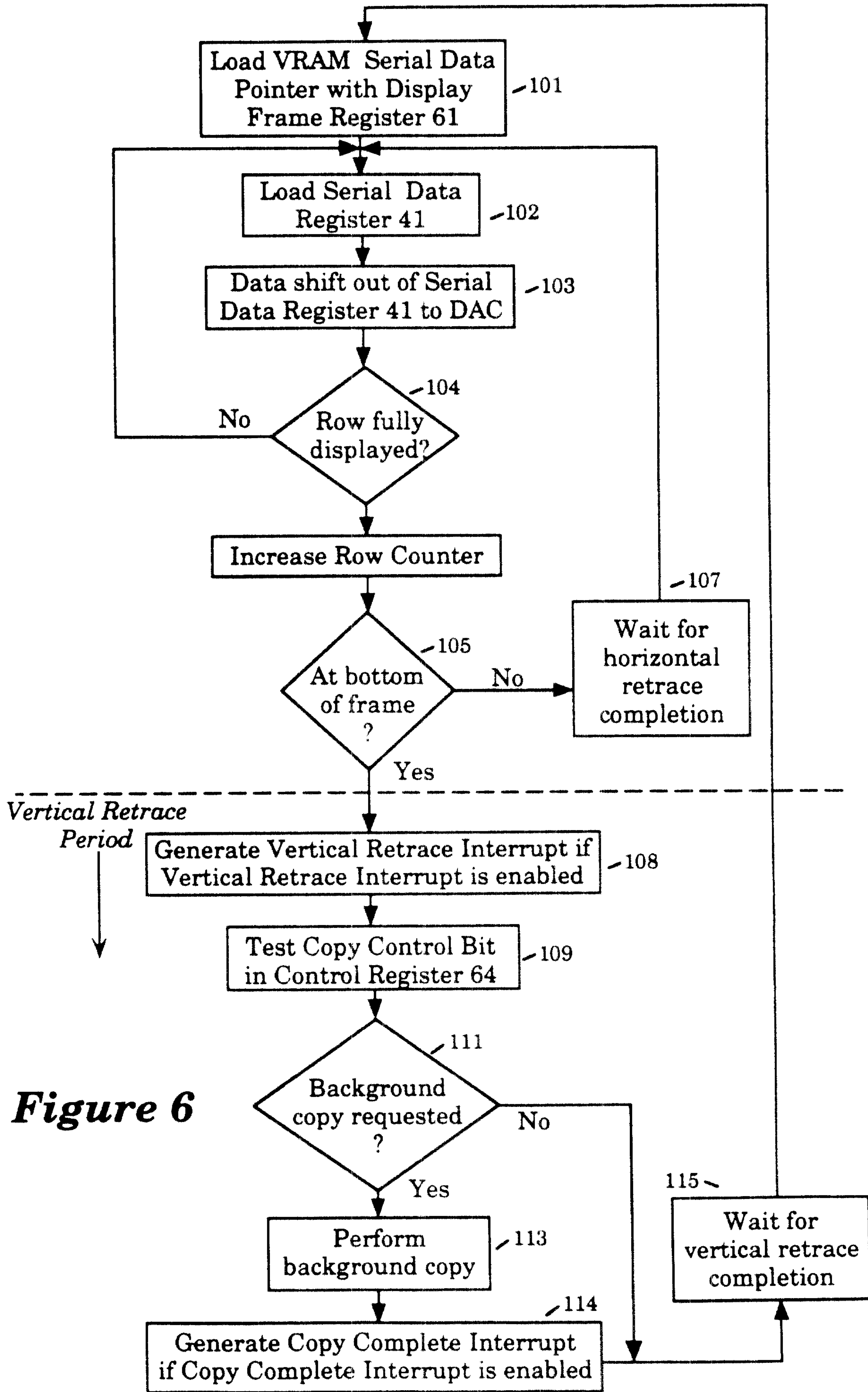


Figure 5



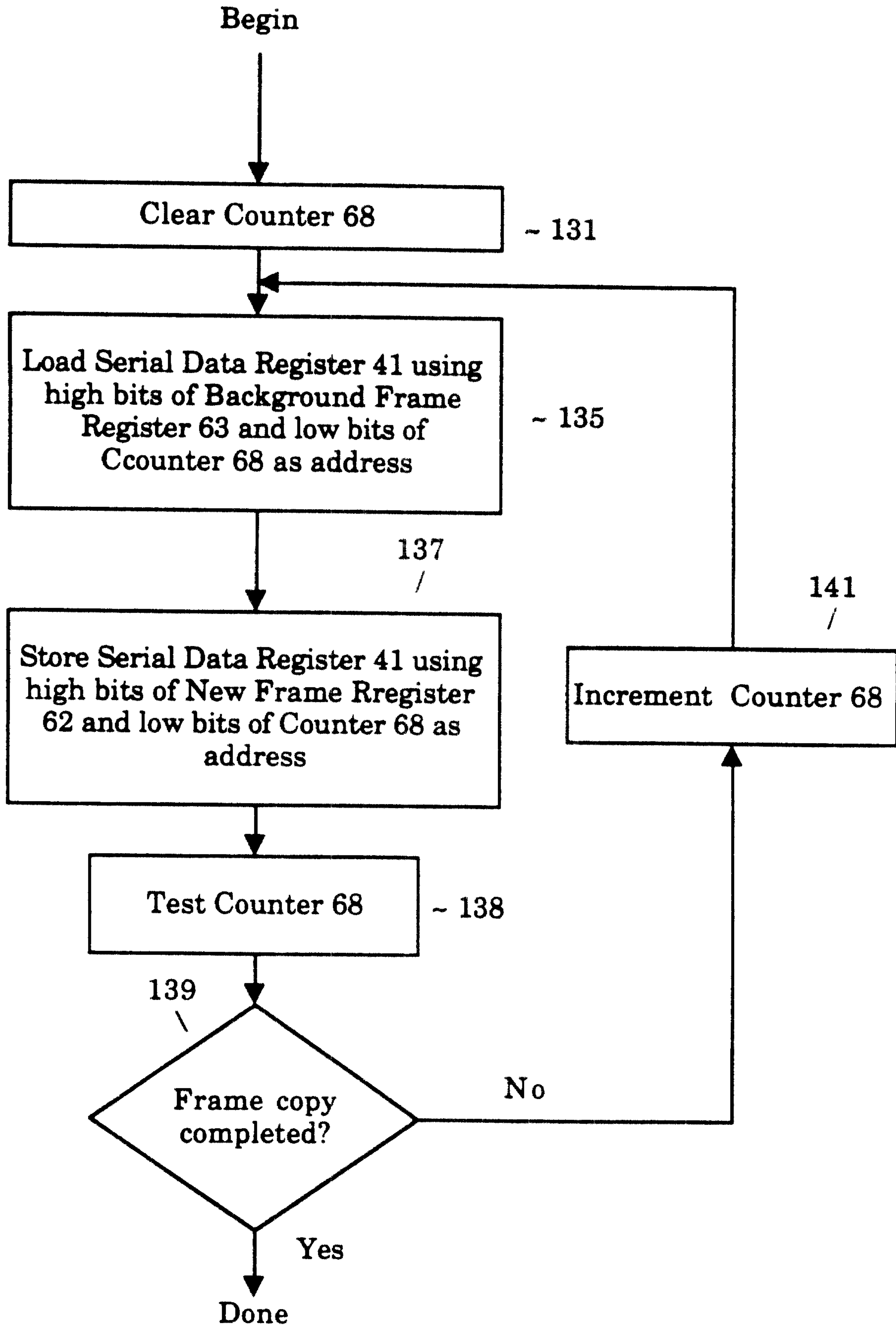
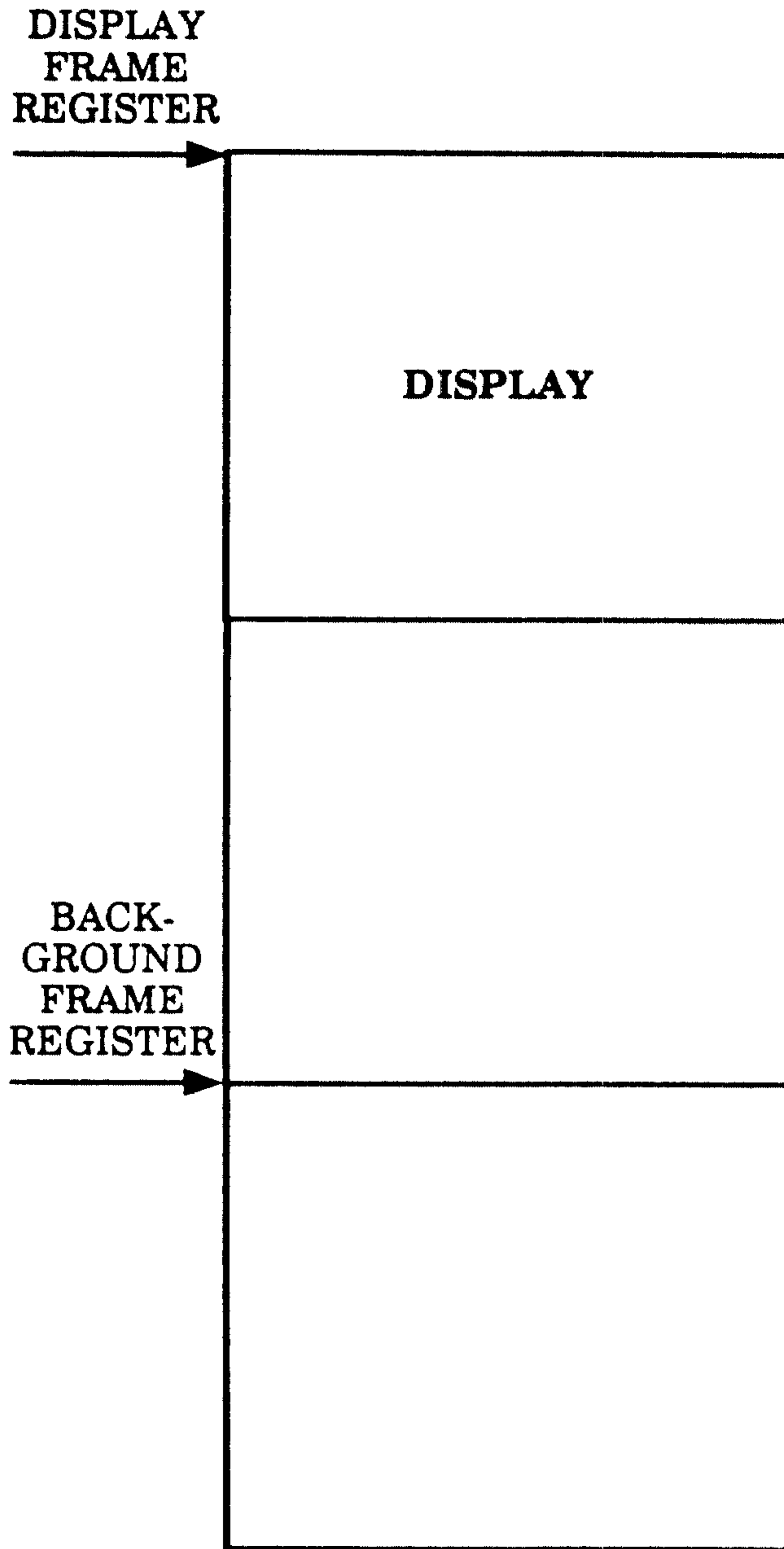
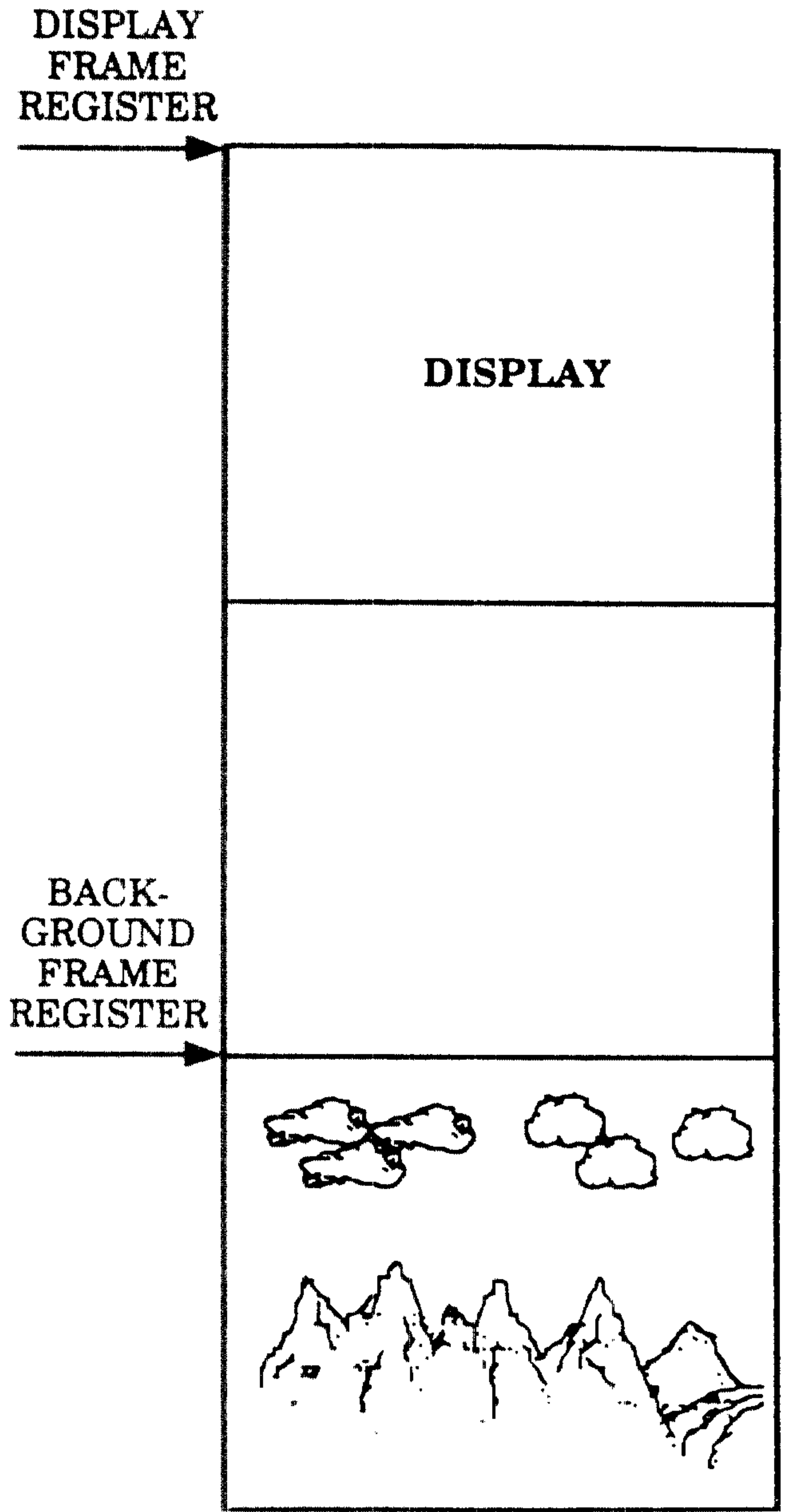


Figure 7



NEW FRAME REGISTER IS NULL

Figure 8a



NEW FRAME REGISTER IS NULL

Figure 8b

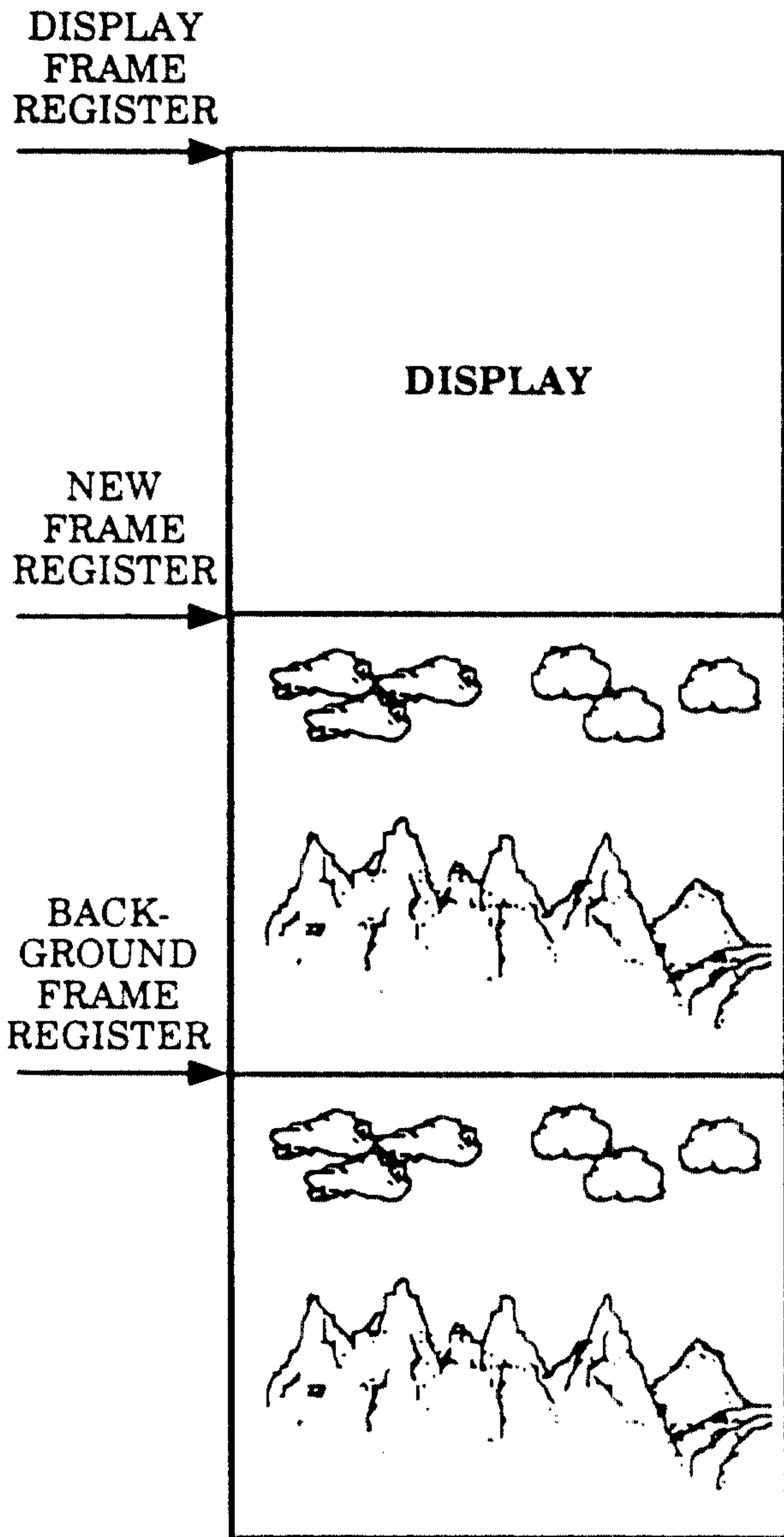


Figure 8c

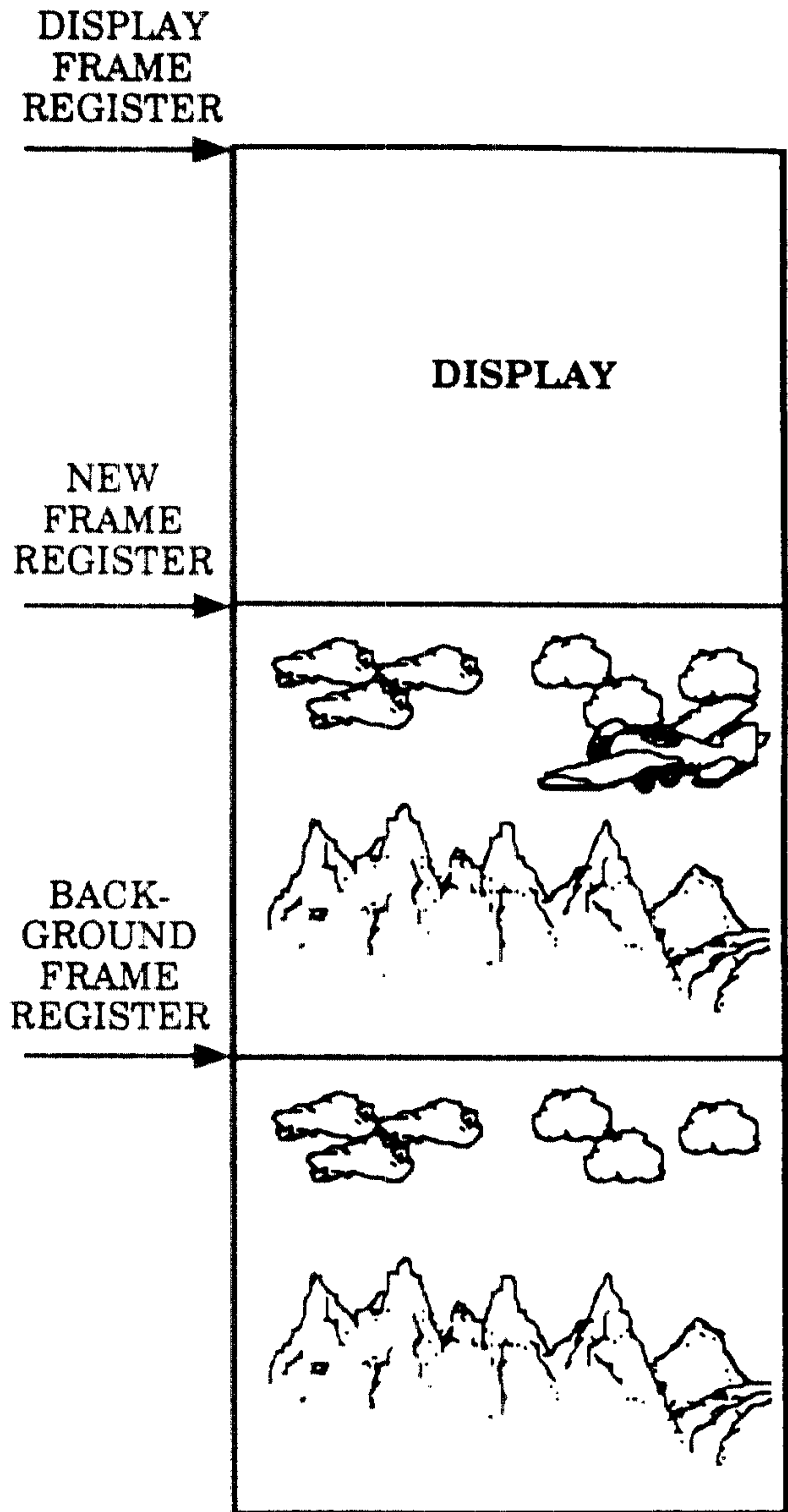


Figure 8d

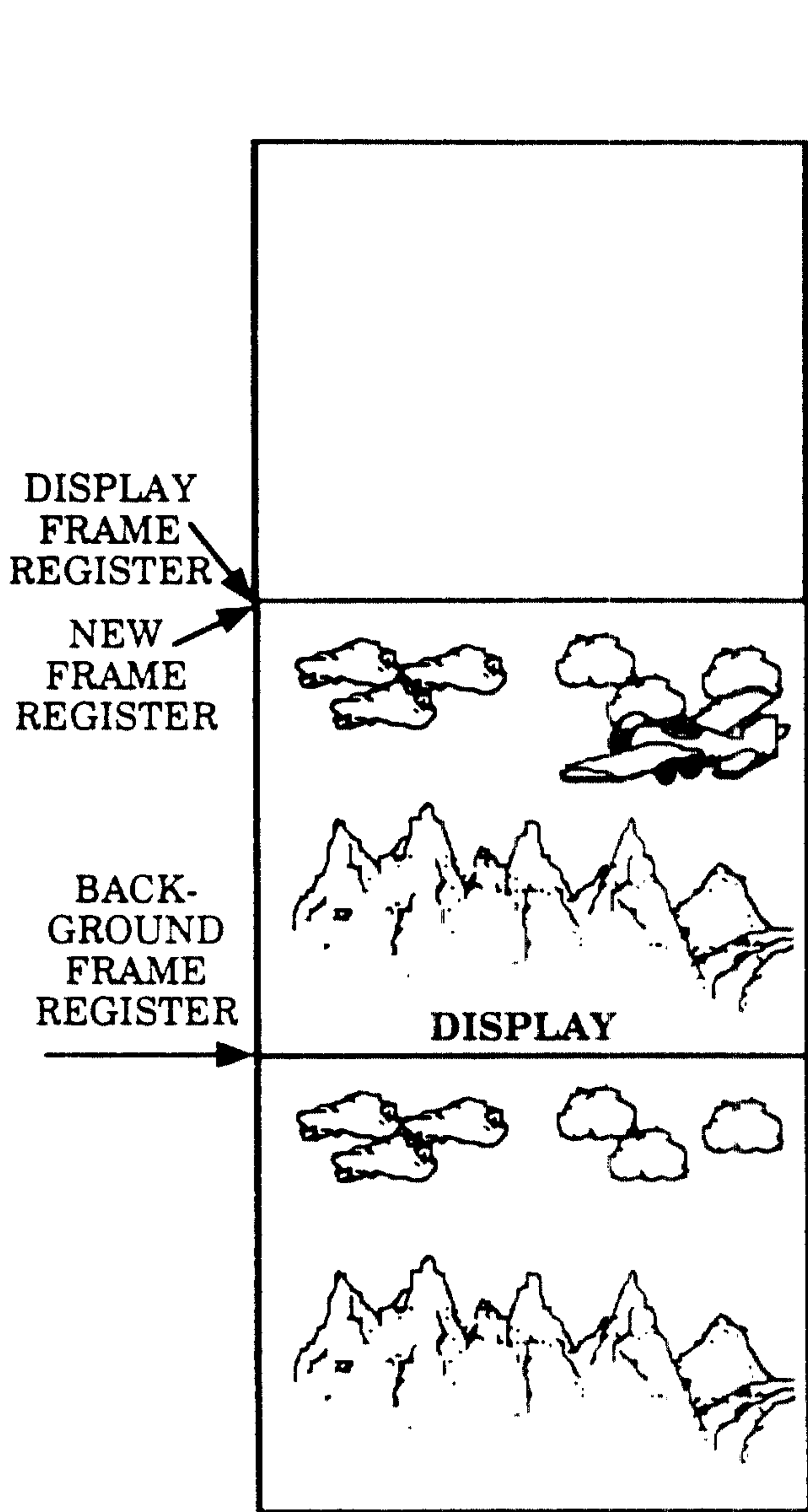


Figure 8e

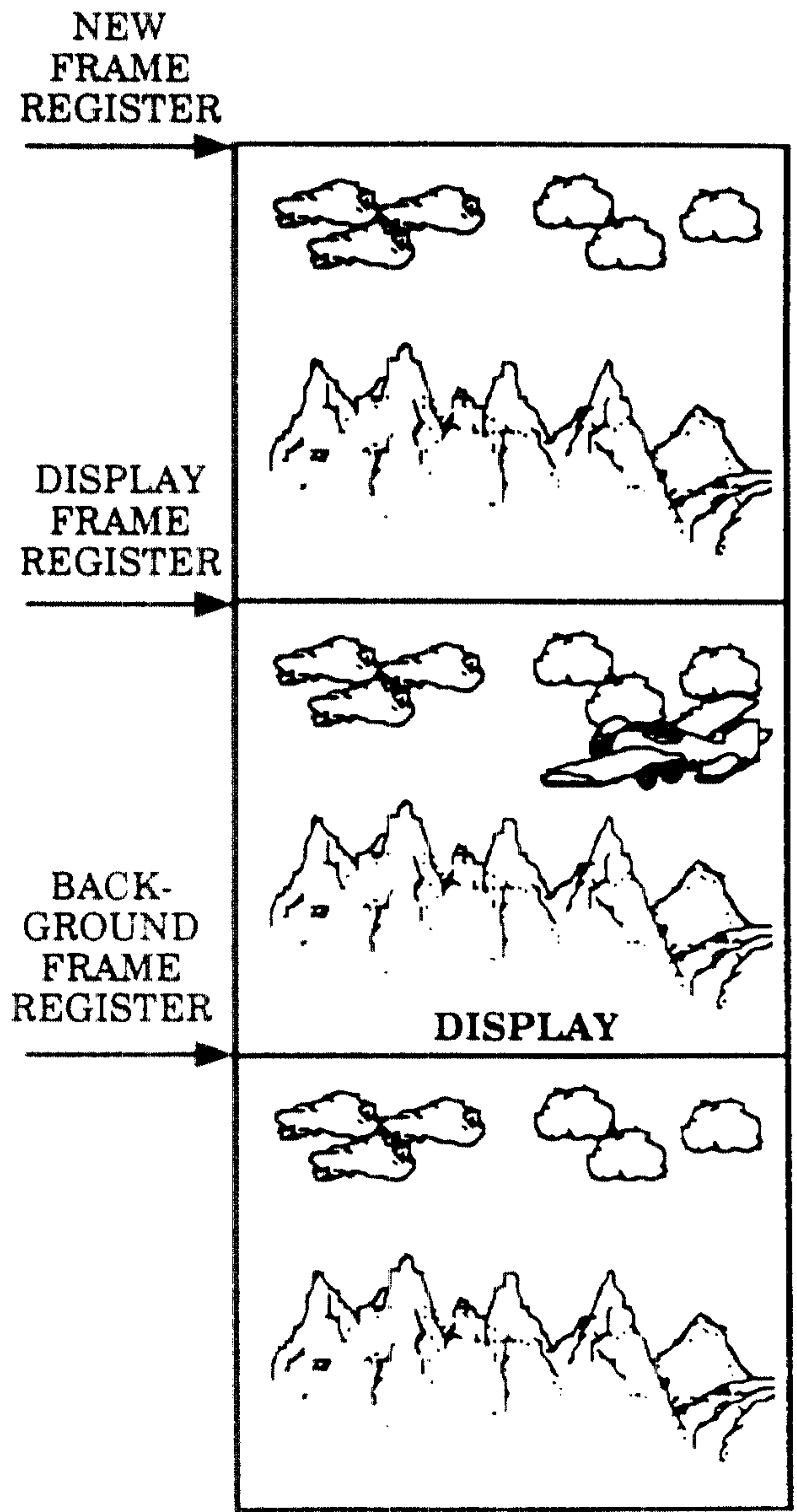


Figure 8f

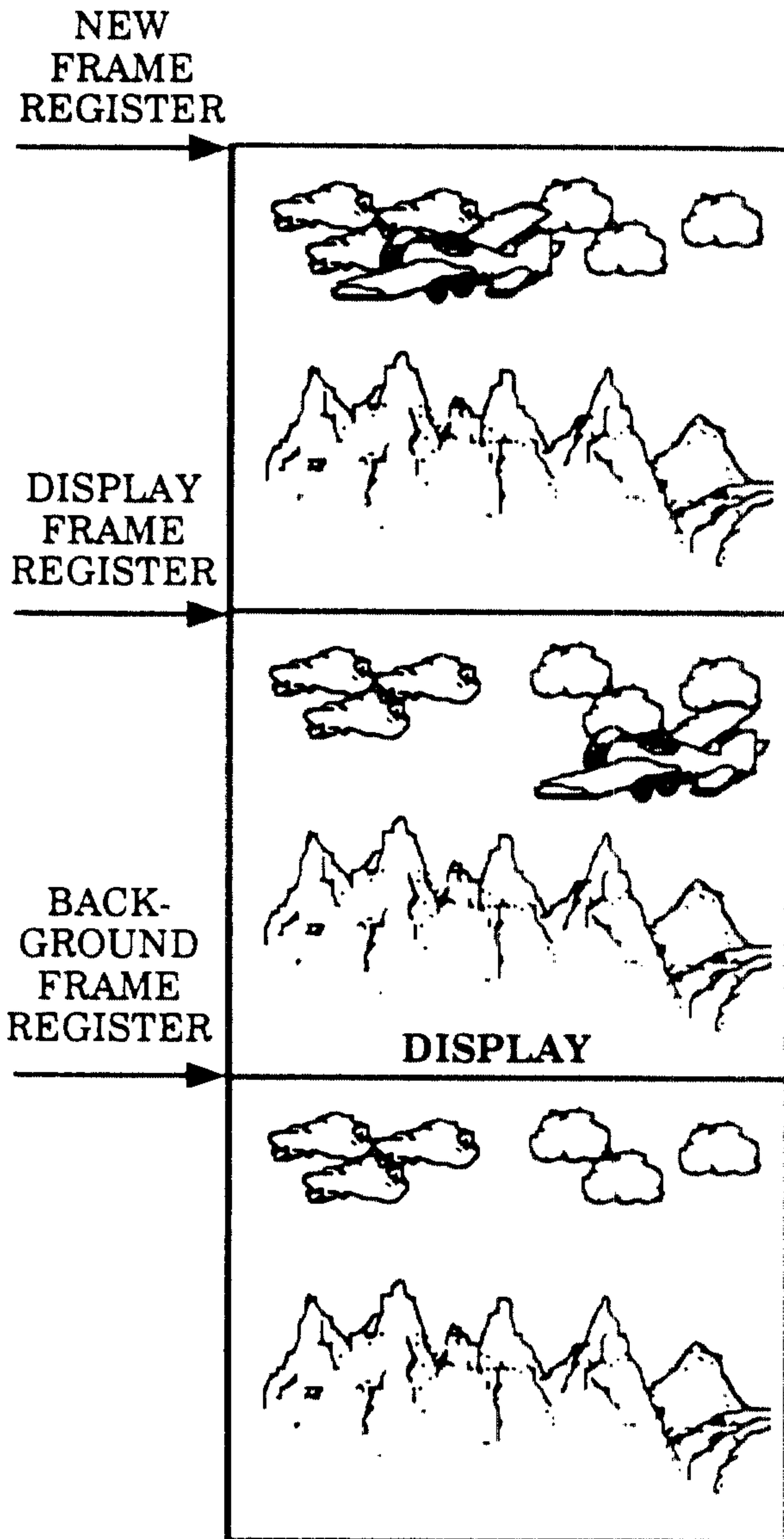


Figure 8g

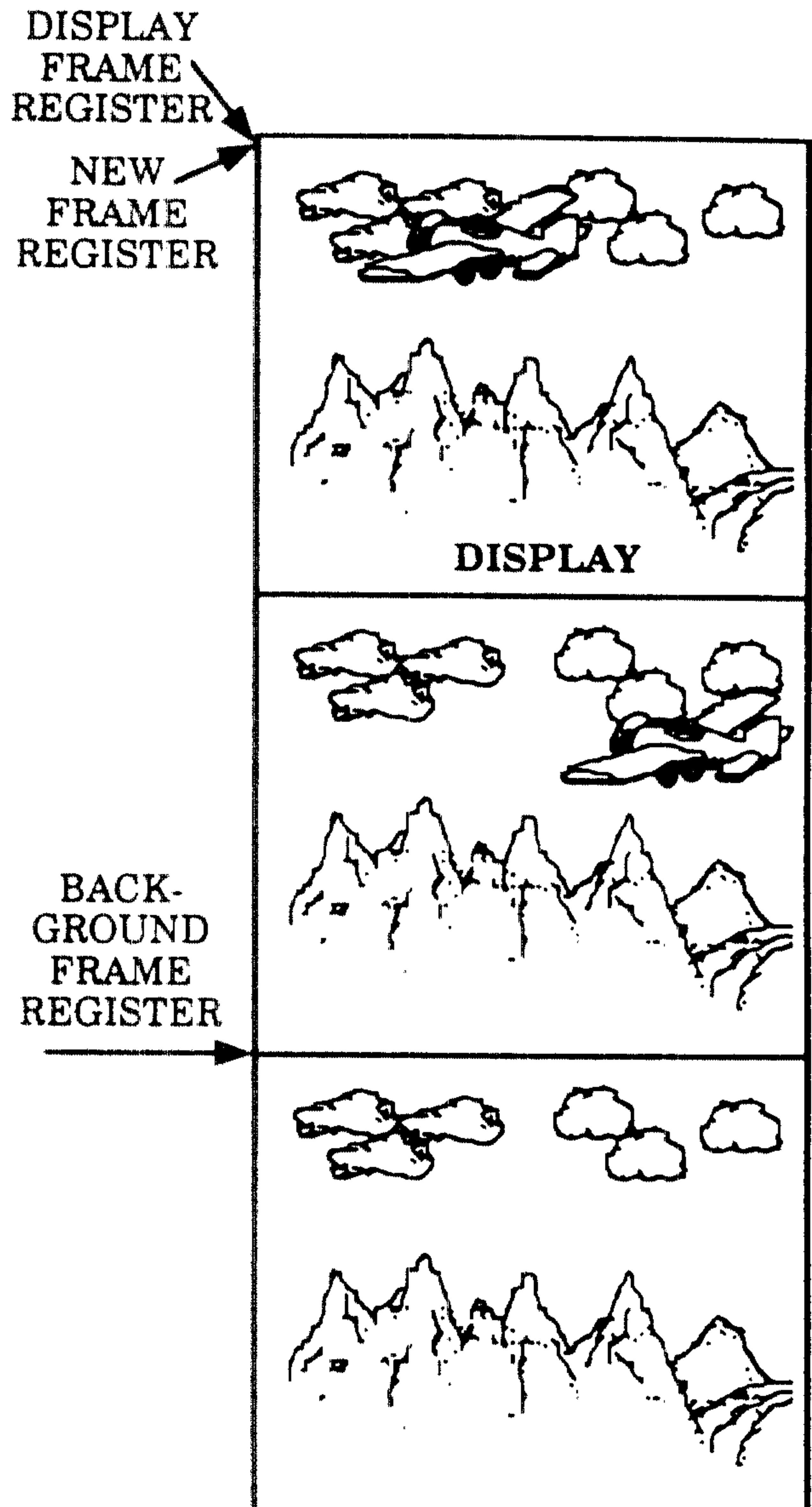


Figure 8h

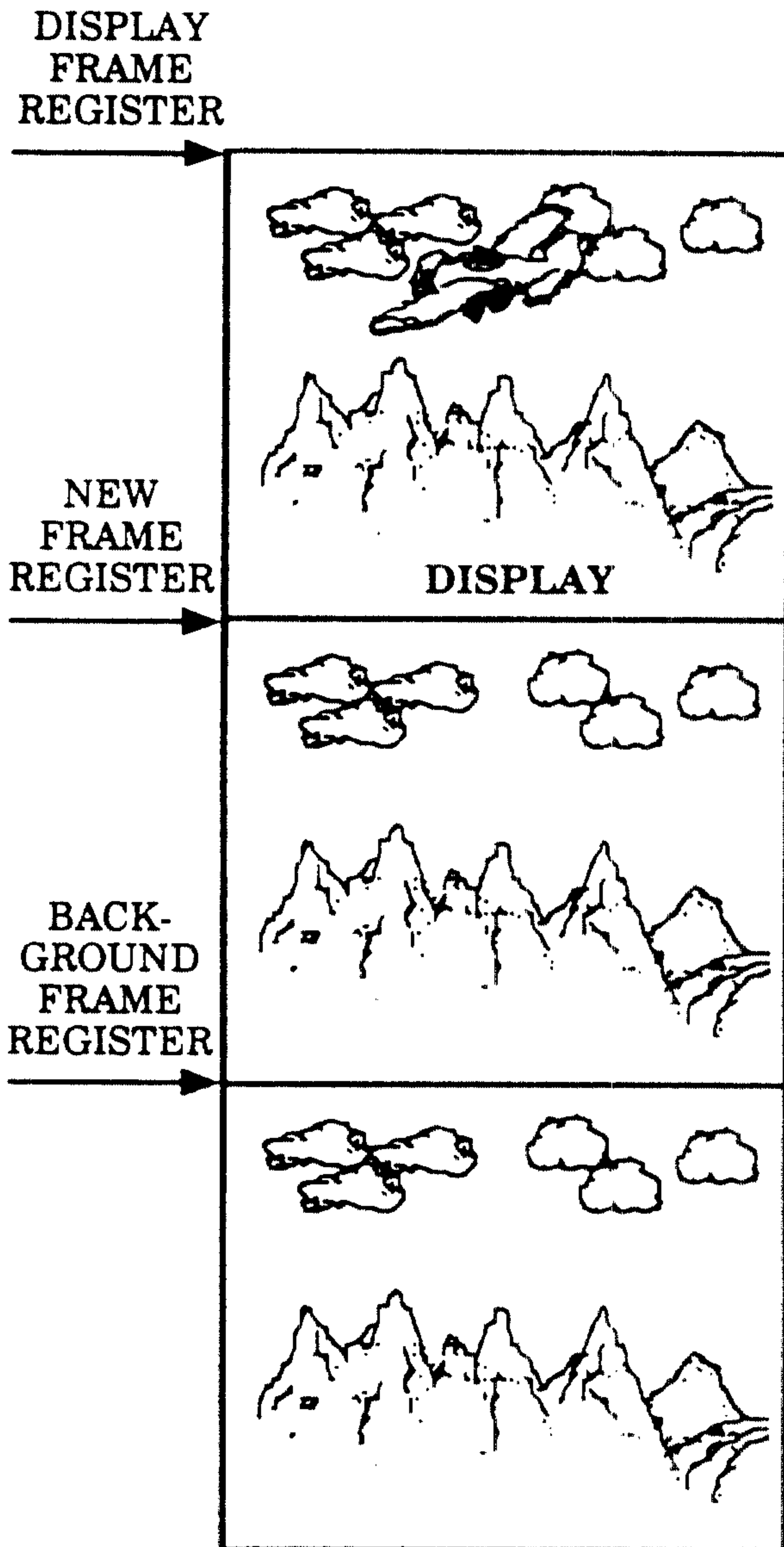


Figure 8i

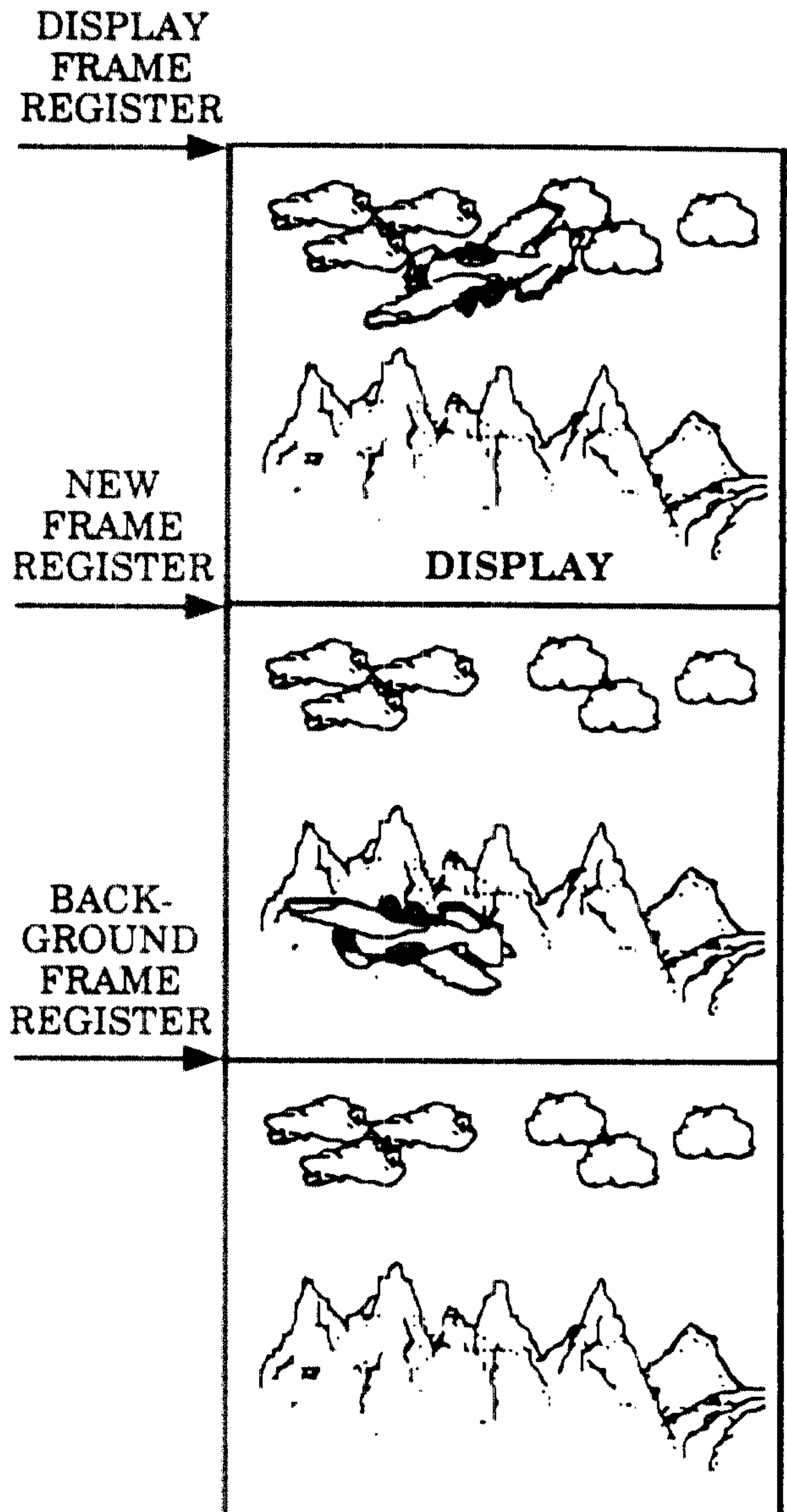


Figure 8j

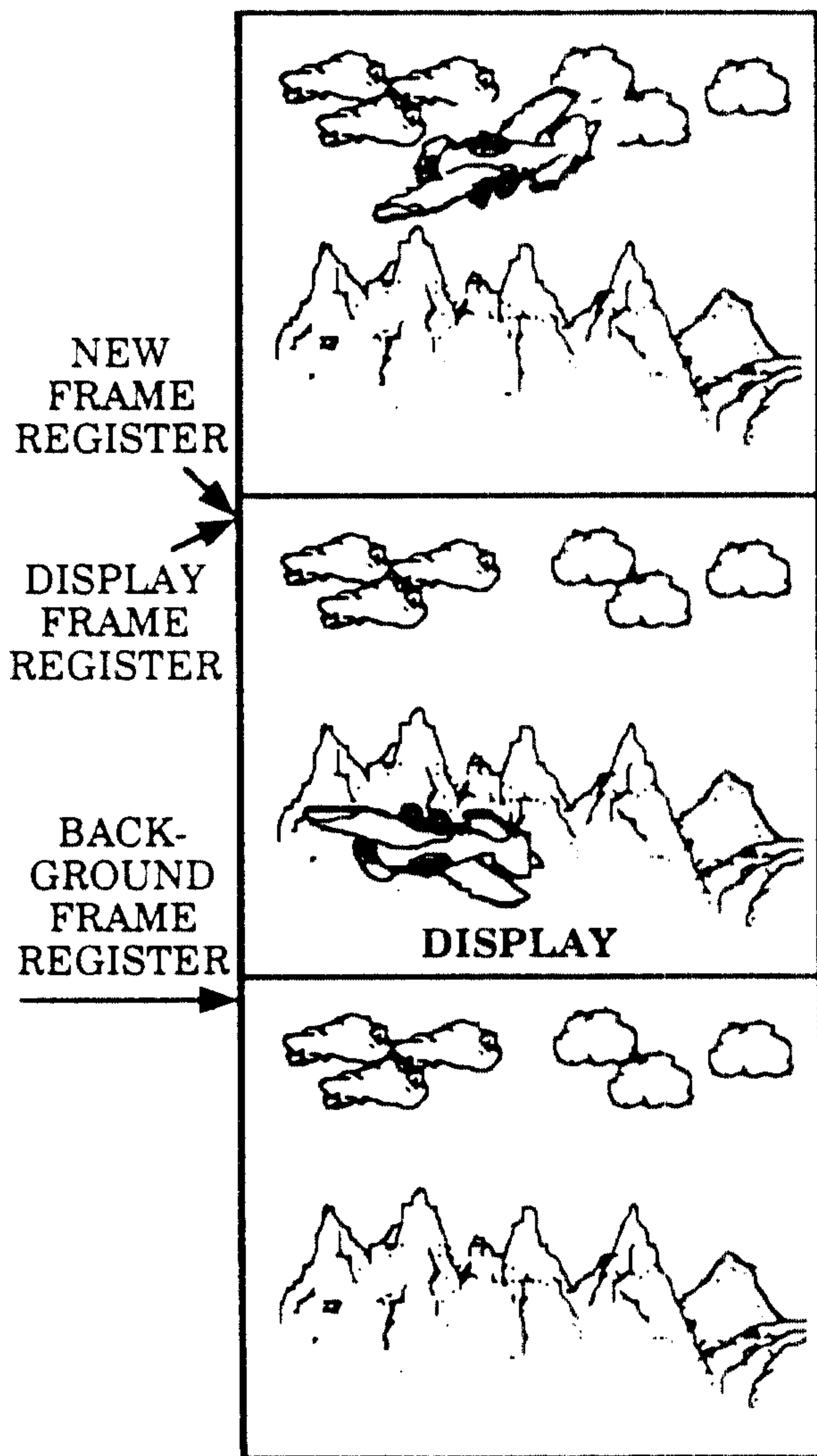


Figure 8k

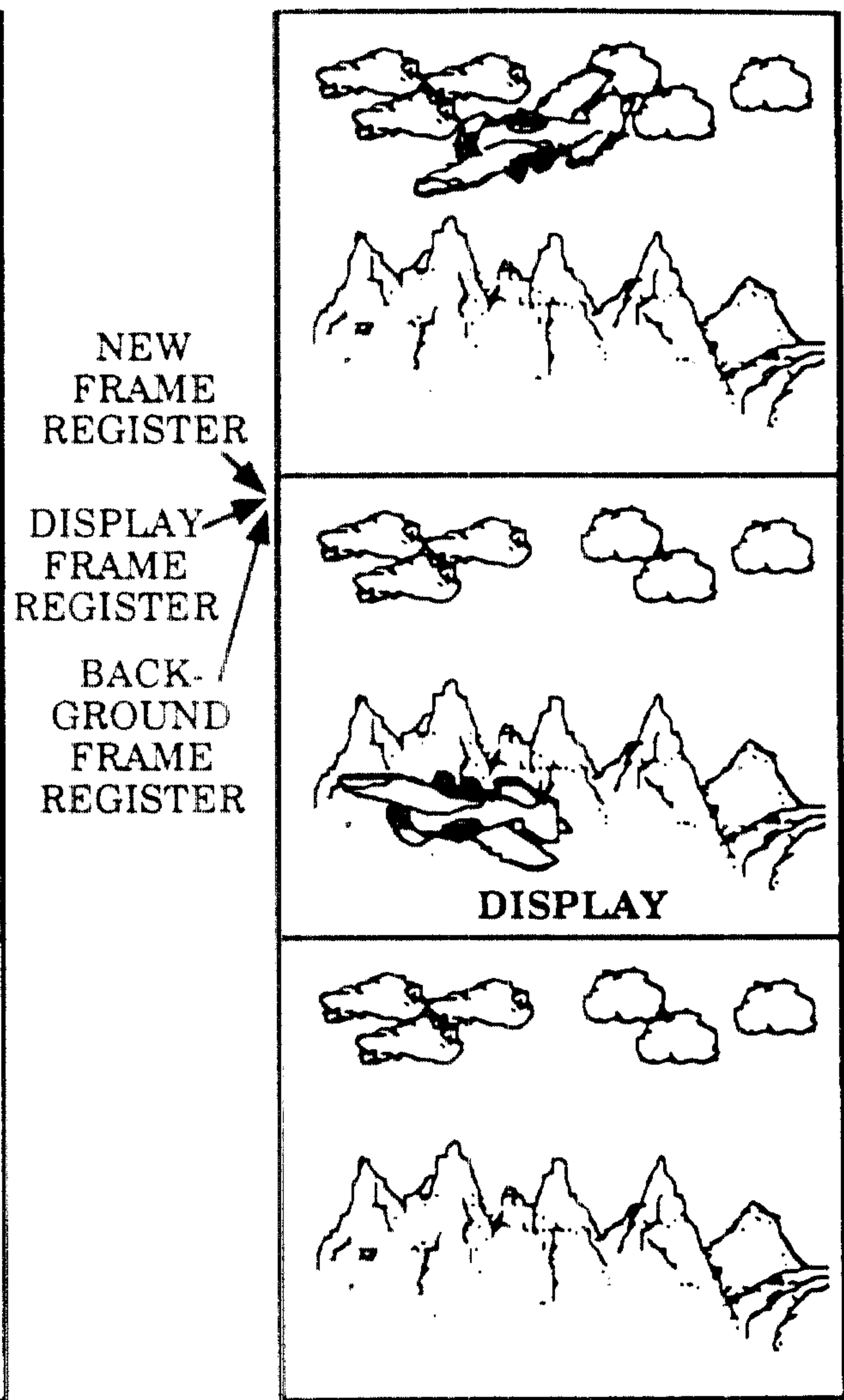


Figure 8l

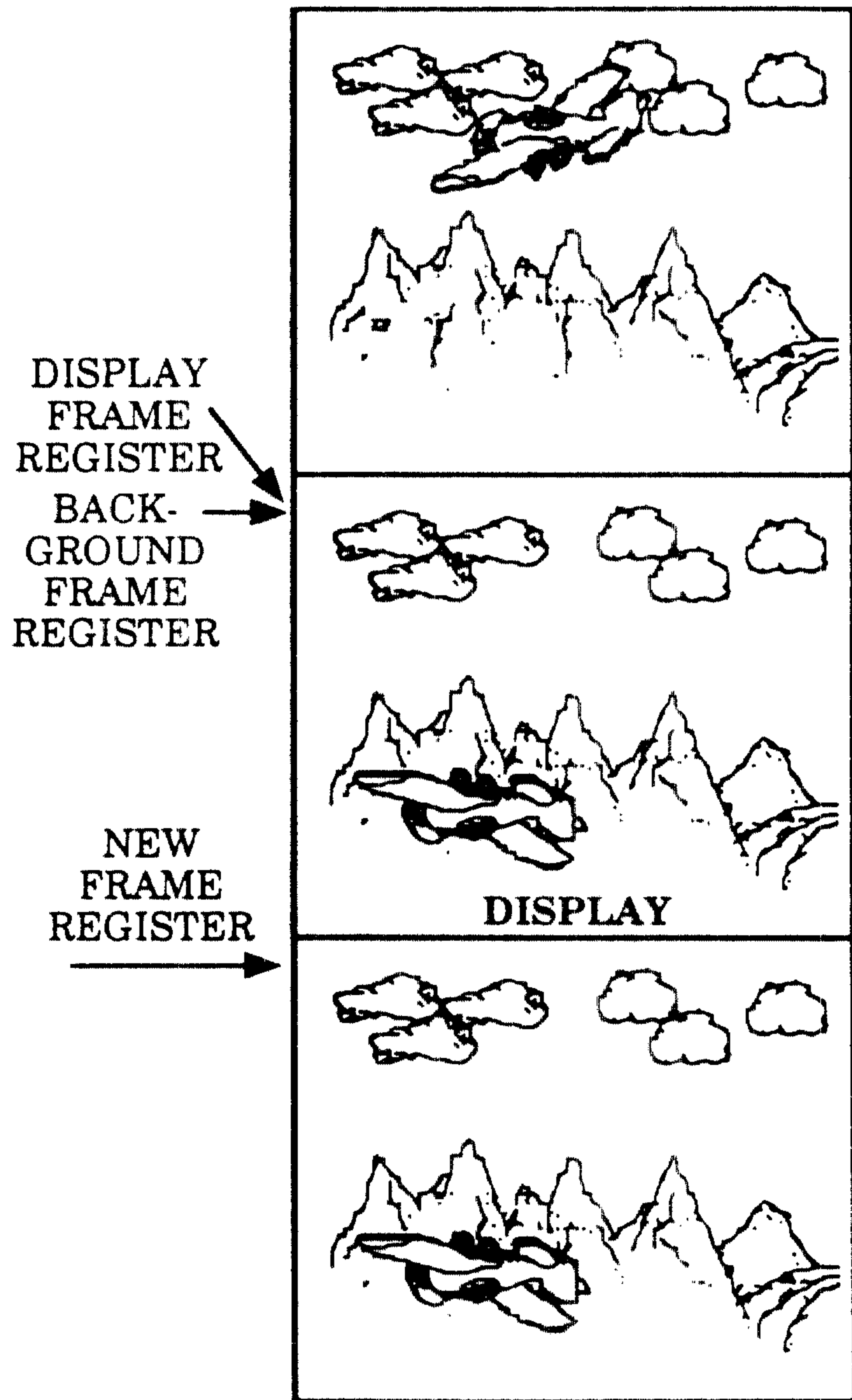


Figure 8m

VRAM ADDRESS SPACE

DISPLAY
FRAME
REGISTER

•
•
• DISPLAY FRAME
REGION

NEW
FRAME
REGISTER

•
•
• NEW FRAME
REGION

BACKGROUND
FRAME
REGISTER

•
•
• BACKGROUND
FRAME REGION

SERIAL DATA REGISTER 41

