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H03M 13/00

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H4P PRV

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EP 0441968 A1 **EP 0138598 A2** **JP 008340262 A**
US 5414738 A **US 5027374 A**

(58) Field of Search
UK CL (Edition O) **H4P PRV**
INT CL^6 **H03M 13/00**
ONLINE : WPI

(54) **Viterbi decoder**

(57) A Viterbi decoder is provided. The Viterbi decoder includes a branch metric calculating unit (210) for receiving the convolutional data and calculating a plurality of branch metrics, a branch metric allocating unit (220) for allocating the plurality of branch metrics as even and odd branch metrics, a state metric storing unit (240) for storing a current state metric and allocating a plurality of state metrics as even and odd state metrics, first and second add-compare-select (ACS) units (232, 234) for performing addition, comparison, and selection on the even branch and state metrics, and selecting paths having optimum distances, third and fourth ACS units (236, 238) for performing addition, comparison, and selection on the odd branch and state metrics, and selecting paths having optimum distances, a path tracing logic unit (250) for tracing the path selection information selected in the first through fourth ACS units (232-236), and outputting decoded data, and a path storing unit (260) for storing a path selection signal generated and selected in the path selection information controller. Therefore, the ACS units receive branch and state metrics and operate a plurality of states at one time, thereby decoding a plurality of channels at an increased speed.

FIG. 2

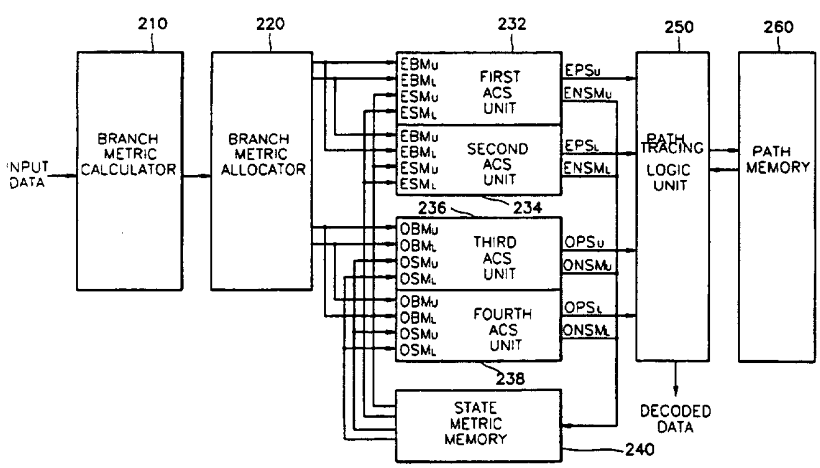

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FIG. 1 (PRIOR ART)

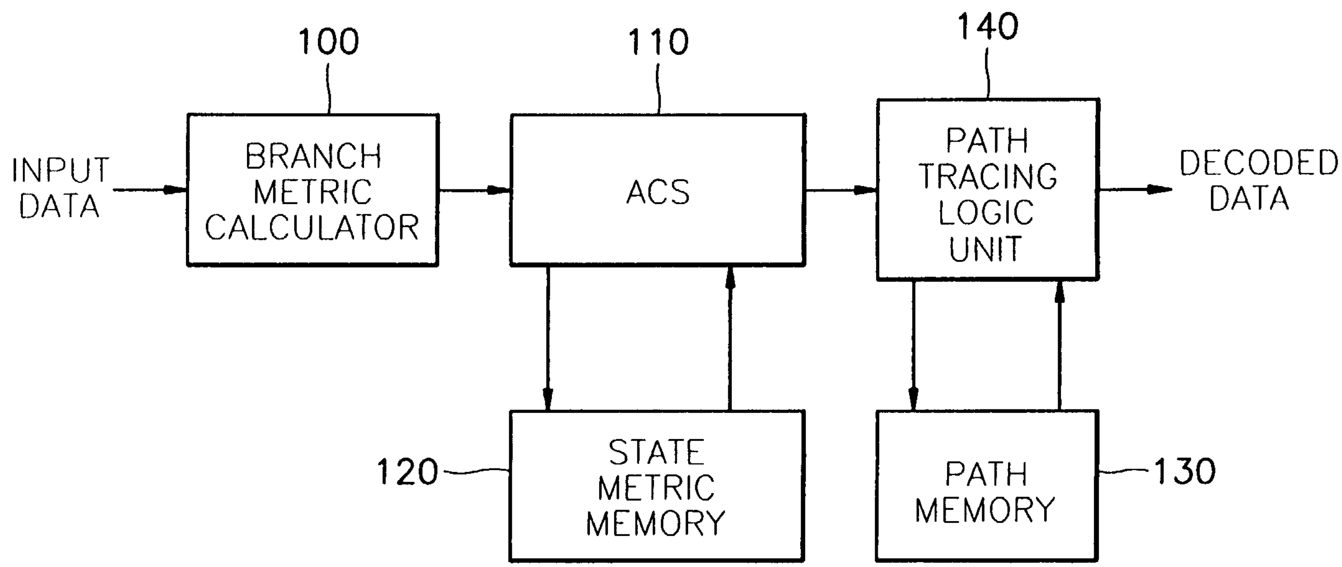
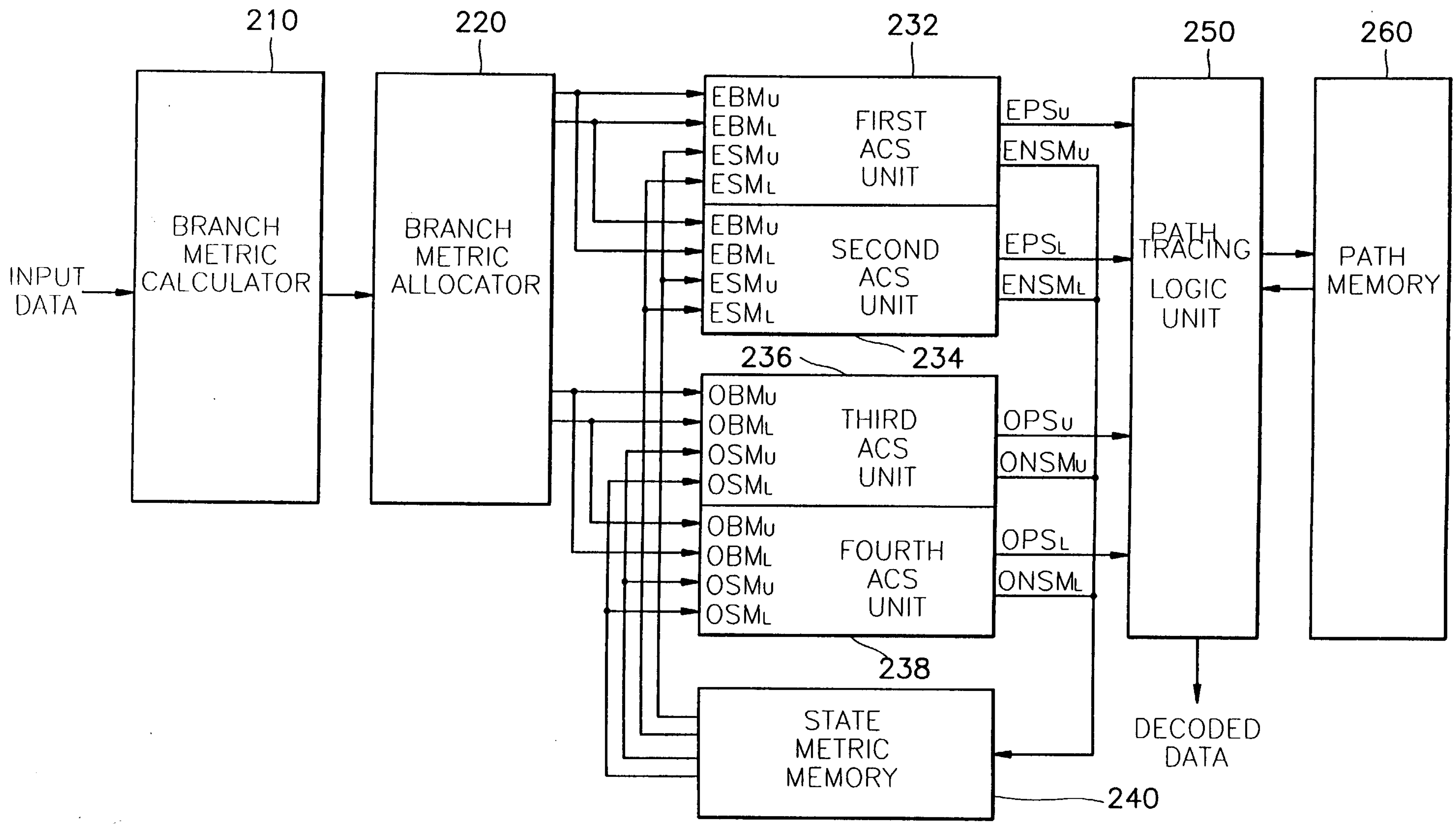


FIG. 2



INPUT DATA
210
BRANCH METRIC CALCULATOR
220
BRANCH METRIC ALLOCATOR
232
EBMU
EBML
ESMU
ESML
FIRST ACS UNIT
EBMU
EBML
ESMU
ESML
SECOND ACS UNIT
234
236
OBMU
OBML
OSMU
OSML
THIRD ACS UNIT
OBMU
OBML
OSMU
OSML
FOURTH ACS UNIT
238
STATE METRIC MEMORY
240
EPSU
ENSMU
EPSL
ENSML
OPSU
ONSMU
OPSL
ONSML
250
PATH TRACING LOGIC UNIT
DECODED DATA
260
PATH MEMORY

FIG. 3

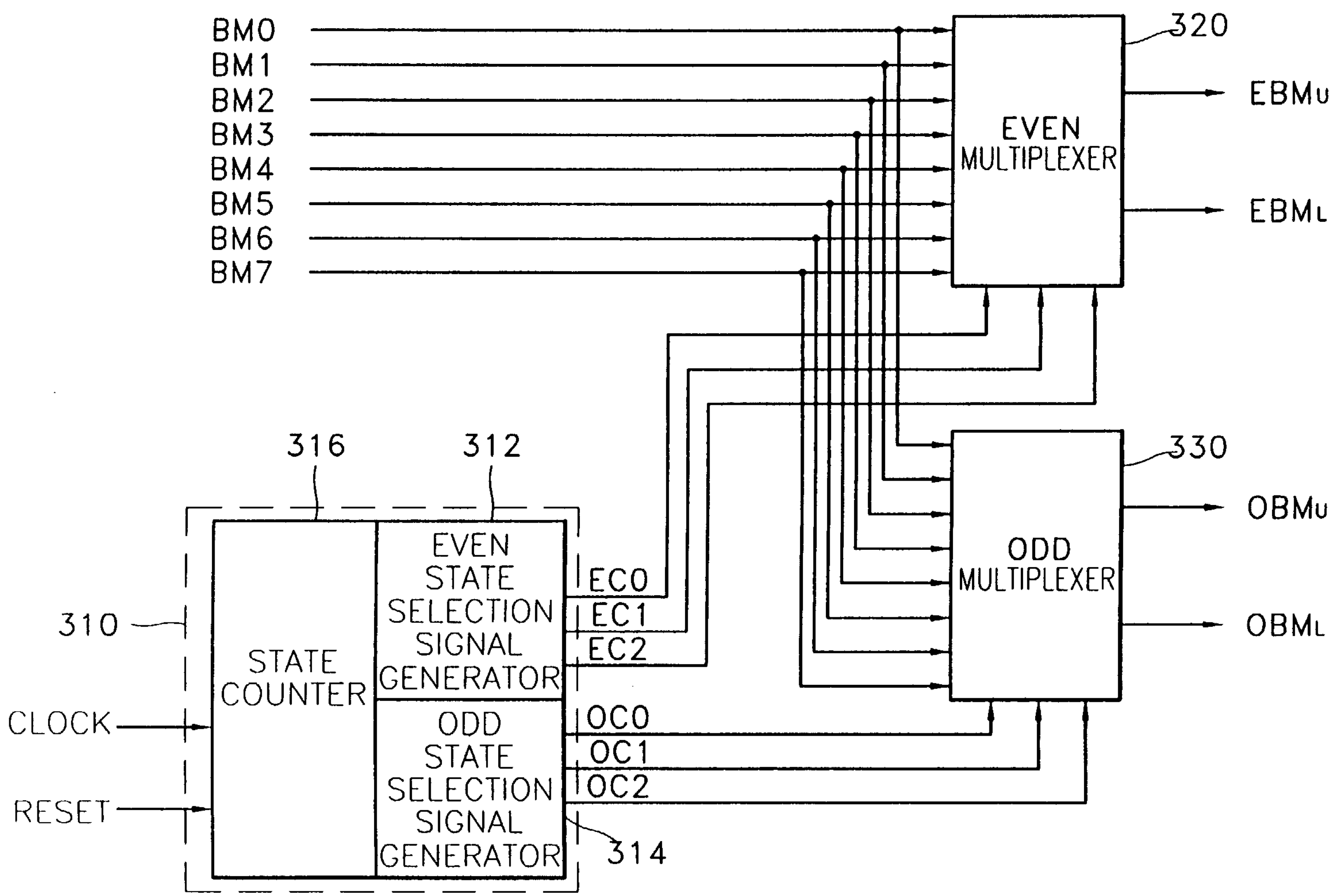

BM0
BM1
BM2
BM3
BM4
BM5
BM6
BM7
320
EVEN MULTIPLEXER
EBMu
EBML
330
ODD MULTIPLEXER
OBMu
OBML
316
312
310
STATE COUNTER
EVEN STATE SELECTION SIGNAL GENERATOR
ODD STATE SELECTION SIGNAL GENERATOR
CLOCK
RESET
EC0
EC1
EC2
OC0
OC1
OC2
314

FIG. 4

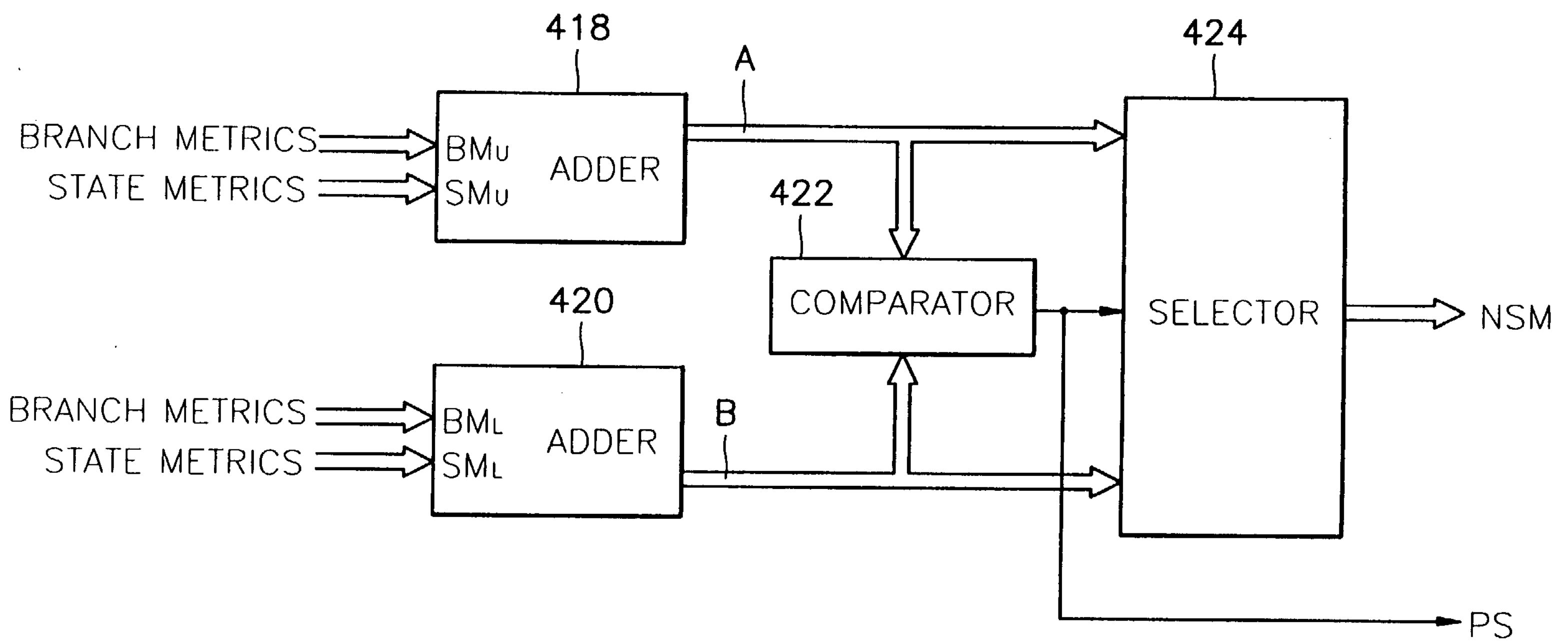

418
420
422
424
BRANCH METRICS
STATE METRICS
BRANCH METRICS
STATE METRICS
BMU
SMU
ADDER
BML
SML
ADDER
A
B
COMPARATOR
SELECTOR
NSM
PS

FIG. 5

K=9, R=1/3, G = (557,663,711), Trellis Diagram

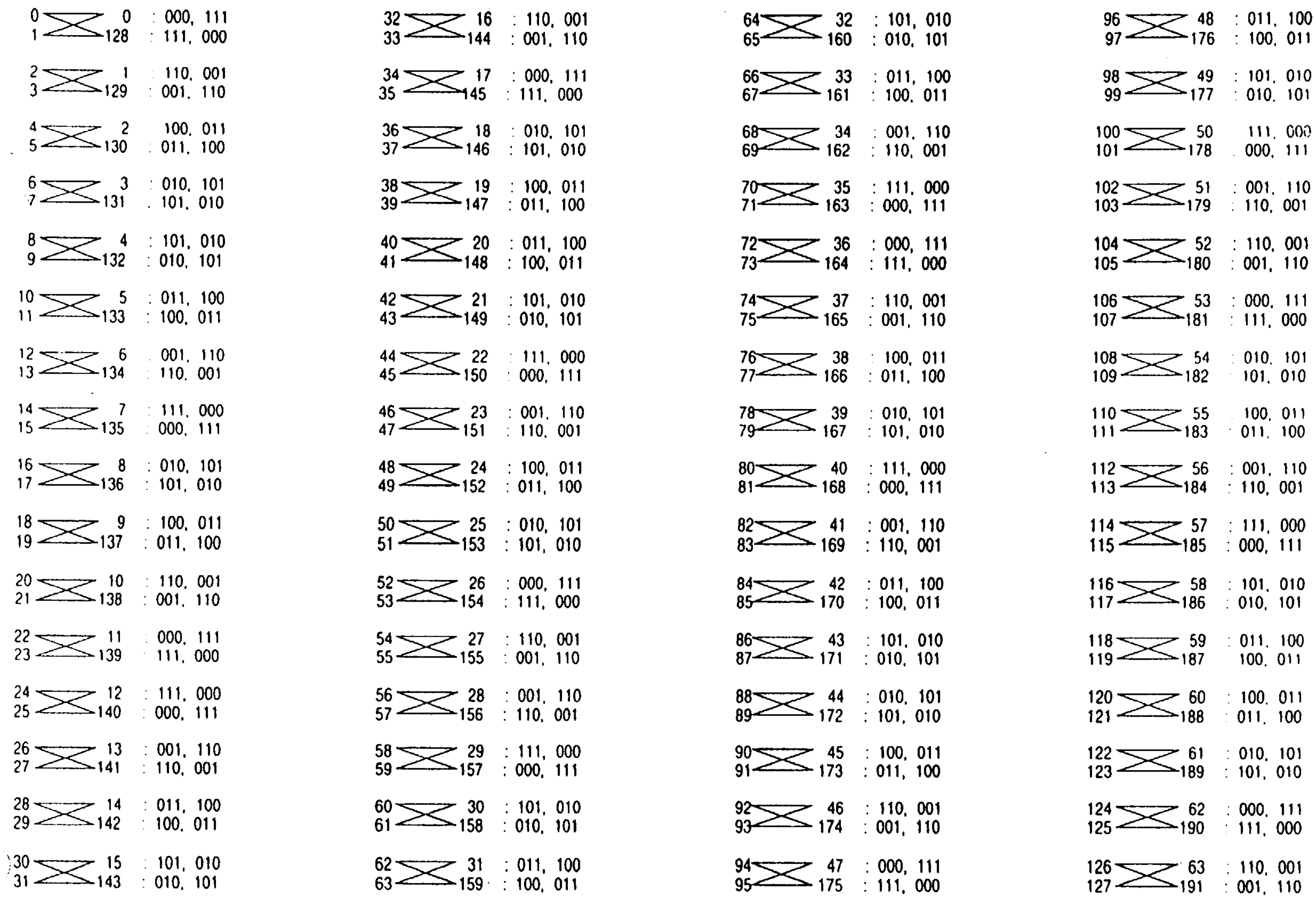


FIG. 5 (cont'd)

128	64	011, 100
129	192	100, 011
130	65	101, 010
131	193	010, 101
132	66	111, 000
133	194	000, 111
134	67	001, 110
135	195	110, 001
136	68	110, 001
137	196	001, 110
138	69	000, 111
139	197	111, 000
140	70	010, 101
141	198	101, 010
142	71	100, 011
143	199	011, 100
144	72	001, 110
145	200	110, 001
146	73	111, 000
147	201	000, 111
148	74	101, 010
149	202	010, 101
150	75	011, 100
151	203	100, 011
152	76	100, 011
153	204	011, 100
154	77	010, 101
155	205	101, 010
156	78	000, 111
157	206	111, 000
158	79	110, 001
159	207	001, 110

160	80	101, 010
161	208	010, 101
162	81	011, 100
163	209	100, 011
164	82	001, 110
165	210	110, 001
166	83	111, 000
167	211	000, 111
168	84	000, 111
169	212	111, 000
170	85	110, 001
171	213	001, 110
172	86	100, 011
173	214	011, 100
174	87	010, 101
175	215	101, 010
176	88	111, 000
177	216	000, 111
178	89	001, 110
179	217	110, 001
180	90	011, 100
181	218	100, 011
182	91	101, 010
183	219	010, 101
184	92	010, 101
185	220	101, 010
186	93	100, 011
187	221	011, 100
188	94	110, 001
189	222	001, 110
190	95	000, 111
191	223	111, 000

192	96	110, 001
193	224	001, 110
194	97	000, 111
195	225	111, 000
196	98	010, 101
197	226	101, 010
198	99	100, 011
199	227	011, 100
200	100	011, 100
201	228	100, 011
202	101	101, 010
203	229	010, 101
204	102	111, 000
205	230	000, 111
206	103	001, 110
207	231	110, 001
208	104	100, 011
209	232	011, 100
210	105	010, 101
211	233	101, 010
212	106	000, 111
213	234	111, 000
214	107	110, 001
215	235	001, 110
216	108	001, 110
217	236	110, 001
218	109	111, 000
219	237	000, 111
220	110	101, 010
221	238	010, 101
222	111	011, 100
223	239	100, 011

224	112	000, 111
225	240	111, 000
226	113	110, 001
227	241	001, 110
228	114	100, 011
229	242	011, 100
230	115	010, 101
231	243	101, 010
232	116	101, 010
233	244	010, 101
234	117	011, 100
235	245	100, 011
236	118	001, 110
237	246	110, 001
238	119	111, 000
239	247	000, 111
240	120	010, 101
241	248	101, 010
242	121	100, 011
243	249	011, 100
244	122	110, 001
245	250	001, 110
246	123	000, 111
247	251	111, 000
248	124	111, 000
249	252	000, 111
250	125	001, 110
251	253	110, 001
252	126	011, 100
253	254	100, 011
254	127	101, 010
255	255	010, 101

VITERBI DECODER

The present invention relates to a Viterbi decoder, and more particularly, to a Viterbi decoder having a plurality of add-compare-select units for adding, comparing, and selecting branch metrics and state metrics, and outputting decoded data from a selection signal representing an optimum path.

Generally, a Viterbi decoder uses a Viterbi algorithm which depends on maximum likelihood decoding when a received convolutional codeword is to be decoded. The Viterbi algorithm compares a plurality of known code sequences with received code sequences, selects a path having the shortest code distance as a maximum likelihood path, and obtains decoded data corresponding to the selected path. The Viterbi algorithm exhibits an excellent error correction ability, thus it is widely used in satellite communications, ground network communications, and mobile communications.

Figure 1 is a schematic block diagram of a conventional Viterbi decoder. The conventional Viterbi decoder of Figure 1 has a branch metric calculator 100, an ACS unit 110, a state metric memory 120, a path memory 130, and a logic unit 140.

The branch metric calculator 100 calculates a Euclidean distance or a Hamming distance between received data and a codeword to be transmitted. The ACS unit 110 adds and compares the branch metrics calculated in the branch metric calculator 100 and state metrics, and selects a survival branch for each state which is the most approximate to the code order of the received data. That is, in the ACS unit 110, calculated branch metrics are added to previous state metrics in an adder according to a trellis diagram, currently received state metrics are compared in a comparator, and small state metrics are selected in a selector, wherein the selected state metrics are stored in the state metric memory 120. Here, selected path selection signals are stored in the path memory 130 after passing through the path tracing logic unit 140. Meanwhile, the state metric memory 120 stores a current state metric. The path tracing logic unit 140 traces path information stored in the path memory 130 for looking for a state having the largest maximum likelihood, finds the most approximate path to that of data sent from a transmitting encoder (not shown), and outputs decoded data. A system employing a code division multiple access (CDMA) communications method uses a Viterbi decoder including a single ACS unit. It usually uses a convolutional codeword with a constrained length K of 9, and thus the number of states is 2^{9-1}, namely, 256. Therefore, the single ACS unit 110 performs addition, comparison, and selection on 256 states for one symbol. As a result, operations for a plurality of channels should be performed, thereby constraining a decoding speed.

It is an aim of preferred embodiments of the present invention to provide a Viterbi decoder employing a Viterbi algorithm for simultaneously processing a plurality of channels by using a plurality of add-compare-select (ACS) units for adding, comparing, and selecting branch metrics and state metrics of received data.

According to a first aspect of the invention, there is provided a Viterbi decoder for receiving convolutional data and correcting an error in the received data, comprising: a branch metric calculating unit for receiving the convolutional data and calculating a plurality of branch metrics; a branch metric allocating unit for allocating the plurality of branch metrics as even and odd branch metrics; a state metric storing unit for storing a current state metric and allocating a plurality of state metrics as even and odd state metrics; first and second ACS units for performing addition, comparison, and selection on the even branch and state metrics, and selecting paths having optimum distances; third and fourth ACS units for performing addition, comparison, and selection on the odd branch and state metrics, and selecting paths having optimum distances; a path tracing logic unit for tracing the path selection information selected in the first through fourth ACS units, and outputting decoded data to find out a most approximate path to the received data path; and a path storing unit for storing a path selection signal generated in the path tracing logic unit.

Preferably, said first through fourth ACS units receive said branch and state metrics in parallel and perform addition and comparison on said metrics.

Each of said first through fourth ACS units may comprise first and second adders for adding branch and state metrics, a comparator for comparing the output values of said first and second adders, and a selector for receiving the outputs of said first and second adders and selecting an optimum state metric.

Preferably, said selector selects said added value by the path selection signal output by comparing values added in said first and second adders in said comparator.

Said branch metric allocating unit preferably comprises: a controller for generating even and odd state selection signals according to a generative equation; a first multiplexer for selecting the branch metrics for addition, comparison, and selection for even states among said plurality of branch metrics according to said even state selection signal of said controller; and a second multiplexer for selecting the branch metrics for addition, comparison, and selection for odd states among said plurality of branch metrics according to said odd state selection signal of said controller.

Preferably, said controller comprises a state counter for calculating a state value, and a state selection signal generator for generating the even and odd state selection signals.

For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 is a block diagram of a conventional Viterbi decoder;

Figure 2 illustrates an embodiment of a Viterbi decoder according to the present invention;

Figure 3 is a detailed block diagram of the branch metric allocator of Figure 2;

Figure 4 is a detailed block diagram of the add-compare-select (ACS) unit of Figure 2; and

Figure 5 is a trellis diagram for Viterbi decoding as adopted in embodiments of the present invention.

Referring to Figure 2, a Viterbi decoder of an embodiment of the present invention has a branch metric calculator 210 for receiving a code, calculating each branch metric from the received code, and outputting eight branch metrics BM0, BM1, BM2, BM3, BM4, BM5, BM6, and BM7, a branch metric allocator 220 for allocating the branch metrics output from the branch metric calculator 210 into EBM_U, EBM_L, OBM_U, and OBM_L, first through fourth ACS units 232, 234, 236, and 238 for adding and comparing the branch metrics output from the branch metric allocator 220 and the state metrics output from a state metric memory 240, selecting an optimum path, and outputting new static metrics, the state metric memory 240 for storing the new state metrics and allocating four state metrics as ESM_U, ESM_L OSM_U, and OSM_L to the first through fourth ACS units 232, 234, 236, and 238, a path tracing logic unit 250 for tracing path selection information selected in the first through fourth ACS units 232, 234, 236, and 238, seeking the most approximate path of the received data, and outputting decoded data, and a path memory 260 for storing a path selection signal selected in the path tracing logic unit 250.

In the embodiment of the present invention, Viterbi decoding at a code rate of 1/3 and a constraint length of 9 is given. Figure 5 shows state transitions for the Viterbi decoding. That is, Figure 5 shows state transitions for 256 states. For example, 0 and 1 denote the number of a previous state, respectively. 0 and 128 denote the number of a current state, respectively. 000 and 111 denote an upper codeword CW_U, respectively. 111 and 000 denote a lower codeword CW_L, respectively.

As shown in Figure 2, the branch metric calculator 210 calculates a Euclidean distance or a Hamming distance between received data and a transmittable codeword. That is, the Euclidean distance between the received data and a codeword (000, 001,...,111) is calculated, and BM0, BM1, BM2, BM3, BM4, BM5, BM6, and BM7 are output. The branch metric allocator 220 allocates the branch metrics calculated from the received data as EBM_U, EBM_L, OBM_U, and OBM_L. Here, E and O represent even and odd numerical data, and BM_U and BM_L are the distances between the upper codeword CW_U and the lower codeword CW_L of Figure 5 and the received data, respectively. The four ACS units 232-238 receive the respective branch metrics allocated in the branch metric allocator 220. The state metric memory 240 stores new state metrics output from the first through fourth ACS units 232-238 and allocates four state metrics ESM_U, ESM_L, OSM_U, and OSM_L to the first through fourth ACS units 232-238. Here, in the Viterbi decoder using the Viterbi algorithm, if a code rate is 1/3(information bits/code bits) and a constraint length is 9, the number of states is 2^{9-1}, namely, 256. Each ACS unit performs 64 (256/4) operations on a single received datum. Therefore, the first and second ACS units 232 and 234 perform operations for even states among the 256 states, whereas the third and fourth ACS units 236 and 238 perform operations for odd states among the 256 states. That is, the first ACS unit 232 receives four signals (EBM_U, EBM_L, ESM_U, and ESM_L) of branch and state metrics and performs operations for one half of even upper states 0, 2, 4,..., 126, and the second ACS unit 234 receives four signals (EBM_U, EBM_L, ESM_U, and ESM_L) of the branch and state metrics and performs operations for the other half of the even lower states 128, 130, 132,..., 254. The third ACS unit 236 receives four signals (OBM_U, OBM_L, OSM_U, and OSM_L) of the branch and state metrics and performs operations for one half of odd upper states 1, 3, 5,..., 127, and the fourth ACS unit 238 receives four signals (OBM_U, OBM_L, OSM_U, and OSM_L) of the branch and state metrics and performs operations for the other half of odd upper states 129, 131, 133, 135,...255. Therefore, the first through fourth ACS 232-238 receive the branch and state metrics in parallel and sequentially perform operations for states(0, 128, 1, 129), (2, 130, 3, 131),...,(126, 254, 127, 255) as shown in Figure 5. Here, to sequentially perform the operations, the branch metrics and state metrics are input to the ACS units, respectively, as follows. BM_U of the first ACS unit 232 is equal to BM_L of the second ACS unit 234, BM_L of the first ACS unit 232 to BM_U of the second ACS unit 234, BM_U of the third ACS unit 236 to BM_L of the fourth ACS unit 238, and BM_L of the third ACS unit 236 to BM_U of the fourth ACS unit 238 (see table 1). Hence, the metrics of branches transited from states 0, 4, 8,...,240, 244, 248, 252 to states 0, 2, 4, 6,..., 120, 122, 124, 126 are received through the BM_U terminal of the first ACS unit 232 and the BM_L terminal of the second ACS unit 234. The metrics of branches transited from states 0, 4, 8,...,240, 244, 248, 252 to states 128, 130, 132,...,248, 250, 252, 254 are received through the BM_L terminal of the first ACS unit 232 and the BM_U terminal of the second ACS unit 234.

In addition, the metrics of branches transmitted from states 0, 4, 8, 12...,240, 244, 248, 252 to states

0, 2, 4, 6,...,120, 122, 124, 126 are received through the SM_U terminal of the first ACS unit 232. The metrics of branches transmitted from states 0, 4, 8, 12,...,240, 244, 248, 252 to states 128, 130, 132, 134,...,248, 250, 252, 254 are received through the SM_L terminal of the second ACS unit 234.

The metrics of branches transited from states 2, 6, 10,...,242, 246, 250, 254 to states 1, 3, 5, 7,..., 121, 123, 125, 127 are received through the BM_U terminal of the third ACS unit 236 and the BM_L terminal of the fourth ACS unit 238. The metrics of branches transited from states 2, 6, 10,...,242, 246, 250, 254 to states 129, 131, 133,...,249, 251, 253, 255 are received through the BM_L terminal of the third ACS unit 236 and the BM_U terminal of the fourth ACS unit 238.

In addition, the metrics of branches transmitted from states 0, 4, 8, 12,...240, 244, 248, 252 to states 0, 2, 4, 6,...,120, 122, 124, 126 are received through the SM_U terminal of the first ACS unit 232. The metrics of branches transmitted from states 1, 5, 9, 13,...241, 245, 249, 253 to states 0, 2, 4, 6,...,120, 122, 124, 126 are received through the SM_L terminal of the first ACS unit 232. The metrics of branches transmitted from states 0, 4, 8, 12,...240, 244, 248, 252 to states 128, 130, 132, 134,...,248, 250, 252, 254 are received through the SM_U terminal of the second ACS unit 234. The metrics of branches transmitted from states 1, 5, 9, 13,...,241, 245, 249, 253 to states 128, 130, 132, 134,...,248, 250, 252, 254 are received through the SM_L terminal of the second ACS unit 234.

Signals $ENSM_U$ and $ENSM_L$ output from the first and second ACS units 232 and 234 are output signals representing new state metrics for even states, and signals EPS_U and EPS_L are path selection signals for the even states. Signals $ONSM_U$ and $ONSM_L$ output from the third and fourth ACS units 236 and 238 are output signals representing new state metrics for odd states, and signals OPS_U and OPS_L are path selection signals for the odd states.

The path selection signals output from the first through fourth ACS units 232-238 represent data decoded by the Viterbi algorithm through the path tracing logic unit 250 and the path memory 260.

Figure 3 is a detailed schematic diagram of the branch metric allocator 220 of Figure 2.

The branch metric allocator 220 has a controller 310 including a state counter 316, an even state selection signal generator 312, and an odd state selection signal generator 314 for receiving a clock signal and a reset signal and outputting even state selection signals EC0, EC1, and EC2 and odd state selection signals OC0, OC1, and OC2, and even and odd multiplexers 320 and 330 for selecting necessary signals among the branch metrics BM0, BM1, BM2, BM3, BM4, BM5, BM6, and BM7 by means of the state selection signals output from the controller 310.

As shown in Table 1, the even branch metrics EBM_U and EBM_L and the odd branch metrics OBM_U and OBM_L of Figure 2 are selected in each pair from the branch metrics BM0, BM1, BM2, BM3, BM4, BM5, BM6, and BM7 which are output from the branch metric allocator 220 of Figure 2 through the even and odd multiplexers 320 and 330 using the even control signals EC0, EC1, and EC2 and the odd control signals OC0, OC1, and OC2 which are output from the controller 310 of Figure 3 as selection control signals, respectively.

The even and odd multiplexers 320 and 330 of Figure 3 operate as outlined in Table 1. Here, selection signals C0, C1, and C2 of the multiplexers are the even selection signals EC0, EC1, and EC2, or the odd selection signals OC0, OC1, and OC2. Branch metrics BM_U and BM_L selected by selection signals C_0, C_1, and C_2 are EBM_U, EBM_L or OBM_U, OBM_L.

The even control signals EC0, EC1, and EC2 and the odd control signals OC0, OC1, and OC2 to be used as selection signals of the even and odd multiplexers 320 and 330 are output from the even and odd state selection signal generators 312 and 314, respectively, of the controller 310.

The even and odd state selection signal generators 312 and 314 output their respective codewords according to a generative equation of a convolutional encoder (not shown) using a value of the state counter 316.

(Table 1)

C0 C1 C2	(BM_U, BM_L)
0 0 0	(BM_0, BM_7)
0 0 1	(BM_1, BM_6)
0 1 0	(BM_2, BM_5)
0 1 1	(BM_3, BM_4)
1 0 0	(BM_4, BM_3)

1 0 1	(BM_5, BM_2)
1 1 0	(BM_6, BM_1)
1 1 1	(BM_7, BM_0)

Figure 4 is a detailed block diagram of the ACS unit of Figure 2.

The device of Figure 4 includes a first adder 418, a second adder 420, a comparator 422, and a selector 424.

The first and second adders 418 and 420 of Figure 4 add received branch and state metrics and output data values A and B, respectively, as described with reference to Figure 2. The comparator 422 compares A with B, outputs 0 as a path selection signal if data A is not larger than data B, and outputs 1 as a path selection signal (PS) if data A is larger than data B. Meanwhile, the selector 424 receives data A and B, selects one of A and B according to the path selection signal of the comparator 422 and outputs the selected data as a new state metric (NSM).

As described above, according to embodiments of the present invention, the ACS units in the Viterbi decoder receive branch and state metrics and operate a plurality of states at one time, thereby decoding a plurality of channels at an increased speed.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. A Viterbi decoder for receiving convolutional data and correcting an error in the received data, comprising:

a branch metric calculating unit for receiving said convolutional data and calculating a plurality of branch metrics;

a branch metric allocating unit for allocating said plurality of branch metrics as even and odd branch metrics;

a state metric storing unit for storing a current state metric and allocating a plurality of state metrics as even and odd state metrics;

first and second add-compare-select (ACS) units for performing addition, comparison, and selection on said even branch and state metrics, and selecting paths having optimum distances;

third and fourth ACS units for performing addition, comparison, and selection on said odd branch and state metrics, and selecting paths having optimum distances;

a path tracing logic unit for tracing said path selection information selected in said first through fourth ACS units to find out a most approximate path to the received data, and outputting decoded data; and

a path storing unit for storing a path selection signal generated in said path tracing logic unit.

2. A Viterbi decoder as claimed In claim 1, wherein said first through fourth ACS units receive said branch and state metrics in parallel and perform addition and comparison on said metrics.

3. A Viterbi decoder as claimed in claim 1 or 2, wherein each of said first through fourth ACS units comprises first and second adders for adding branch and state metrics, a comparator for comparing the output values of said first and second adders, and a selector for receiving the outputs of said first and second adders and selecting an optimum state metric.

4. A Viterbi decoder as claimed in claim 3, wherein said selector selects said added value by the path selection signal output by comparing values added in said first and second adders in said comparator.

5. A Viterbi decoder as claimed in claim 1, 2, 3 or 4, wherein said branch metric allocating unit comprises:

a controller for generating even and odd state selection signals according to a generative equation;

a first multiplexer for selecting the branch metrics for addition, comparison, and selection for even states among said plurality of branch metrics according to said even state selection signal of said controller; and

a second multiplexer for selecting the branch metrics for addition, comparison, and selection for odd states among said plurality of branch metrics according to said odd state selection signal of said controller.

6. A Viterbi decoder as claimed in claim 5, wherein said controller comprises a state counter for calculating a state value, and a state selection signal generator for generating the even and odd state selection signals.

7. A Viterbi decoder substantially as herein described with reference to Figure 2 onwards.

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Application No: GB 9705479.5
Claims searched: 1 to 7

Examiner: Ken Long
Date of search: 9 June 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4P (PRV)

Int Cl (Ed.6): H03M (13/00)

Other: ONLINE :- WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP 0441968 A1	FUJITSU (column 4 line 40 to column 5 line 9)	None
A	EP 0138598 A2	NEC (page 6 line 6 to page 7 line 15)	None
A	US 5414738	MOTOROLA (column 7 line 30 to column 8 line 16)	None
A	US 5027374	MOTOROLA (column 3 line 63 to column 4 line 44)	None
A	JP 08340262 A	NEC	None

X Document indicating lack of novelty or inventive step
Y Document indicating lack of inventive step if combined with one or more other documents of same category.
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