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(54) Method for driving liquid crystal panel

Steuerverfahren für eine Flüssigkristallanzeigetafel

Méthode de commande d'un panneau d'affichage à cristaux liquides

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Description

FIELD OF THE INVENTION

The present invention relates to a method for driving a liquid crystal panel, and more particularly to a method for driving a liquid crystal panel using a ferroelectric liquid crystal (hereinafter referred to as a FLC).

DESCRIPTION OF THE RELATED ART

Fig. 2 is a schematic section view showing the structure of a FLC panel. More specifically, glass substrates 5a and 5b are provided opposite to each other. A plurality of signal electrodes S are provided in parallel with one another on the surface of one glass substrate 5a. The signal electrodes S are transparent and consist of indium tin oxide (hereinafter referred to as ITO) and the like. The signal electrodes S are covered by a transparent insulating film 6a which consists of SiO_2 and the like.

A plurality of scanning electrodes L are provided in parallel with one another and perpendicularly to the signal electrodes S on the surface of the other glass substrate 5b which is opposite to the signal electrodes S. The scanning electrodes L are transparent and consist of ITO and the like. The scanning electrodes L are covered by a transparent insulating film 6b which consists of SiO_2 and the like.

On the insulating films 6a and 6b are formed transparent orientation films 7a and 7b which are subjected to rubbing processing and consist of polyvinyl alcohol and the like. The glass substrates 5a and 5b are stuck together by a sealing agent 8 with an inlet left. A FLC 9 is introduced into a space interposed between the orientation films 7a and 7b through the inlet by vacuum injection. Then, the inlet is sealed by the sealing agent 8.

The glass substrates 5a and 5b thus stuck together are interposed between polarizing plates 10a and 10b. The polarizing plates 10a and 10b are provided in such a manner that their polarizing axes are perpendicular to each other.

Fig. 3 is a plan view showing the schematic structure of a FLC display (hereinafter referred to as a FLCD) 4 in which the scanning electrodes L and signal electrodes S of the FLC panel 1 are connected to a scanning side drive circuit 11 and a signal side drive circuit 12 respectively.

For simplicity, there will be described the FLCD 4 which has 16 scanning electrodes L and 16 signal electrodes S, that is, which is formed by 16 x 16 pixels. Each scanning electrode L is coded by adding a subscript i (i = 0 to F) to a character L. Each signal electrode S is coded by adding a subscript j (j = 0 to F) to a character S. In the following description, a pixel in a portion or a cell where a given scanning electrode Li and a given signal electrode Sj intersect each other is indicated at Aij.

The scanning side drive circuit 11 serves to apply voltages to the scanning electrodes L and includes an address decoder, a latch and an analog switch which are not shown. More specifically, the scanning side drive circuit 11 applies a selection voltage V_{c1} to the scanning electrode Li corresponding to an address Ax which is specified, and applies a non-selection voltage V_{c0} to other scanning electrodes Lk ($k \neq i$). The signal side drive circuit 12 serves to apply voltages to the signal electrodes S and includes a shift register, a latch and an analog switch which are not shown. More specifically, the signal side drive circuit 12 applies an active voltage V_{s1} to the signal electrode S in which data DATA corresponds to "1", and applies a non-active voltage V_{s0} to the signal electrode S in which the data DATA corresponds to "0".

As shown in Fig. 7 (B), a FLC molecule 101 forming the pixel Aij has a spontaneous polarization Ps perpendicularly to the direction of a major axis thereof, receives a force which is proportional to a vector product composed of an electric field E and the spontaneous polarization Ps, and is moved on the surface of a circular cone 102. The electric field E is produced by the voltages of the scanning electrode L and signal electrode S. The circular cone 102 has an apex angle 2θ which is twice as great as a tilt angle. The FLC molecule 101 has two stable states. When moved to an axis 107 shown in Fig. 7 (A) by the electric field E, the FLC molecule 101 is brought into a stable state 105. When moved to an axis 106 by the electric field E, the FLC molecule 101 is brought into a stable state 104. When the FLC molecule 101 in a given stable state is moved by the electric field E, a restoring force for returning to an original stable state acts on the FLC molecule 101 while the given stable state is not changed.

The other force acting on the FLC molecule is proportional to a difference $\Delta\varepsilon$ of permittivities in the directions of major and minor axes and to square of the electric field E. More specifically, a force F acting on the FLC molecule is as follows.

$$F = K0 \times Ps \times E + K1 \times \Delta\varepsilon \times E^2 \qquad (1)$$

When a FLC material having a negative dielectric anisotropy $\Delta\varepsilon$ is sealed in a panel, a force produced by the effect of the dielectric anisotropy $\Delta \varepsilon < 0$ is much greater than a force produced by the effect of the spontaneous polarization Ps if the electric field is not greater than Ee. Both forces are almost equal to each other if the electric field is greater than Ef.

For example, Japanese Unexamined Patent Publication Nos. 56933/1987, 280824/1987 and 24234/1989 have disclosed a method for driving a FLC panel utilizing the foregoing. Fig. 17 shows a graph which represents the relationship between a voltage and a response speed of the FLC material disclosed in the Japanese Unexamined Patent Publication No. 24234/1989.

Fig. 16 shows a driving method disclosed in the Japanese Unexamined Patent Publication No. 24234/1989. The stable state of a FLC molecule forming a pixel Aij is changed or rewritten into another stable state in the following manner. More specifically, when a voltage waveform shown in Fig. 16 (1) is applied to a scanning electrode Li, a voltage waveform shown in Fig. 16 (3) is applied to a signal electrode Sj and a voltage waveform shown in Fig. 16 (5) is applied to the FLC molecule forming the pixel Aij. Consequently, the stable state of the FLC molecule is changed or rewritten into another stable state. The stable state of the FLC molecule forming the pixel Aij is changed into a further stable state in the following manner. More specifically, when the voltage waveform shown in Fig. 16 (1) is applied to the scanning electrode Li, a voltage waveform shown in Fig. 16 (4) is applied to the signal electrode Sj and a voltage waveform shown in Fig. 16 (6) is applied to the FLC molecule forming the pixel Aij. Consequently, the stable state of the FLC molecule is changed into the further stable state. When the stable state of a FLC molecule forming a pixel Akj ($k \neq i$) is changed, a voltage waveform shown in Fig. 16 (2) is applied to the scanning electrode Li and the voltage waveform shown in Fig. 16 (3) or (4) is applied to the signal electrode Sj. Accordingly, a voltage waveform shown in Fig. 16 (7) or (8) is applied to the FLC molecule forming the pixel Aij so that the stable state of the FLC molecule is not changed.

In the case that the absolute value of a voltage -Va or Va of Fig. 16 (6) or (5) is about 30 v shown in Fig. 17 and a voltage is in an area where the effect of a dielectric anisotropy $\Delta \varepsilon < 0$ is smaller than that of the spontaneous polarization Ps, and the absolute value of a voltage (-Va - 2Vb) or (Va + 2Vb) of Fig. 16 (5) or (6) is about 50 v shown in Fig. 17 and a voltage is in an area where the effect of the dielectric anisotropy $\Delta \varepsilon < 0$ is substantially equal to that of the spontaneous polarization Ps, the above-mentioned driving method can be executed. The reason is that a force acting on the FLC molecule by virtue of the former voltage is greater than a force acting on the FLC molecule by virtue of the latter voltage. The foregoing can be presumed because a response time shown in Fig. 17 has a minimum value when a voltage is 30 to 40 v and the response time is greater when the voltage is greater than 40 v as compared with the case where the voltage is 30 v.

In FLC' 91 Institute held in U.S.A., RSRE Co., Ltd. published "The JOERS/ALVEY Ferroelectric Multiplexing Scheme" for another driving method using a FLC material SCE8 which has a negative dielectric anisotropy and is manufactured by BDH Co., Ltd. Fig. 15 shows the relationship between a voltage and a memory pulse width of the FLC material SCE8 disclosed in the above-mentioned paper. Data shown in Fig. 15 (a) is obtained by applying a pulse on which a bias voltage of ± 10 v is superposed as shown in Fig. 14 (B). Data shown in Fig. 15 (b) is obtained by applying a pulse on which a bias voltage of ± 0 v is superposed as shown in Fig. 14 (A). Referring to the driving method disclosed in the above-mentioned paper, two fields are necessary for rewriting a screen. Driving waveforms shown in Fig. 13 (A) are applied in a first field and driving waveforms shown in Fig. 13 (B) are applied in a second field.

The stable state of the FLC molecule forming the pixel Aij is changed into another stable state in the following manner. More specifically, when a selection voltage shown in Fig. 13 (A) (1) is applied to a scanning electrode Li in the first field, a rewriting voltage shown in Fig. 13 (A) (3) is applied to the signal electrode Sj and a voltage waveform shown in Fig. 13 (A) (5) is applied to the FLC molecule forming the pixel Aij so as to change the stable state of the FLC molecule into another stable state. Furthermore, when a selection voltage shown in Fig. 13 (B) (1) is applied to the scanning electrode Li in the second field, a holding voltage shown in Fig. 13 (B) (4) is applied to the signal electrode Sj and a voltage waveform shown in Fig. 13 (B) (6) is applied to the FLC molecule forming the pixel Aij so as not to change the stable state of the FLC molecule.

The stable state of the FLC molecule forming the pixel Aij is changed into a further stable state in the following manner. More specifically, when the selection voltage shown in Fig. 13 (A) (1) is applied to the scanning electrode Li in the first field, a holding voltage shown in Fig. 13 (A) (4) is applied to the signal electrode Sj and a voltage waveform shown in Fig. 13 (A) (6) is applied to the FLC molecule forming the pixel Aij so as not to change the stable state of the FLC molecule. Furthermore, when the selection voltage shown in Fig. 13 (B) (1) is applied to the scanning electrode Li in the second field, a rewriting voltage shown in Fig. 13 (B) (3) is applied to the signal electrode Sj and a voltage waveform shown in Fig. 13 (B) (5) is applied to the FLC molecule forming the pixel Aij so as to change the stable state of the FLC molecule into the further stable state.

In case the stable state of a FLC molecule forming a pixel Akj ($k \neq i$) is changed, a non-selection voltage shown in Fig. 13 (A) (2) is applied to the scanning electrode Li, the voltage waveform shown in Fig. 13 (A) (3) or (4) is applied to the signal electrode Sj and a voltage waveform shown in Fig. 13 (A) (7) or (8) is applied to the FLC molecule forming the pixel Aij in the first field. In the second field, when a non-selection voltage shown in Fig. 13 (B) (2) is applied to the scanning electrode Li, the voltage waveform shown in Fig. 13 (B) (4) or (3) is applied to the signal electrode Sj and a voltage waveform shown in Fig. 13 (B) (8) or (7) is applied to the FLC molecule forming the pixel Aij. Even though a voltage is applied, the stable state of the FLC molecule is not changed.

In case a voltage (-Vs + Vd) or (Vs - Vd) shown in Fig. 13 (A) (5) or Fig. 13 (B) (5) is in an area where the effect of the dielectric anisotropy $\Delta \varepsilon < 0$ is smaller than that of the spontaneous polarization Ps, and a voltage (-Vs - Vd) or (Vs + Vd) shown in Fig. 13 (A) (6) or Fig. 13 (B) (6) is in an area where the effect of the dielectric anisotropy $\Delta \varepsilon < 0$ is almost equal to that of the spontaneous polarization Ps, the above-mentioned driving method can be executed. The reason is that a force acting on the FLC molecule by virtue of the former voltage is greater than a force acting on the FLC molecule by virtue of the latter voltage. In Fig. 13 (A) (5) or Fig. 13 (B) (5), the polarity of a voltage -Vd or Vd is the same as that of the voltage (-Vs + Vd) or (Vs - Vd). In Fig. 13 (A) (6) or Fig. 13 (B) (6), the polarity of the voltage Vd or -Vd is reverse to that of the voltage (-Vs - Vd) or (Vs + Vd). Consequently, the stable state of the FLC molecule is easy to change by virtue of the voltage (-Vs + Vd) or (Vs - Vd) in the former case, and is hard to change by virtue of the voltage (-Vs - Vd) or (Vs + Vd) in the latter case.

Referring to the paper "The JOERS/ALVEY Ferroelectric Multiplexing Scheme" published by RSRE Co., Ltd. in FLC 91 Institute, the voltage Vs is 50 v and the voltage Vd is 10 v (or 7.5 v) in Fig. 13. Accordingly, when the voltage is about ±60 v, the effect of $\Delta \varepsilon < 0$ is substantially equal to that of Ps.

However, the driving voltage of a commercially available CMOS driver is 25 to 35 v. In order to use the driving method according to the prior art, consequently, it is necessary to develop a FLC material in which the effect of $\Delta \varepsilon < 0$ is substantially equal to that of Ps by virtue of a half voltage as compared with the SCE8 manufactured by BDH Co., Ltd.

If the electric field E is halved in the formula (1), a force acting on the FLC molecule is represented by the following formula (2).

$$F/2 = K1 \times Ps \times E1/2 + K2 \times \Delta \varepsilon \times (E1/2)^2 \qquad (2)$$

The value of the first term involving Ps is made 1/2. The value of the second term involving $\Delta \varepsilon$ is made 1/4. The effect of $\Delta \varepsilon < 0$ is assumed to be almost equal to that of Ps in an electric field E1, though, the effect of $\Delta \varepsilon\ 0 <$ becomes about half of that of Ps in an electric field E1/2.

$\Delta \varepsilon$ is mainly controlled by the base LC of the FLC material. Ps is controlled by a quantity of chiral of the FLC material to be added. If the quantity of chiral to be added is reduced by half or more, it is easy to blend the FLC material which has the same $\Delta \varepsilon$ and half of Ps (on the other hand, it is very difficult to change the value of $\Delta \varepsilon$ because the base LC should be changed into another composition system).

If the above-mentioned FLC material is used and the electric field E is halved in the formula (1), the following formula (3) is obtained.

$$F/4 = K1 \times (Ps/2) \times E1/2 + K2 \times \Delta \varepsilon\ (E1/2)^2 \qquad (3)$$

The value of the first term involving Ps is made 1/4. The value of the second term involving $\Delta \varepsilon$ is made 1/4. Consequently, if the effect of $\Delta \varepsilon < 0$ is substantially equal to that of Ps in the electric field E1 of the FLC material having the spontaneous polarization Ps, the effect of $\Delta \varepsilon < 0$ is equal to that of Ps in the electric field E1/2 of the FLC material having a spontaneous polarization Ps/2.

However, the response speed of the FLC material having the spontaneous polarization Ps/2 is lower than that of the FLC material having the spontaneous polarization Ps by about twice because a force acting on the FLC molecule of the formula (3) is half of that of the formula (2).

Referring to the driving method shown in Fig. 13, a voltage to be effectively used for changing or rewriting the stable state of the FLC molecule is (Vs - Vd) / (Vs + Vd) = 2/3. In the case that the driving method and FLC material having such a low response speed are applied to a dynamic driving method which executes rewriting all pixels with and without the change of display, it takes a lot of time to rewrite pixels on all scanning electrodes from top to bottom on a screen. The time for rewriting comes to have the worst value of a response speed in the case that the displayed contents are changed. Consequently, the response speed is lowered.

Document EP-A-0 306 203 is concerned with determining optimum relative voltage levels and pulse durations on the basis of the empirically observed non-monotonic voltage response for negative dielectric anistropy FLCDs. The effect is considered of an immediately preceding pulse on a certain pixel's response to given switching pulses. In this context this document also consideres pulse sequences applied to pixels sharing electrodes with pixels which are provided with addressing and data signals, and prescribes the choice of voltage values to avoid spurious switching in relation to a response showing both negative and positive gradients.

Further relevant prior art is disclosed in document EP-A-0 435 701.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a driving method for visually increasing a response speed by applying a FLC material having a low response speed to a static driving method to rewrite only pixels on scanning electrodes of which display is changed.

This and other objectives are met by a driving method as defined in claim 1.

In the case of a FLC material having a negative dielectric anisotropy, forces acting on a FLC molecule are almost equal to each other in an electric field Eg where the effect of the dielectric anisotropy $\Delta \varepsilon < 0$ is smaller than that of a spontaneous polarization Ps and in an electric field Eh where the effect of the dielectric anisotropy $\Delta \varepsilon < 0$ is almost equal to that of the spontaneous polarization Ps according to the formula (1).

When an electric field $\pm (Eg + \alpha)$ is applied to the FLC molecule forming a pixel which is formed by the scanning electrode having a non-selection voltage applied thereto and electric fields $(-Eg - \alpha)$, Eh or $(Eg + \alpha)$, and -Eh are applied to the FLC molecule forming a pixel which is formed by the scanning electrode having a selection voltage applied thereto and the signal electrode having a holding voltage applied thereto, a force acting on the FLC molecule in the former case is greater than $(\alpha > 0)$ or almost equal to $(\alpha = 0)$ that in the latter case, and the change of a quantity of transmitted light of the pixel in the former case is greater than or almost equal to that in the latter case.

If the change of a quantity of transmitted light of the pixel formed by the scanning electrode having a selection voltage applied thereto and the signal electrode having a holding voltage applied thereto is smaller than or almost equal to that of the pixel formed by the scanning electrode having a non-selection voltage applied thereto, the change of a quantity of transmitted light of a pixel having no change of display is always constant (the change of the quantity of transmitted light which is less slight is not marked). Consequently, even though the selection voltage is applied to the scanning electrode forming the pixel to change a display state thereof, a flicker cannot be observed.

In case of DTP (Desk Top Publishing) or CAD (Computer Edit Design), the number of scanning electrodes including pixels having the change of display is very small. Consequently, even though there is used a FLC material having a small Pc and a low response speed, an apparent response speed can greatly be increased.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram showing the schematic structure of a display system of a FLCD;

Figure 2 is a section view showing the structure of a FLC panel used in the FLCD;

Figure 3 is a view showing the state in which characters of "A B C D" are displayed on the FLCD;

Figure 4 is a waveform diagram showing output signals from a personal computer;

Figure 5 is a diagram showing data implied by the output signals in a matrix;

Figure 6 is a diagram showing data implied by the output signals in a matrix;

Figure 7 (A) is a view showing the state of a FLC molecule seen from a glass substrate, and Figure 7 (B) is a view showing the state of the FLC molecule in a smectic C phase;

Figure 8 is a block diagram showing the schematic structure of a display controller according to the present invention.

Figure 9 is a waveform diagram showing each applied voltage used for driving a FLC panel according to the present invention;

Figure 10 is a waveform diagram showing each applied voltage used for driving the FLC panel according to the present invention;

Figure 11 is a waveform diagram showing each applied voltage used for driving the FLC panel according to the present invention;

Figure 12 is a waveform diagram showing voltages applied to the scanning electrodes, signal electrodes and pixels of the FLC panel according to the present invention;

Figure 13 is a waveform diagram showing each applied voltage used for driving a FLC panel according to the prior art;

Figure 14 is a voltage waveform diagram showing the conditions of measurement in Figure 15;

Figure 15 is a graph showing the voltage and memory pulse width characteristics of a FLC material having $\Delta \varepsilon < 0$ according to the prior art;

Figure 16 is a waveform diagram showing each applied voltage used for driving the FLC panel according to the prior art;

Figure 17 is a graph showing the voltage and response time characteristics of a FLC material according to another prior art;

Figure 18 is a graph showing the voltage and memory pulse width characteristics of the FLC material which are

actually measured;
Figure 19 is a theoretical diagram for defining the state of orientations based on the relationship between rubbing and chevron directions;
Figure 20 is a waveform diagram showing the combinations of applied voltage waveforms which have equal optical characteristics to be given to pixels in the memory state of "dark" or "bright";
Figure 21 is a waveform diagram for calculating the relationship of voltages among four kinds of pixels in which a selection or non-selection voltage is applied to the scanning electrode and a rewriting or holding voltage is applied to the signal electrode;
Figure 22 is a waveform diagram showing the combinations of applied voltage waveforms which have equal optical characteristics to be given to pixels in the memory state of "dark" or "bright";
Figure 23 is a waveform diagram showing the combinations of applied voltage waveforms which have almost equal optical characteristics to be given to pixels in the memory state of "dark" or "bright";
Figure 24 is a waveform diagram showing the combinations of applied voltage waveforms which have almost equal optical characteristics to be given to pixels in the memory state of "dark" or "bright";
Figure 25 is a graph showing the voltage and memory pulse width characteristics of the FLC material which are actually measured; and
Figure 26 is a graph showing the voltage and memory pulse width characteristics of the FLC material which are actually measured.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

First, there is given a test of Fig. 15 which has been disclosed in a paper published by RSRE Co., Ltd. Since a FLC panel to be used has the same structure as that of a FLC panel 1 shown in Fig. 2, its description will be omitted.

"SCE8" manufactured by BDH Co., Ltd. is used for a FLC material, which has been disclosed in the above-mentioned paper. "PSI-XS012, PSI-XS014, PSI-X7355, PVA and nylon" manufactured by Chisso Co., Ltd. are used for orientation films. The FLC material and orientation films are used for producing five FLC panels in total. Fig. 18 graphically shows the relationship between a voltage and a memory pulse width of each of four FLC panels except for a FLC panel made of nylon, which is measured by voltage waveforms shown in Fig. 14 (A). The basic characteristic of each panel is as follows.

	Pretilt Angle	Tilt Angle θ	Memory angle α
PSI-XS012	2.5°	20.9°	13.8°
PSI-XS014	2.3°	21.4°	14.0°
PSI-X7355	7.5°	21.4°	13.9°
PVA	--0°	22.0°	11.9°
Nylon	--0°	19.2°	13.6°

Fig. 19 shows rubbing, pretilt and chevron directions. Fig. 19 (a) shows a C1 uniform orientation. Fig. 19 (b) shows a C1 twist orientation. Fig. 19 (c) shows a C2 orientation. The state of each panel can be specified as the C2 orientation based on the relationship between the disclination and the rubbing direction.

The terms "C1 uniform orientation", "C1 twist orientation" and "C2 orientation" are explained in, for example, Japanese Journal of Applied Physics, Vol 31 (1992) pp 852-857.

Referring to the relationship between a voltage and a memory pulse width shown in Fig. 18, each panel has a voltage to which a minimum memory pulse width is related. The voltage is represented by Vmin for each panel.

$$(V0 + V1) > Vmin \qquad (4)$$

When (V0 + V1) is determined, a voltage V0/2 gives a FLC molecule a force which is equal to that acting on the FLC molecule when the voltage (V0 + V1) is applied.

$$V0/2 < Vmin \qquad (5)$$

The following voltage waveforms give the change of a quantity of transmitted light which is equal to that made on pixels when a voltage waveform in which a voltage -V0/2 shown in Fig. 20 (1) is followed by voltages V0/2 and 0 is applied to the pixels in the memory state of "dark" or "bright": voltage waveforms shown in Figs. 20 (2) to (4); a voltage waveform in which a voltage -(V0 + V1) is followed by voltages (V0 + V1) and 0; a voltage waveform in which the voltage 0 is followed by the voltages -(V0 + V1) and (V0 + VI).

The following voltage waveforms give the change of a quantity of transmitted light which is equal to that made on pixels when a voltage waveform in which a voltage V0/2 shown in Fig. 20 (5) is followed by voltages -V0/2 and 0 is applied to the pixels in the memory state of "dark" or "bright": voltage waveforms shown in Figs. 20 (6) to (8); a voltage waveform in which a voltage (V0 + V1) is followed by voltages -(V0 + V1) and 0; a voltage waveform in which the voltage 0 is followed by the voltages (V0 + V1) and -(V0 + V1).

There will be described a method for determining a driving waveform used for a FLC panel into which a liquid crystal having the above-mentioned characteristics and a negative dielectric anisotropy is injected.

At the time of non-selection, a voltage to be applied to a pixel is determined so as not to cause crosstalk. In case Fig. 20 (1) shows a voltage waveform to be applied to a pixel A22 formed by a scanning electrode having a non-selection voltage applied thereto and a signal electrode having a holding voltage applied thereto, the following voltage waveforms give the change of a quantity of transmitted light which is almost equal to that of the pixel made when the voltage waveform shown in Fig. 20 (1) is applied to the FLC molecule forming the pixel: voltage waveforms shown in Figs. 20 (2) to (4); a voltage waveform in which a voltage - (V0 + V1) is followed by voltages (V0 + V1) and 0; a voltage waveform in which the voltage 0 is followed by the voltages -(V0 + V1) and (V0 + V1). It is assumed that Fig. 20 (2) shows a voltage waveform to be applied to a pixel A21 formed by the scanning electrode having a non-selection voltage applied thereto and the signal electrode having a rewriting voltage applied thereto.

Then, a voltage waveform to be applied to a pixel A12 formed by the scanning electrode having a selection voltage applied thereto and the signal electrode having a holding voltage applied thereto is selected from voltage waveforms shown in Figs. 20 (1) to (4), the voltage waveform in which the voltage -(V0 + V1) is followed by the voltages (V0 + V1) and 0, and the voltage waveform in which the voltage 0 is followed by the voltages -(V0 + V1) and (V0 + V1). In this case, there is the following relationship between voltages V22, V21 and V12 to be applied to the pixels A22, A21 and A12 and a voltage V11 to be applied to a pixel A11 formed by the scanning electrode having a selection voltage applied thereto and the signal electrode having a rewriting voltage applied thereto.

$$V22 - V21 = V12 - V11 \tag{6}$$

$$V11 = V12 - (V22 - V21) \tag{6'}$$

When a voltage waveform to be applied to the pixel A12 is determined in such a manner that a voltage to be applied to the pixel A11 is 0 or positive, the voltage waveform shown in Fig. 20 (3) is selected.

The above-mentioned calculation is performed with reference to the combinations of voltage waveforms shown in Fig. 21 (a). Fig. 21 (a) (5) shows a voltage waveform to be applied to the pixel A11.

Similarly, there can be obtained the combinations of voltage waveforms shown in Figs. 21 (b) to (d) and Figs. 22 (a) to (d). The combinations of voltage waveforms shown in Figs. 23 (a) to (d) and Figs. 24 (a) to (d) which are slightly different from those of voltage waveforms shown in Figs. 21 (a) to (d) can also be used if the change of a quantity of transmitted light of the pixel A12 having a voltage waveform (4) applied thereto is almost equal to that of the pixel A22 having a voltage waveform (1) having applied thereto or the pixel A21 having a voltage waveform (2) applied thereto.

Based on the combinations of voltage waveforms shown in Fig. 21 (c), it is possible to determine the combinations of voltage waveforms to be applied to the scanning electrodes, signal electrodes and pixels which are shown in Fig. 9 (A). Based on the combinations of voltage waveforms shown in Fig. 21 (a), it is possible to determine the combinations of voltage waveforms to be applied to the scanning electrodes, signal electrodes and pixels which are shown in Fig. 9 (B).

A voltage waveform shown in Fig. 21 (c) or (a) (1) is assigned for a voltage waveform to be applied to a pixel formed by the scanning electrode having a non-selection voltage applied thereto and the signal electrode having a holding voltage applied thereto which is shown in Fig. 9 (A) or (B) (8). A voltage waveform shown in Fig. 21 (c) or (a) (2) is assigned for a voltage waveform to be applied to a pixel formed by the scanning electrode having a non-selection voltage applied thereto and the signal electrode having a rewriting voltage applied thereto which is shown in Fig. 9 (A) or (B) (7). A voltage waveform shown in Fig. 21 (c) or (a) (4) is assigned for a voltage waveform to be applied to a pixel formed by the scanning electrode having a selection voltage applied thereto and the signal electrode having a holding voltage applied thereto which is shown in Fig. 9 (A) or (B) (6). A voltage waveform shown in Fig. 21 (c) or (a) (5) is assigned for a voltage waveform to be applied to a pixel formed by the scanning electrode having a selection voltage applied thereto and the signal electrode having a rewriting voltage applied thereto which is shown in Fig. 9 (A) or (B) (5).

In case the voltage waveform to be applied to the pixel is determined, the change of a quantity of transmitted light of the pixel made by applying the voltage waveform shown in Fig. 9 (A) or (B) (6) to the FLC molecule forming the pixel is almost equal to that made by applying the voltage waveform shown in Fig. 9 (A) (7) or (8) or Fig. 9 (B) (7) or (8) to the FLC molecule forming the pixel.

In case a voltage ($V0 + \alpha$) ($\alpha > 0$) is used in place of a voltage V0 in Figs. 9 (A) and (B), the change of a quantity of transmitted light of the pixel made by applying the voltage waveform shown in Fig. 9 (A) (6) or Fig. 9 (B) (6) to the FLC molecule forming the pixel is smaller than that made by applying the voltage waveform shown in Fig. 9 (A) (7) or (8) or Fig. 9 (B) (7) or (8) to the FLC molecule forming the pixel.

If a voltage waveform shown in Fig. 9 (A) (1) or Fig. 9 (B) (1) is applied to the scanning electrode, a rewriting voltage waveform shown in Fig. 9 (A) (3) or Fig. 9 (B) (3) is applied to the signal electrode, a holding voltage waveform shown in Fig. 9 (A) (4) or Fig. 9 (B) (4) is applied to the signal electrode and a non-selection voltage waveform shown in Fig. 9 (A) (2) or Fig. 9 (B) (2) is applied to the scanning electrode. For example, when voltages shown in Figs. 9 (A) (1) to (7) are V1 to V7 respectively, the following formulas can be obtained.

$$V3 = V1 - V5 \qquad (7)$$

$$V4 = V1 - V6 \qquad (8)$$

$$V2 = V3 + V7 \qquad (9)$$

Referring to the combinations of voltage waveforms shown in Fig. 9, the area ratio of a voltage having a unipolarity shown in Fig. 9 (A) (5) or Fig. 9 (B) (5) to that shown in Fig. 9 (A) (7) or (8), or Fig. 9 (B) (7) or (8), that is, a bias ratio B is found by the following formula.

$$B = (V0/2) \div (V1 + V0/2) \qquad (10)$$

There cannot be expected a very high contrast. The time axes of the combinations of voltage waveforms shown in Fig. 9 (A) are changed from t0 to t1, and the combinations of voltage waveforms shown in Fig. 9 (A) are added to those of voltage waveforms which are obtained by shifting the combinations of voltage waveforms shown in Fig. 9 (A) by a time 2t1 so that the combinations of voltage waveforms shown in Fig. 11 (A) are obtained. The time axes of the combinations of voltage waveforms shown in Fig. 9 (B) are changed from t0 to t1, and the combinations of voltage waveforms shown in Fig. 9 (B) are added to those of voltage waveforms which are obtained by shifting those of voltage waveforms shown in Fig. 9 (B) by a time 2t1 so that the combinations of voltage waveforms shown in Fig. 11 (B) are obtained. The bias ratio B of Fig. 11 is found by the following formula.

$$B = (V0/2) \div (2V1 + V0) \qquad (11)$$

Consequently, there can be expected a very high contrast.

According to the above-mentioned driving method, the contrast depends on how many times the combinations of voltage waveforms shown in Fig. 9 are shifted and superposed. The combinations of voltage waveforms shown in Fig. 9 can be superposed many times for the following reason. Since the voltage waveform shown in Fig. 9 (A) or (B) (6) is preliminarily designed in such a manner that a torque which is equal to those of the voltage waveforms shown in Figs. 9 (A) or (B) (7) and (8) is given to the FLC molecule, the memory state of the FLC molecule is not changed in similar to the time of biasing. This fact is made clearer by using a voltage $(V0 + \alpha) / 2$ ($\alpha > 0$) in place of a voltage V0/2 in Fig. 9.

In a panel using PSI-X7355 for an orientation film, there is partially seen a C1 twist orientation. In a panel using PSI-XS012 or PSI-XS014 for the orientation film, there is partially seen a C2 twist orientation. In the C1 and C2 twist orientations, there is obtained a voltage and memory pulse width characteristic having a voltage to which a minimum memory pulse width is related in similar to Fig. 18. Consequently, there is a voltage V0/2 which gives the FLC molecule a force equal to that generated by applying a voltage (V0 + V1) in similar to the C2 uniform orientation.

In a FLC panel 1 using the orientation film PSI-X7355 manufactured by Chisso Co., Ltd., a voltage (V0 + V1) is set to 50 v, a voltage V0 is variable to compare characteristics obtained by applying voltages shown in Figs. 11 (A) (7) and (8) to the pixel and measuring an optical response as an electric signal by means of a photodiode with characteristics obtained by applying a voltage shown in Fig. 11 (A) (6) to the pixel and measuring an optical response as an electric signal by means of the photodiode. Consequently, there are obtained following voltages by which the quantities of transmitted light are almost equal to each other.

V0/2 = 10 v
V1 = 30 v

Although driving waveforms shown in Fig. 13 according to the prior art can also be superposed, crosstalk remains. Accordingly, this superposition is not very preferable.

V0/2 is set to 12 v and V1 is set to 26 v. The voltages shown in Fig. 11 (A) (6) and Fig. 11 (A) (7) or (8) are sequentially applied. Then, Fig. 11 (B) (6) and Fig. 11 (B) (7) or (8) are sequentially applied. Although this operation is repeated in a cycle of 10 Hz, a flicker is not sensed. It is a matter of course that the state of a pixel can be changed into another state by applying a voltage shown in Fig. 11 (A) (5) in place of the voltage shown in Fig. 11 (A) (6), and that the state of a pixel can be changed into a further state by applying a voltage shown in Fig. 11 (B) (5) in place of the voltage shown in Fig. 11 (B) (6).

In order to reduce the voltage (V0 + V1) from 50 v. liquid crystal compositions A and B are injected into panels using the orientation films PSI-X012, PSI-X014 and PSI-X7355 manufactured by Chisso Co., Ltd. The liquid crystal compositions A and B are prepared by diluting a ferroelectric liquid crystal SCE-8 with compounds A and B having a negative dielectric anisotropy.

	Liquid Crystal	Compound	Blending Ratio
Liquid Crystal Composition A	SCE-8	Compound A	8 : 2
Liquid Crystal Composition B	SCE-8	Compound B	9 : 1

Figs. 25 and 26 show the relationship between a voltage and a memory pulse width measured by voltage waveforms shown in Fig. 14 (A). When Figs. 25 and 26 are compared with Fig. 18, it is apparent that a voltage Vmin having a minimum memory pulse width is reduced. It is found that the voltage (V0 + V1) can be reduced by decreasing the ratio of chiral in a liquid crystal.

The structures of a FLC panel 1 and a FLCD 4 used in the present embodiment which are shown in Figs. 2 and 3 are the same as those of the prior art, so that their description will be omitted.

Fig. 1 is a block diagram schematically showing the structure of a display system using the FLCD 4. Referring to the display system, information necessary for image display is obtained from a digital signal which is outputted from a personal computer 2 to a CRT display 3. and a display controller 13 converts the digital signal into a signal for causing the FLCD 4 to perform image display. Based on a conversion signal thus obtained, image display is performed by the FLCD 4.

Fig. 4 is a waveform diagram for each signal outputted from the personal computer 2 to the CRT display 3. Fig. 4 (1) shows a horizontal synchronizing signal HD which gives a cycle for a horizontal scanning partition of image information outputted to the CRT display 3. Fig. 4 (2) shows a vertical synchronizing signal VD which gives a cycle for a screen of the image information. Fig. 4 (3) collectively shows the image information as display data Data for each horizontal scanning partition, in which numerals are attached to distinguish the data Data for each horizontal period. Fig. 4 (4) is an enlarged waveform diagram showing the horizontal scanning partition of the horizontal synchronizing signal HD. Fig. 4 (5) is an enlarged waveform diagram showing the horizontal scanning partition of the display data Data, in which numerals are attached to distinguish the data Data for each pixel. Fig. 4 (6) is a waveform diagram showing a data transfer clock CLK of the display data Data.

Although the digital signal has data for only 9 x 8 pixels, data for 16 x 16 pixels of the FLC panel 1 can be displayed for the following reason. The 16 x 16 pixels of the FLC panel 1 are virtually divided into display portions 0 to 3. The display portion 0 has scanning electrodes L0 to L7 and signal electrodes S0 to S7. The display portion 1 has the scanning electrodes L0 to L7 and signal electrodes S8 to SF. The display portion 2 has scanning electrodes L8 to LF and the signal electrodes S0 to S7. The display portion 3 has the scanning electrodes L8 to LF and the signal electrodes S8 to SF. As shown in Figs. 5 and 6, data in the 0th horizontal scanning partition of the digital signal for 9 x 8 pixels to be inputted indicates the correspondence of data in first to eighth horizontal scanning partitions to the display portions 0 to 3.

Referring to Figs. 5 and 6, if third and seventh data in the 0th horizontal scanning partition are "bright" (data having no slash) and "bright" (to which Fig. 5 is suited) respectively, data in the first to eighth horizontal scanning partitions correspond to the display portion 0. If the third and seventh data in the 0th horizontal scanning partition are "bright" and "dark" (data having slash) respectively, the data in the first to eighth horizontal scanning partitions correspond to the display portion 1. If the third and seventh data in the 0th horizontal scanning partition are "dark" and "bright" (to which Fig. 6 is suited) respectively, the data in the first to eighth horizontal scanning partitions correspond to the display portion 2. If the third and seventh data in the 0th horizontal scanning partition are "dark", the data in the first to eighth horizontal scanning partitions correspond to the display portion 3.

Fig. 8 is a block diagram showing the schematic structure of the display controller 13. The display controller 13 includes an interface circuit 14, a display memory circuit 15, a group memory circuit 16, an identity and difference memory circuit 17, an input control circuit 18, an output control circuit 19, an address circuit 20 and a driving control circuit 21. The interface circuit 14 receives a digital signal from the personal computer 2 and distributes the same to necessary circuits. The display memory circuit 15 records display data DA to be displayed next on the FLC panel 1. The group memory circuit 16 collectively records the change of data of the display memory circuit 15 every two scanning electrodes (if at least one pixel is changed, there is change). The identity and difference memory circuit 17 collectively records the change of data of the display memory circuit 15 every four pixels (if at least one pixel is changed, there is change). The input control circuit 18 controls a timing at which the digital signal outputted from the personal computer 2 is written into the memory circuits 15, 16 and 17. The output control circuit 19 and address circuit 20 control timings at which data to be outputted from the memory circuits 15, 16 and 17 to the FLCD 4 are read out. The driving control circuit 21 controls the operations of a scanning side drive circuit 11 and a signal side drive circuit 12 forming the FLCD 4 on receipt of data from the memory circuits 15, 16 and 17, the output control circuit 19 and the address circuit 20.

The memory circuits 15 and 17 repeat four continuous cycles in which the data of addresses specified by input side addresses IACx and IASx are first read out from the memory, the data of addresses specified by output side addresses OACx and OASx are secondly read out from the memory, the data of addresses specified by the input side addresses IACx and IASx are thirdly written into the memory, and the data of addresses specified by the output side addresses OACx and OASx are fourthly read out from the memory. The group memory circuit 16 brings the data of the address specified by the output side address OAGx into the state of no change in a second cycle.

By using the display controller 13, 16 scanning electrodes L of the FLCD 4 shown in Fig. 3 are virtually divided into 8 groups two by two, the group memory circuit 16 records whether the display of pixels on 2 scanning electrodes for each group needs to be changed, the identity and difference memory circuit 17 collectively records, every 4 pixels, which pixel on the 2 scanning electrodes needs to be changed in the display state, and the display memory circuit 15 records, for each pixel, the display state into which the pixel is brought.

When the display of the FLCD 4 is "A B C D" shown in Fig. 3 and 9 x 8 matrix data Data shown in Fig. 5 is inputted from the personal computer 2 to the display controller 13, the data of groups 0 to 3 indicate that display is changed and the data of groups 4 to 7 indicate that display is not changed in the group memory circuit 16 of the display controller 13. The group 0 corresponds to the scanning electrodes L0 and L1. The group 1 corresponds to the scanning electrodes L2 and L3. The group 2 corresponds to the scanning electrodes L4 and L5. The group 3 corresponds to the scanning electrodes L6 and L7.

A selection voltage shown in Fig. 11 (A) (1) is applied to the scanning electrodes L0 and L1 belonging to the group 0 in order. When the data of the identity and difference memory circuit 17 corresponding to an pixel Aij on the scanning electrode Li to which the selection voltage is applied is changed and the data of the display memory circuit 15 is in the display state of "dark", a rewriting voltage shown in Fig. 11 (A) (3) is applied to the signal electrode Sj forming the pixel Aij so as to change the display state of the pixel Aij into "dark". A holding voltage shown in Fig. 11 (A) (4) is applied to a signal electrode Sh forming a pixel Aih ($j \neq h$) on the scanning electrode Li.

Then, a selection voltage shown in Fig. 11 (B) (1) is applied to the scanning electrodes L0 and L1 belonging to the group 0 in order. When the data of the identity and difference memory circuit 17 corresponding to the pixel Aij on the scanning electrode Li to which the selection voltage is applied is changed and the data of the display memory circuit 15 is in the display state of "bright", a rewriting voltage shown in Fig. 11 (B) (3) is applied to the signal electrode Sj forming the pixel Aij so as to change the display state of the pixel Aij into "bright". A holding voltage shown in Fig. 11 (B) (4) is applied to the signal electrode Sh forming the pixel Aih ($j \neq h$) on the scanning electrode Li.

Thereafter, the display of the FLCD 4 shown in Fig. 3 is changed from "A B C D" to "E B C D" in the same manner as in the groups 1 to 3.

The display state of a pixel is decided as "dark" or "bright" by causing the polarizing axis of the polarizing plate 10a shown in Fig. 2 to correspond to the direction of a major axis in the stable state 104 or 105 of the FLC molecule shown in Fig. 7 (A). If the polarizing axis corresponds to the direction of a major axis, one of the stable states 104 and 105 is "dark" and the other is "bright". The pixel formed by the FLC molecule in the stable state of "dark" is in the display state of "dark". The pixel formed by the FLC molecule in the stable state of "bright" is in the display state of "bright".

Not only the combinations of voltage waveforms shown in Fig. 9 but also those of voltage waveforms shown in Fig. 10 can be applied to a dynamic driving method for rewriting pixels on all scanning electrodes. Each voltage waveform shown in Fig. 10 is different from each voltage waveform shown in Fig. 9 in that the quantities of transmitted light are not equal to each other when voltage waveforms shown in Fig. 10 (6) and Fig. 10 (7) or (8) are applied to the pixel. In other respects, the voltage waveforms of Fig. 10 are the same as those of Fig. 9. Therefore, further description will be omitted.

The combinations of voltage waveforms shown in Fig. 10 can be applied to a static driving method in similar to the combinations of voltage waveforms shown in Fig. 11. In this case, the voltage waveform shown in Fig. 10 (A) (6) indicates that a voltage V1 is applied for a time t0/2 and a voltage (-V1 - V0) is then applied for a time t0. Consequently, a force acting on the FLC molecule by virtue of the voltage V1 should be about twice as great as a force acting on the FLC molecule by virtue of the voltage (V1 + V0).

The voltage waveform shown in Fig. 11 (A) (5) or Fig. 11 (B) (5) includes only a voltage having a unipolarity. For this reason, it is relatively difficult to sense a flicker attendant on rewriting even though there are performed driving operations in which the scanning electrodes L0 and L1 belonging to the group 0 are driven based on the combinations of voltage waveforms shown in Fig. 11 (A), pixels on the scanning electrodes are rewritten based on the combinations of voltage waveforms shown in Fig. 11 (A) or (B) by 4:1 jump scan, the scanning electrodes L0 and L1 belonging to the group 0 are driven based on the combinations of voltage waveforms shown in Fig. 11 (B), and pixels on the scanning electrodes are rewritten based on the combinations of voltage waveforms shown in Fig. 11 (B) or (A) by the 4:1 jump scan.

Fig. 12 is a waveform diagram in which the scanning electrode LD is rewritten by the voltage waveforms shown in Fig. 11 (A), the group 6 is driven by the voltage waveforms shown in Fig. 11 (A), the scanning electrode L2 is rewritten by the voltage waveforms shown in Fig. 11 (B), the group 0 is driven by the voltage waveforms shown in Fig. 11 (B), the scanning electrode L2 is rewritten by the voltage waveforms shown in Fig. 11 (A), the group 0 is driven by the voltage waveforms shown in Fig. 11 (A), the scanning electrode L6 is rewritten by the voltage waveforms shown in Fig. 11 (B), and the group 1 is driven by the voltage waveforms shown in Fig. 11 (B). Figs. 12 (1) to (8) show voltages to be applied to the scanning electrode L2, the scanning electrode L3, the signal electrode S1, the signal electrode S2, the pixel A21, the pixel A22, the pixel A31 and the pixel A 32, respectively.

As seen from the voltages to be applied to the pixels A21 and A22 shown in Figs. 12 (5) and (6), the quantities of transmitted light of the pixels A21 and A22 are the largest when the combinations of applied voltage waveforms are changed from Fig. 11 (A) to Fig. 11 (B) or from Fig. 11 (B) to Fig. 11 (A), and the voltage waveform of Fig. 11 (A) (5) or Fig. 11 (B) (5) is applied to the pixels A21 and A22.

The voltage waveform shown in Fig. 11 (A) (5) or Fig. 11 (B) (5) is a unipolar pulse. Consequently, the FLC molecule is only moved from the stable state 105 or 104 shown in Fig. 7 (A) to the axis 107 or 106 by a critical tilt angle $\pm \theta$. If the tilt angle θ is almost equal to a memory angle ω , the change of a quantity of transmitted light made on pixels is not greatly different from that obtained by exchanging the combinations of applied voltage waveforms of Fig. 11 (A) for those of Fig. 11 (B), or reversely. Consequently, there can be realized driving in which a flicker is not strongly marked.

According to the present invention, it is possible to increase an apparent response speed and enhance a contrast.

Claims

1. A method of driving a liquid crystal panel, the liquid crystal panel comprising a ferroelectric liquid crystal (9) disposed between a plurality of scanning electrodes (L) and a plurality of signal electrodes (S), the scanning electrodes (L) being perpendicular to the signal electrodes (S), a pixel being defined where a scanning electrodes crosses a signal electrode, the liquid crystal having two stable states and a negative dielectric anisotropy and being able to be switched from one stable state to the other stable state by a voltage pulse having its minimum pulse width at a specific pulse voltage Vmin, the method comprising the step of applying a selection voltage to the scanning electrode corresponding to a pixel to be re-written and applying a re-writing voltage to the signal electrode corresponding to the pixel to be re-written while applying a non-selection voltage to other scanning electrodes and applying a holding voltage to other signal electrodes;

wherein the holding voltage, the selection voltage, the re-writing voltage and the non-selection voltage are chosen such that when a selection voltage and a holding voltage, or a non-selection and a rewriting voltage, or a non-selection and a holding voltage are applied concurrently to any pixel, the resultant voltage waveform across the pixel in each case comprises a sequence of pulses; wherein in each case

a) the sequence of pulses has the same number and order of alternating pulses of opposite polarities;
b) the first and final pulses in each sequence of pulses have opposite polarities;
c) no individual pulse can switch the liquid crystal; and
d) the resultant waveform when the selection voltage and the holding voltage are applied concurrently to any said pixel is such that the magnitude of a pulse of the 1st polarity is within the range where the effect of the negative dielectric anisotropy acting on the ferroelectric liquid crystal molecules is increased and the magnitude of a pulse of the opposite polarity is within the range where the effect of the negative dielectric anisotropy acting on the ferro-electric liquid crystal molecules is decreased.

2. A method for driving a liquid crystal panel according to claim 1 further comprising the steps of;

virtually dividing the scanning electrodes into a plurality of groups;

analysing display data supplied to the liquid crystal panel to determine whether or not the pixels on scanning electrodes belonging to each of the groups need te be re-written;
sequentially applying the selection voltage to scanning electrodes belonging to a group containing a pixel to be re-written;
applying the non-selection voltage to the other scanning electrodes; and
applying the rewriting voltage to the pixel to be rewritten via the signal electrode.

3. A method for driving a liquid crystal panel according to claim 1 wherein the liquid crystal panel comprises an orientation film having a pretilt angle of 2.3° to 7.5°.

Patentansprüche

1. Verfahren zum Ansteuern einer Flüssigkristalltafel mit einem ferroelektrischen Flüssigkristall (9), der zwischen mehreren Abtastelektroden (L) und mehreren Signalelektroden (S) vorgesehen ist, wobei die Abtastelektroden (L) senkrecht zu den Signalelektroden (5) verlaufen, ein Pixel definiert ist, wo eine Abtastelektrode eine Signalelektrode kreuzt, der Flüssigkristall zwei stabile Zustände und eine negative dielektrische Anisotropie hat und in der Lage ist, von einem stabilen Zustand in den anderen stabilen Zustand durch einen Spannungsimpuls geschaltet zu werden, der eine Mindestimpulsbreite bei einer spezifischen Impulsspannung Vmin hat, wobei das Verfahren den Schritt des Anlegens einer Auswahlspannung an die Abtastelektrode entsprechend einem umzuschreibenden Pixel und des Anlegens einer Umschreibspannung an die Signalelektrode entsprechend einem umzuschreibenden Pixel aufweist, während eine Nicht-Auswahlspannung an anderen Abtastelektroden anliegt und eine Haltespannung andere Signalelektroden beaufschlagt,

   wobei die Haltespannung, die Auswahlspannung, die Umschreibspannung und die Nicht-Auswahlspannung derart gewählt sind, daß, wenn eine Auswahlspannung und eine Haltespannung oder eine Nicht-Auswahl- und eine Umschreibspannung oder eine Nicht-Auswahl- und eine Haltespannung gleichzeitig an irgendeinem Pixel anliegen, die sich ergebende Spannungswellenform über dem Pixel in jedem Fall eine Sequenz von Impulsen aufweist, wobei in jedem Fall

   a) die Sequenz der Impulse die gleiche Zahl und Reihenfolge von sich ändernden Impulsen von entgegengesetzten Polaritäten hat,

   b) der erste und der letzte Impuls in jeder Sequenz von Impulsen entgegengesetzte Polaritäten haben,

   c) kein einzelner Impuls den Flüssigkristall schalten kann, und

   d) die sich ergebende Wellenform, wenn die Auswahlspannung und die Haltespannung an dem beliebigen Pixel anliegen, derart ist, daß die Größe eines Impulses der ersten Polarität innerhalb des Bereiches liegt, in welchem die Auswirkung der negativen dielektrischen Anisotropie, die auf die ferroelektrischen Flüssigkristallmoleküle einwirkt, zunimmt, und die Größe eines Impulses der entgegengesetzten Polarität innerhalb des Bereiches liegt, in welchem die Auswirkung der negativen dielektrischen Anisotropie, die auf die ferroelektrischen Flüssigkristallmoleküle einwirkt, abnimmt.

2. Verfahren zum Ansteuern einer Flüssigkristalltafel nach Anspruch 1, weiterhin umfassend die folgenden Schritte:

   virtuelles Teilen der Abtastelektroden in eine Vielzahl von Gruppen,

   Analysieren der zu der Flüssigkristalltafel gespeisten Anzeigedaten, um zu bestimmen, ob die Pixels auf Abtastelektroden, die zu jeder der Gruppen gehören, umgeschrieben werden müssen oder nicht,

   sequentielles Anlegen der Auswahlspannung an Abtastelektroden, die zu einer Gruppe gehören, die ein umzuschreibendes Pixel enthält,

   Anlegen der Nicht-Auswahlspannung an die anderen Abtastelektroden, und

   Anlegen der Umschreibspannung an das umzuschreibende Pixel über die Signalelektrode.

3. Verfahren zum Ansteuern einer Flüssigkristalltafel nach Anspruch 1, bei dem die Flüssigkristalltafel einen Orien-

tierungsfilm mit einem Vorneigungswinkel von 2,3° bis 7,5° umfaßt.

Revendications

1. Méthode pour commander un panneau d'affichage à cristaux liquides, le panneau d'affichage à cristaux liquides comprenant un cristal liquide ferroélectrique (9) disposé entre plusieurs électrodes de balayage (L) et plusieurs électrodes de signaux (S), étant précisé que les électrodes de balayage (L) sont perpendiculaires aux électrodes de signaux (S), qu'un élément d'image est défini là où une électrode de balayage croise une électrode de signal, que le cristal liquide a deux états stables et une anisotropie diélectrique négative et qu'il est apte à passer d'un état stable à un autre état stable grâce à une impulsion de tension dont la largeur d'impulsion minimale est située à une tension d'impulsion spécifique Vmin, laquelle méthode consiste à appliquer une tension de sélection à l'électrode de balayage correspondant à un élément d'image à réécrire, et à appliquer une tension de réécriture à l'électrode de signal correspondant à l'élément d'image à réécrire tandis qu'une tension de non-sélection est appliquée à d'autres électrodes de balayage et qu'une tension de maintien est appliquée à d'autres électrodes de signaux ;

   selon laquelle la tension de maintien, la tension de sélection, la tension de réécriture et la tension de non-sélection sont choisies pour que lorsqu'une tension de sélection et une tension de maintien, ou une tension de non-sélection et une tension de réécriture, ou une tension de non-sélection et une tension de maintien sont appliquées simultanément à un élément d'image quelconque, la forme de la tension qui en résulte à travers l'élément d'image comprenne dans chaque cas une suite d'impulsions ; et selon laquelle, dans chaque cas,

   a) la suite d'impulsions a le même nombre et le même ordre d'impulsions alternatives de polarités opposées ;
   b) la première et la dernière impulsion de chaque suite d'impulsions ont des polarités opposées ;
   c) aucune impulsion individuelle ne peut commuter le cristal liquide ; et
   d) la forme d'onde résultante lorsque la tension de sélection et la tension de maintien sont appliquées simultanément à un élément d'image quelconque est telle que l'amplitude d'une impulsion de la première polarité est située à l'intérieur de la plage dans laquelle l'effet de l'anisotropie diélectrique négative qui agit sur les molécules de cristal liquide ferroélectrique est accru, et l'amplitude d'une impulsion de la polarité opposée est située à l'intérieur de la plage dans laquelle l'effet de l'anisotropie diélectrique négative agissant sur les molécules de cristal liquide ferroélectrique est réduit.

2. Méthode pour commander un panneau d'affichage à cristaux liquides selon la revendication 1, consistant aussi à :

   diviser virtuellement les électrodes de balayage en plusieurs groupes ;
   analyser les données d'affichage fournies au panneau à cristaux liquides pour déterminer si les éléments d'image sur les électrodes de balayage appartenant à chacun des groupes ont besoin ou pas d'être réécrits ;
   appliquer de façon séquentielle la tension de sélection aux électrodes de balayage appartenant à un groupe qui contient un élément d'image à réécrire ;
   appliquer la tension de non-sélection aux autres électrodes de balayage ; et
   appliquer la tension de réécriture à l'élément d'image à réécrire par l'intermédiaire de l'électrode de signal.

3. Méthode pour commander un panneau à cristaux liquides selon la revendication 1, selon laquelle le panneau à cristaux liquides comprend un film d'orientation qui présente un angle de pré-inclinaison de 2,3° à 7,5°.

FIG. 1

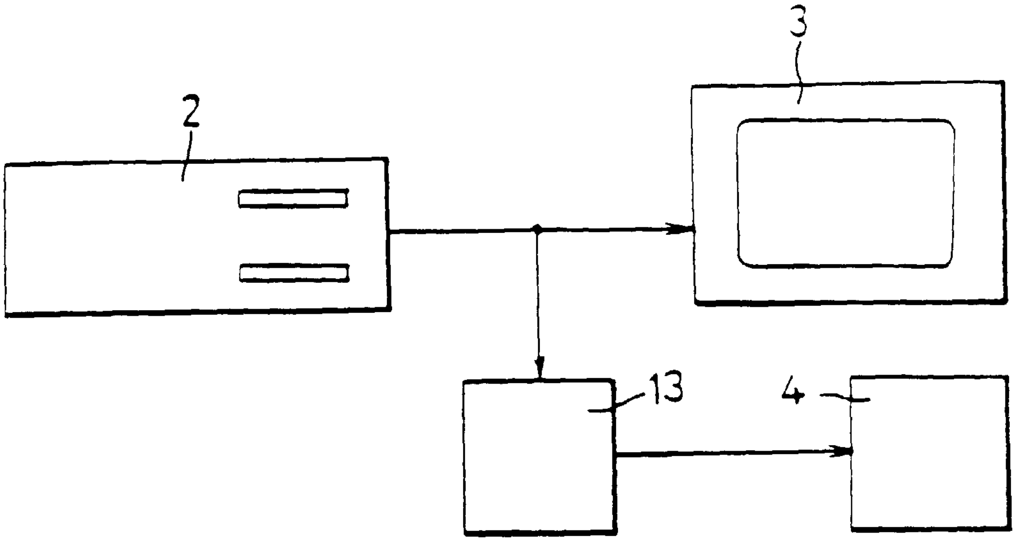


FIG. 2

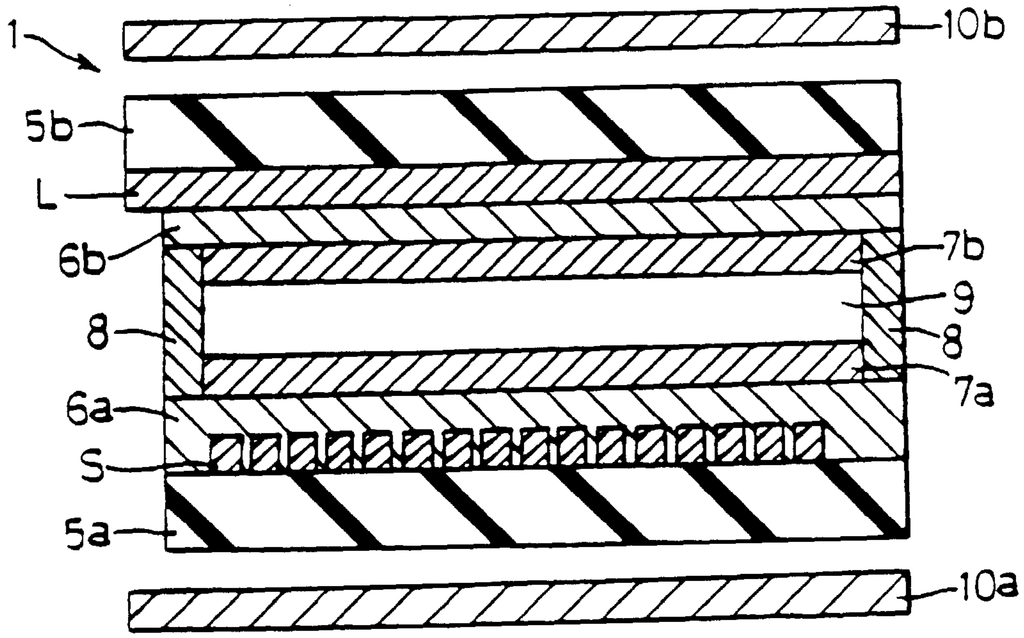


FIG. 3

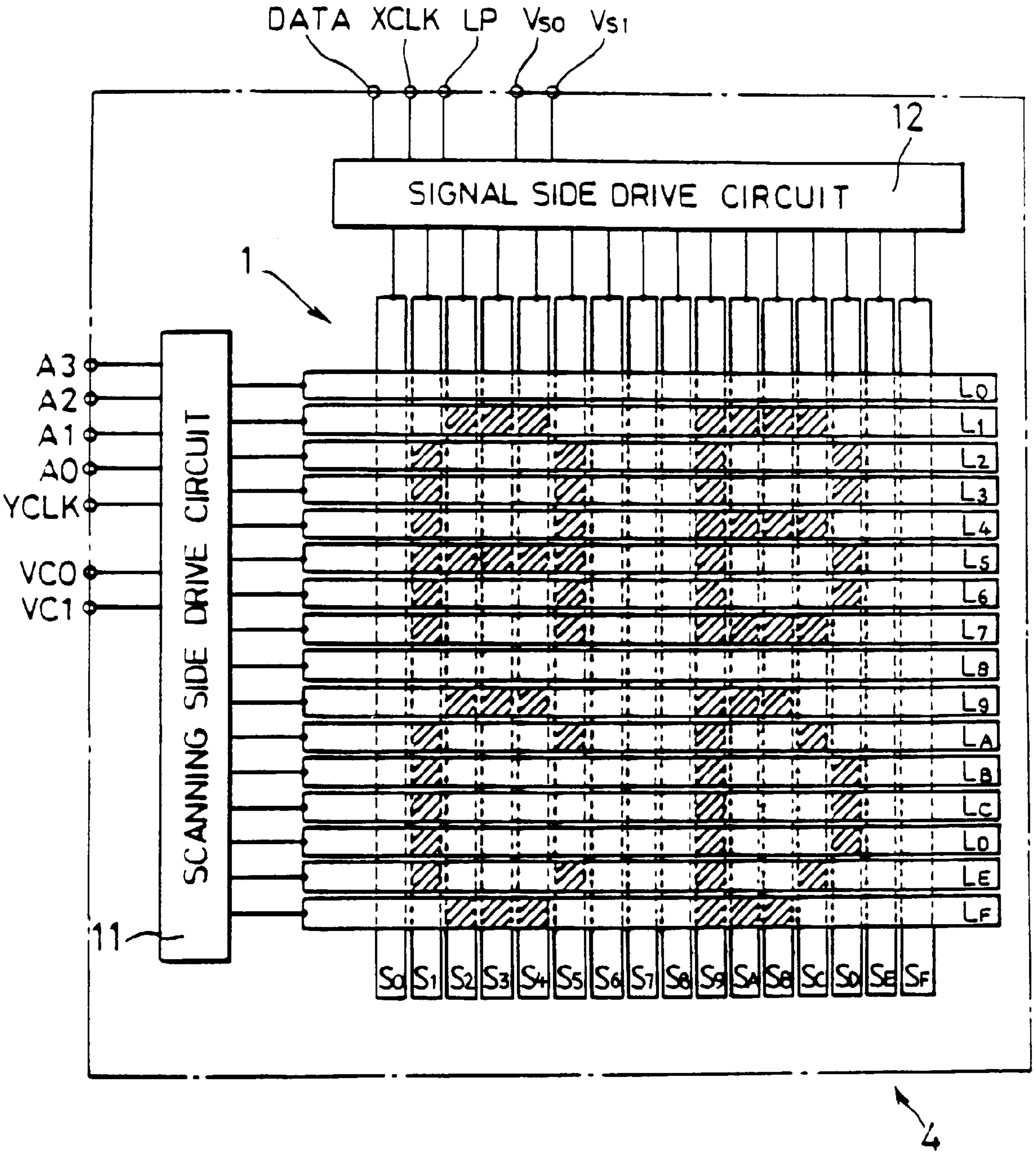

DATA
XCLK
LP
V_{S0}
V_{S1}
12
SIGNAL SIDE DRIVE CIRCUIT
1
A3
A2
A1
A0
YCLK
VC0
VC1
SCANNING SIDE DRIVE CIRCUIT
11
L_0
L_1
L_2
L_3
L_4
L_5
L_6
L_7
L_8
L_9
L_A
L_B
L_C
L_D
L_E
L_F
S_0
S_1
S_2
S_3
S_4
S_5
S_6
S_7
S_8
S_9
S_A
S_B
S_C
S_D
S_E
S_F
4

FIG. 4

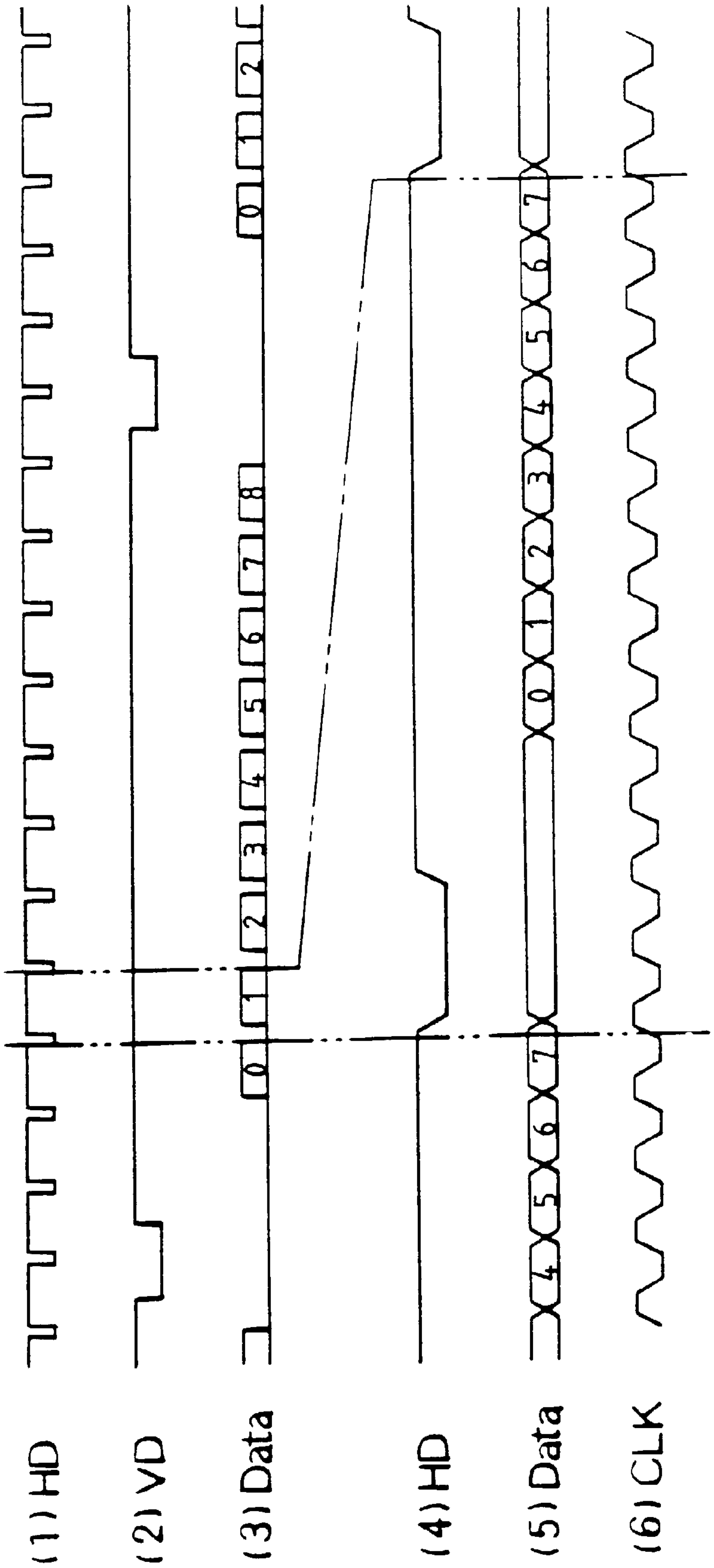


FIG. 5

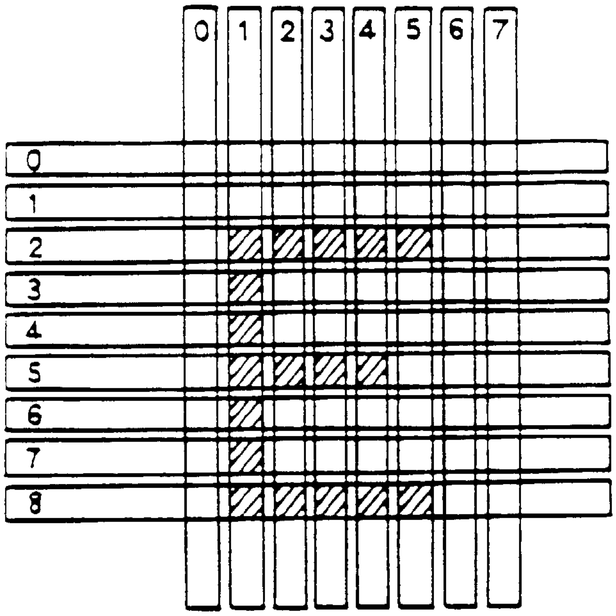


FIG. 6

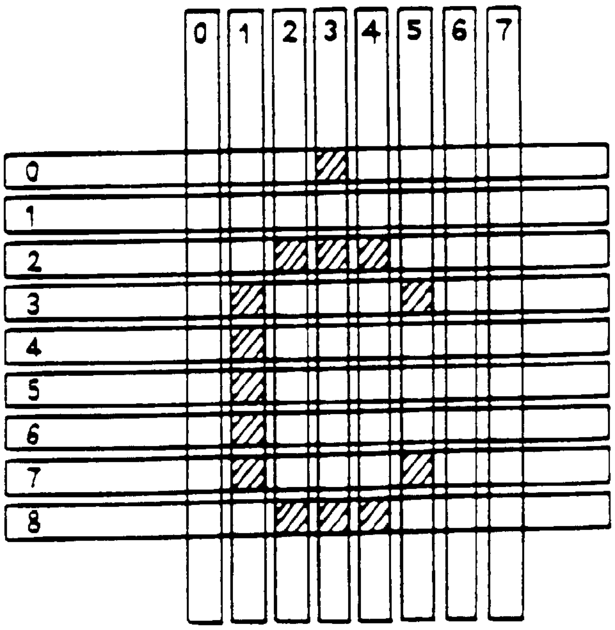
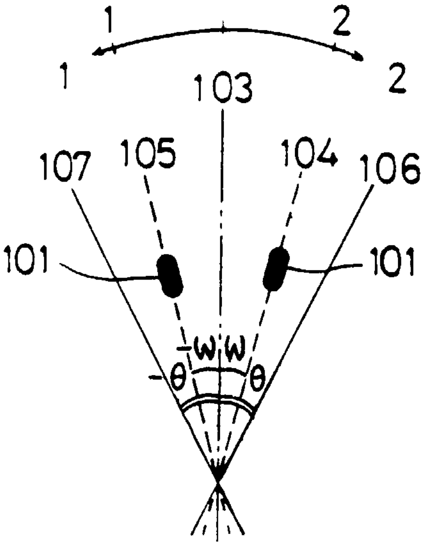


FIG.7

(A)



(B)

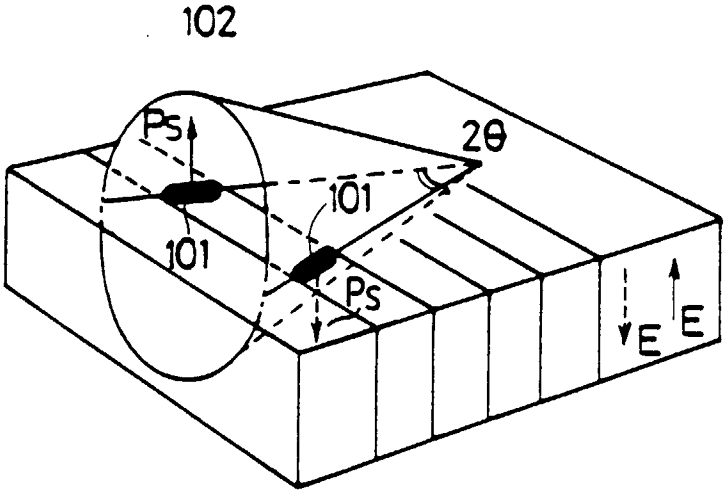


FIG.8

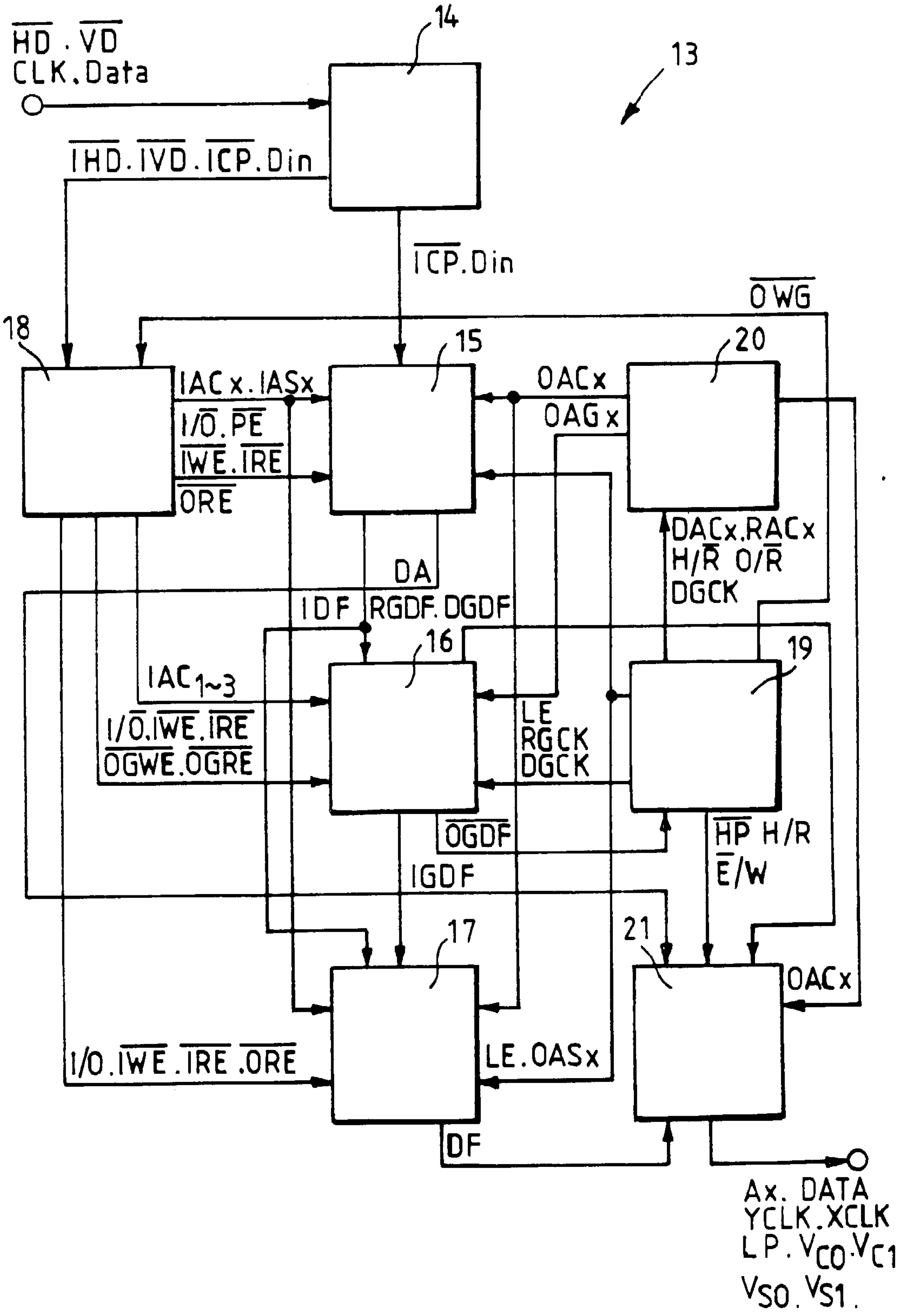

HD · VD
CLK.Data
14
13
IHD.IVD.ICP.Din
ICP.Din
OWG
18
15
20
IACx.IASx
I/O.PE
IWE.IRE
ORE
OACx
OAGx
DACx.RACx
H/R O/R
DGCK
DA
IDF
RGDF.DGDF
16
19
IAC1~3
I/O.IWE.IRE
OGWE.OGRE
LE
RGCK
DGCK
OGDF
HP H/R
E/W
IGDF
17
21
OACx
I/O.IWE.IRE.ORE
LE.OASx
DF
Ax. DATA
YCLK.XCLK
LP.VC0.VC1
VS0.VS1.

FIG. 9

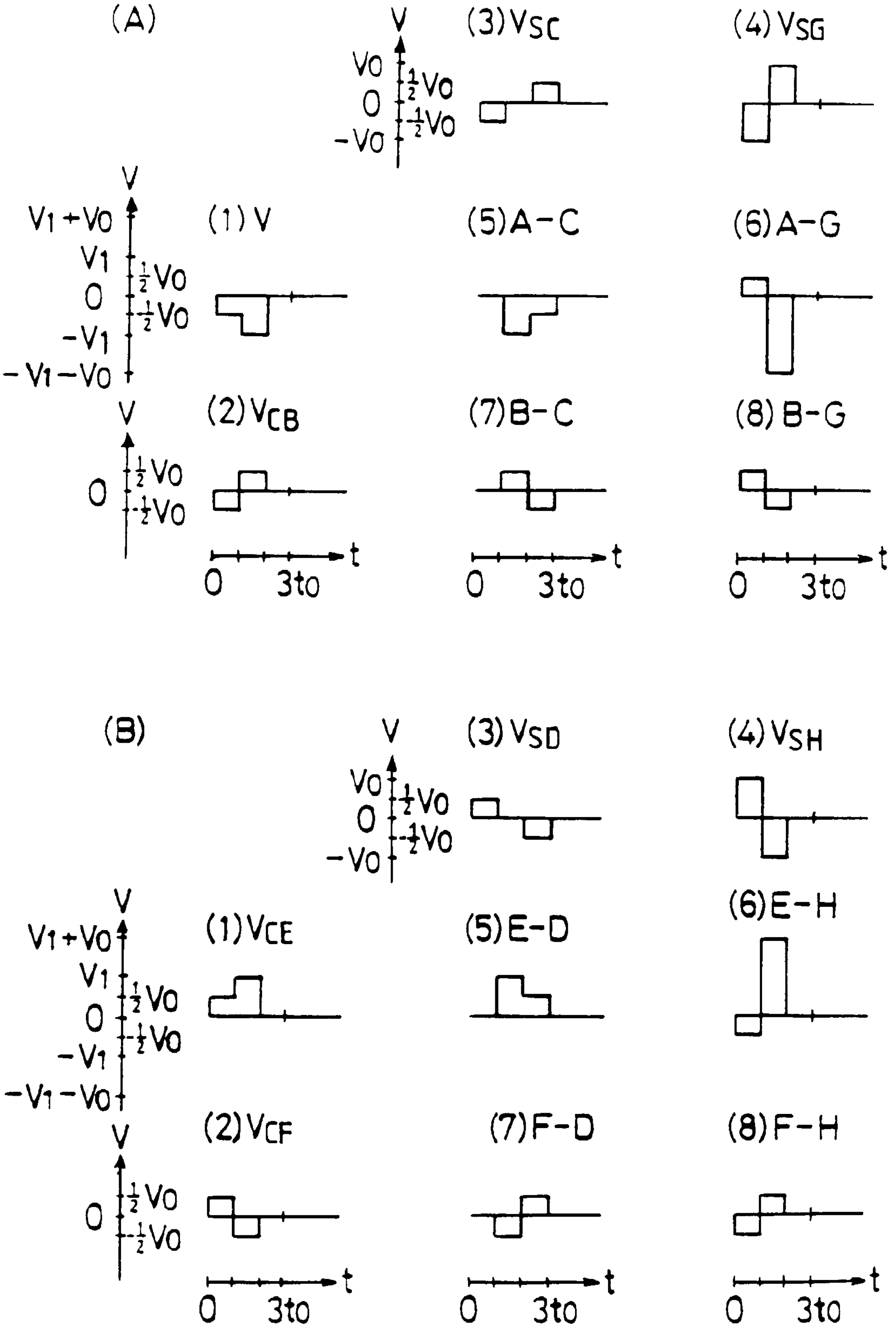

(A)
V
(3) VSC
(4) VSG
V0
$\frac{1}{2}$V0
0
$-\frac{1}{2}$V0
-V0
V
V1+V0
(1) V
(5) A-C
(6) A-G
V1
$\frac{1}{2}$V0
0
$-\frac{1}{2}$V0
-V1
-V1-V0
V
(2) VCB
(7) B-C
(8) B-G
0
$\frac{1}{2}$V0
$-\frac{1}{2}$V0
t
0
3to
(B)
V
(3) VSD
(4) VSH
V0
$\frac{1}{2}$V0
0
$-\frac{1}{2}$V0
-V0
V
V1+V0
(1) VCE
(5) E-D
(6) E-H
V1
$\frac{1}{2}$V0
0
$-\frac{1}{2}$V0
-V1
-V1-V0
V
(2) VCF
(7) F-D
(8) F-H
0
$\frac{1}{2}$V0
$-\frac{1}{2}$V0
t
0
3to

FIG.10

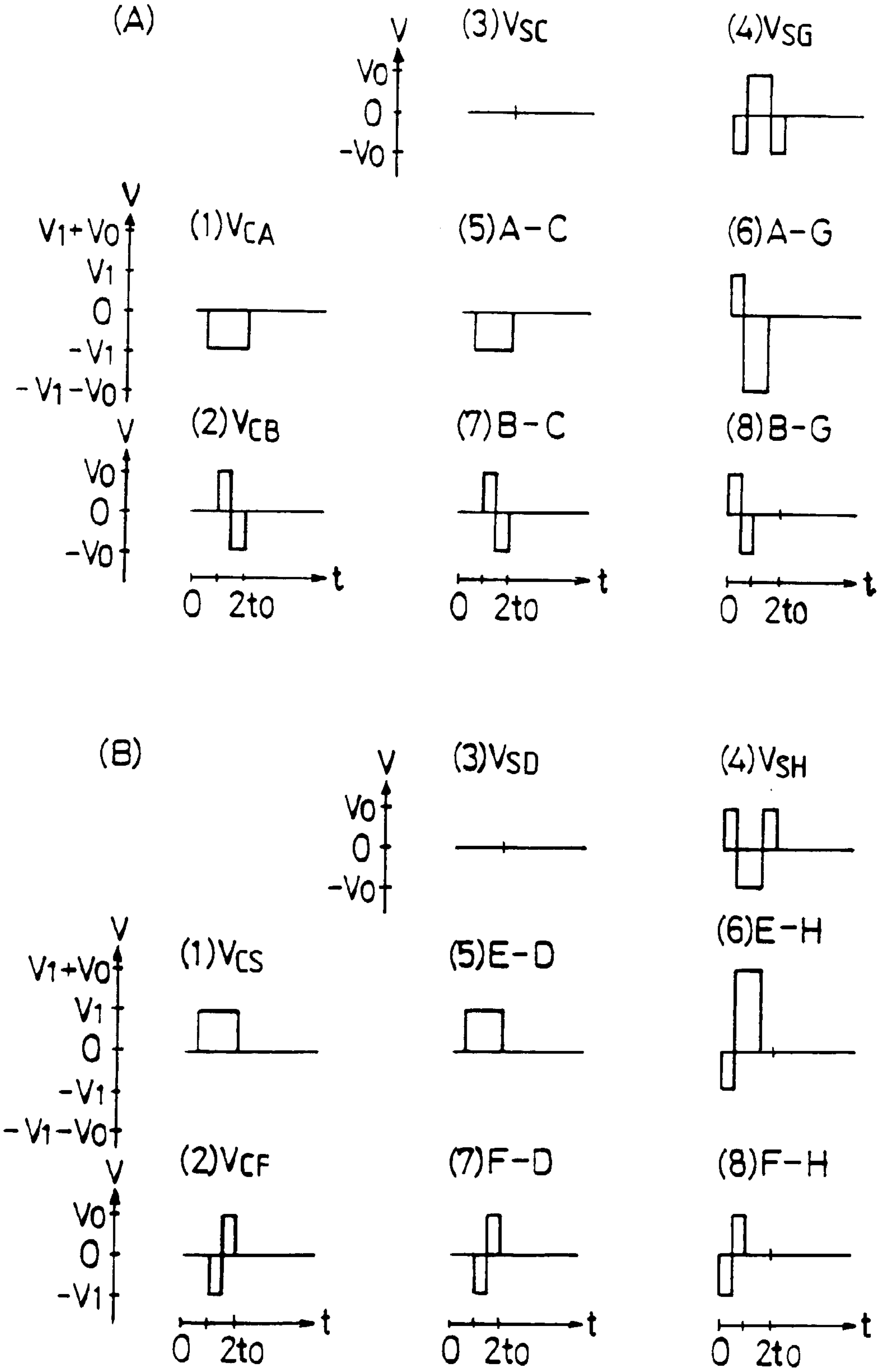

(A)
(1)VCA
(2)VCB
(3)VSC
(4)VSG
(5)A-C
(6)A-G
(7)B-C
(8)B-G
V
V1+V0
V1
0
-V1
-V1-V0
V0
-V0
0
2to
t
(B)
(1)VCS
(2)VCF
(3)VSD
(4)VSH
(5)E-D
(6)E-H
(7)F-D
(8)F-H
-V1

FIG.11

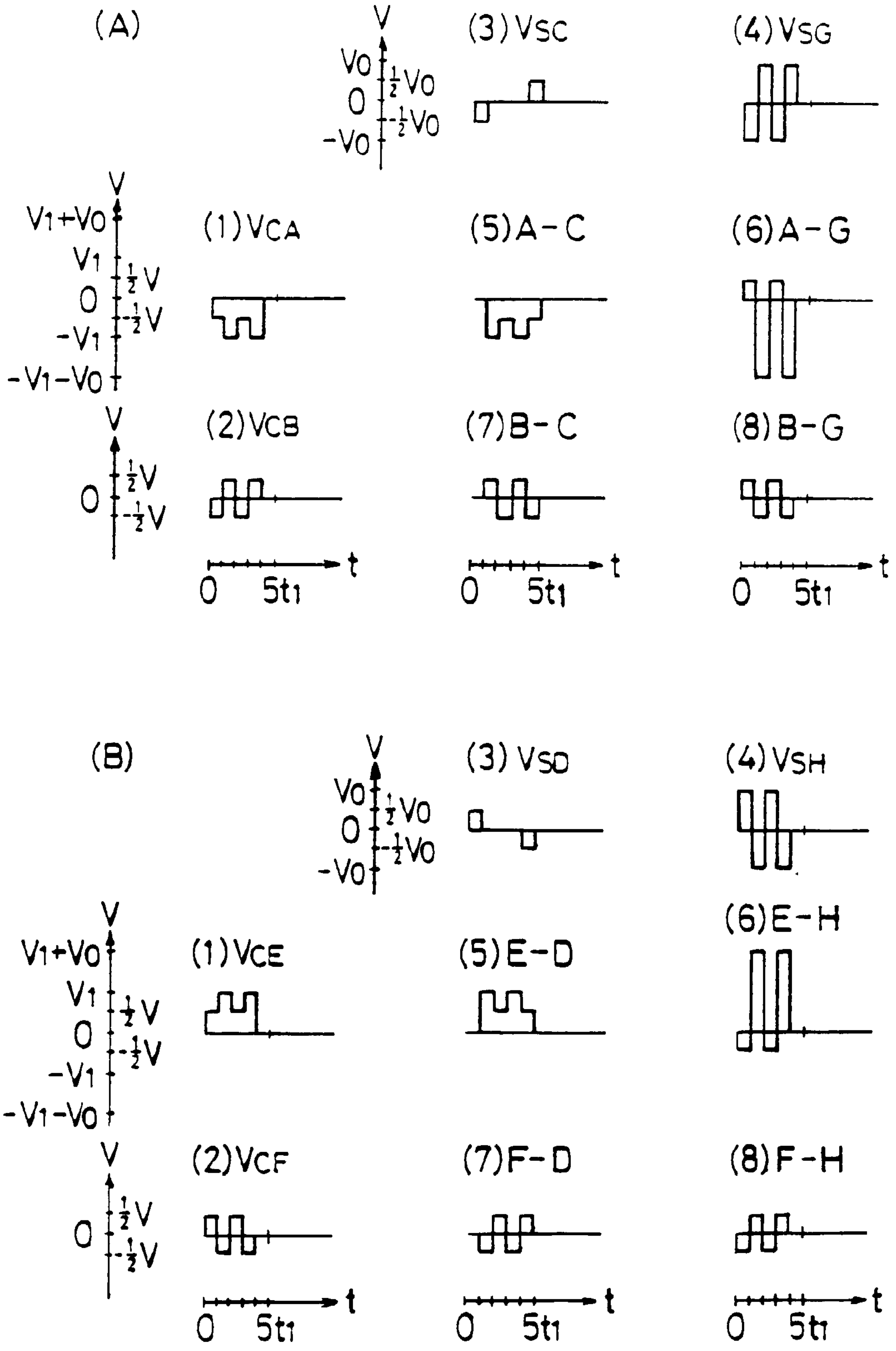

(A)
V
V0
$\frac{1}{2}$V0
0
$-\frac{1}{2}$V0
-V0
(3) VSC
(4) VSG
V
V1+V0
V1
$\frac{1}{2}$V
0
$-\frac{1}{2}$V
-V1
-V1-V0
(1) VCA
(5) A-C
(6) A-G
V
0
$\frac{1}{2}$V
$-\frac{1}{2}$V
(2) VCB
(7) B-C
(8) B-G
t
0
5t1
t
0
5t1
t
0
5t1
(B)
V
V0
$\frac{1}{2}$V0
0
$-\frac{1}{2}$V0
-V0
(3) VSD
(4) VSH
V
V1+V0
V1
$\frac{1}{2}$V
0
$-\frac{1}{2}$V
-V1
-V1-V0
(1) VCE
(5) E-D
(6) E-H
V
0
$\frac{1}{2}$V
$-\frac{1}{2}$V
(2) VCF
(7) F-D
(8) F-H
t
0
5t1
t
0
5t1
t
0
5t1

FIG. 12

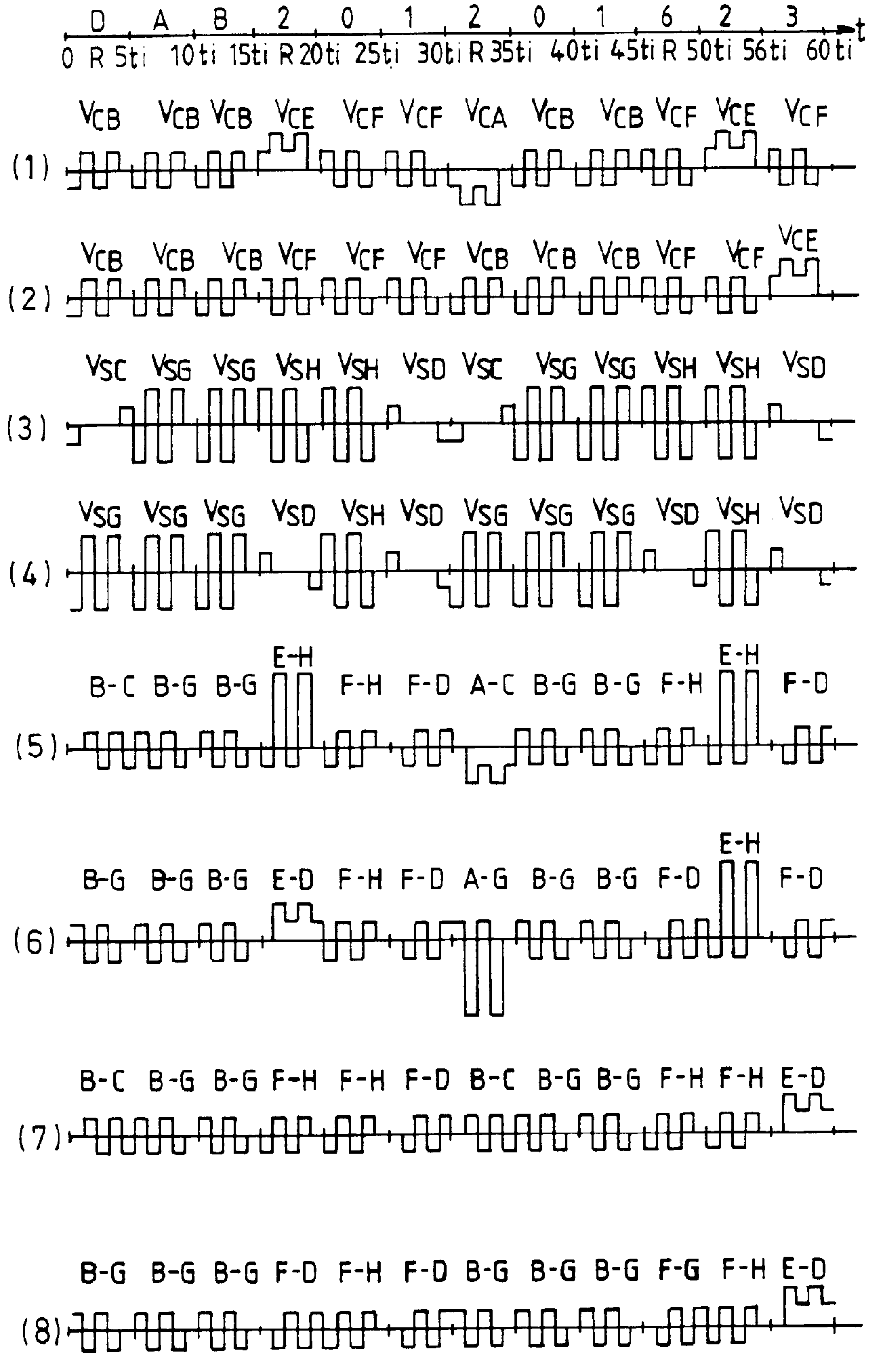

D A B 2 0 1 2 0 1 6 2 3
t
0 R 5ti 10ti 15ti R 20ti 25ti 30ti R 35ti 40ti 45ti R 50ti 56ti 60ti
(1)
VCB VCB VCB VCE VCF VCF VCA VCB VCB VCF VCE VCF
(2)
VCB VCB VCB VCF VCF VCF VCB VCB VCB VCF VCF VCE
(3)
VSC VSG VSG VSH VSH VSD VSC VSG VSG VSH VSH VSD
(4)
VSG VSG VSG VSD VSH VSD VSG VSG VSG VSD VSH VSD
(5)
B-C B-G B-G E-H F-H F-D A-C B-G B-G F-H E-H F-D
(6)
B-G B-G B-G E-D F-H F-D A-G B-G B-G F-D E-H F-D
(7)
B-C B-G B-G F-H F-H F-D B-C B-G B-G F-H F-H E-D
(8)
B-G B-G B-G F-D F-H F-D B-G B-G B-G F-G F-H E-D

FIG.13

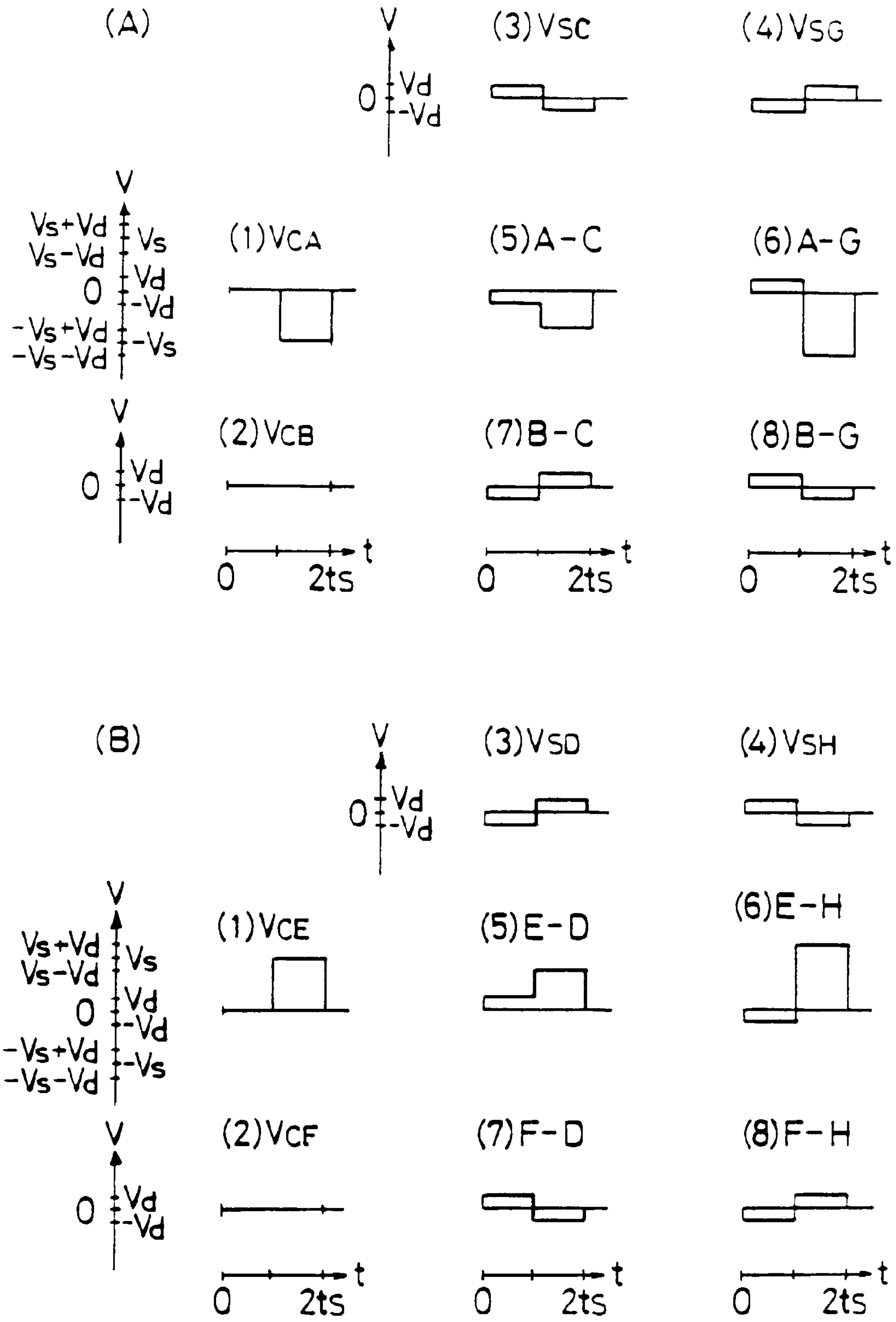

(A)
V
0
Vd
-Vd
(3) VSC
(4) VSG
V
Vs+Vd
Vs-Vd
0
-Vs+Vd
-Vs-Vd
Vs
Vd
-Vd
-Vs
(1) VCA
(5) A-C
(6) A-G
V
0
Vd
-Vd
(2) VCB
(7) B-C
(8) B-G
0
2ts
t
(B)
(3) VSD
(4) VSH
(1) VCE
(5) E-D
(6) E-H
(2) VCF
(7) F-D
(8) F-H

FIG 14

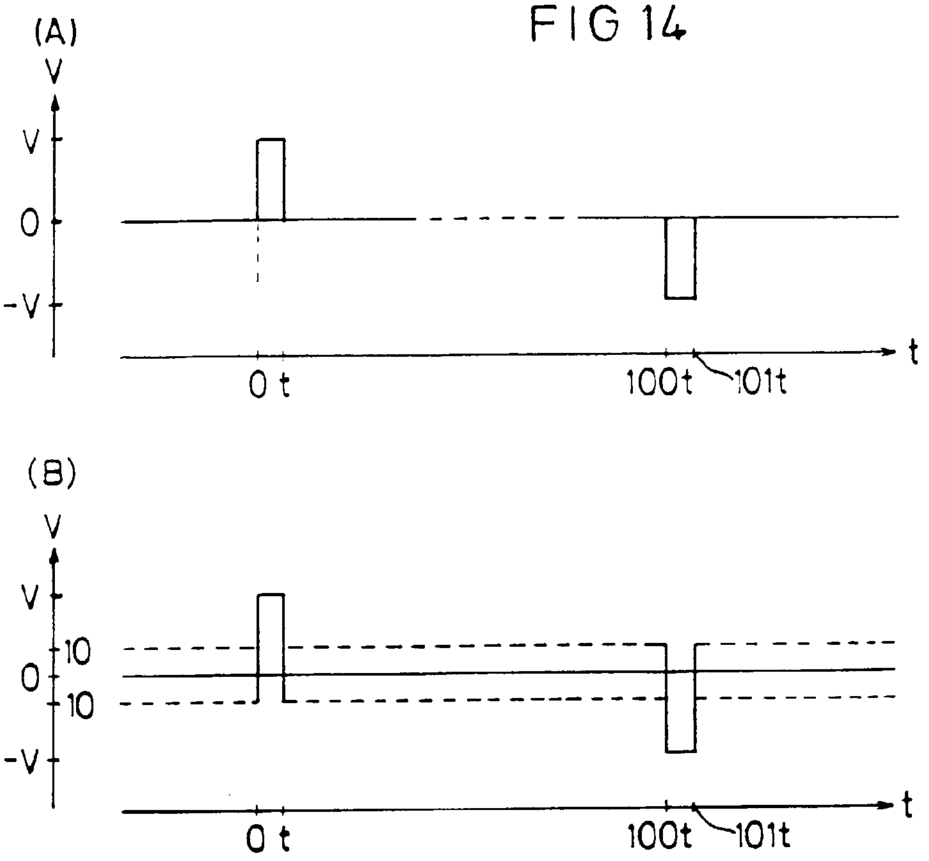

(A)
V
V
0
-V
t
0 t
100t
101t
(B)
V
V
10
0
10
-V
t
0 t
100t
101t

FIG.15

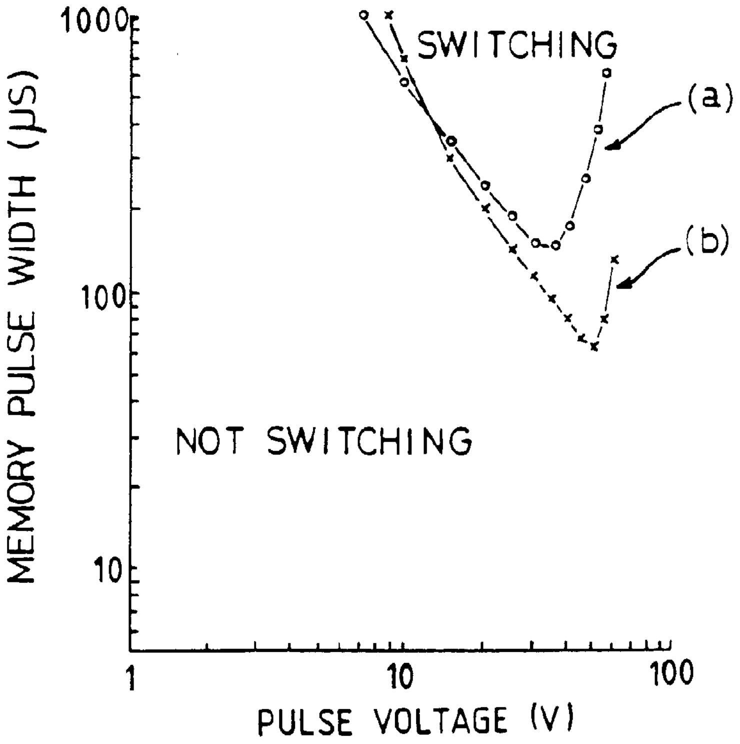

MEMORY PULSE WIDTH (μS)
1000
100
10
1
10
100
PULSE VOLTAGE (V)
SWITCHING
NOT SWITCHING
(a)
(b)

FIG. 16

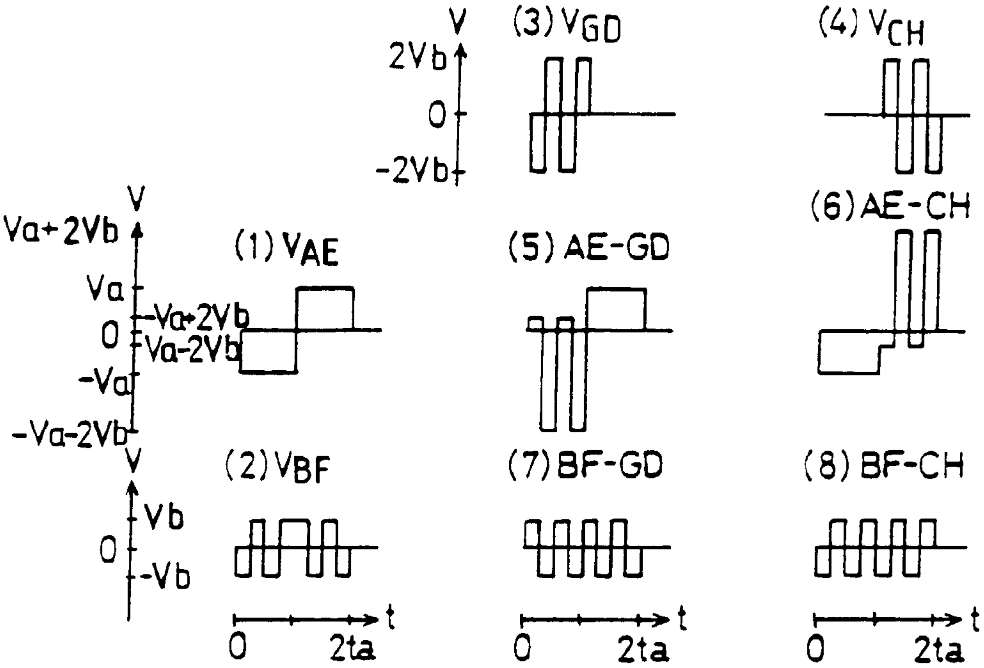

V
2Vb
0
-2Vb
(3) VGD
(4) VCH
V
Va+2Vb
Va
-Va+2Vb
0
Va-2Vb
-Va
-Va-2Vb
(1) VAE
(5) AE-GD
(6) AE-CH
V
Vb
0
-Vb
(2) VBF
(7) BF-GD
(8) BF-CH
t
0
2ta
t
0
2ta
t
0
2ta

FIG. 17

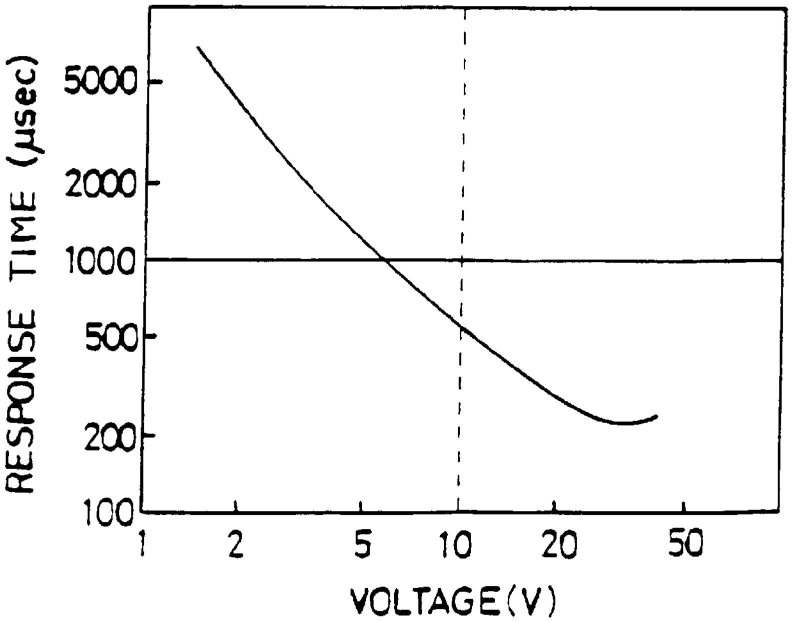

RESPONSE TIME (μsec)
5000
2000
1000
500
200
100
1
2
5
10
20
50
VOLTAGE(V)

FIG. 18

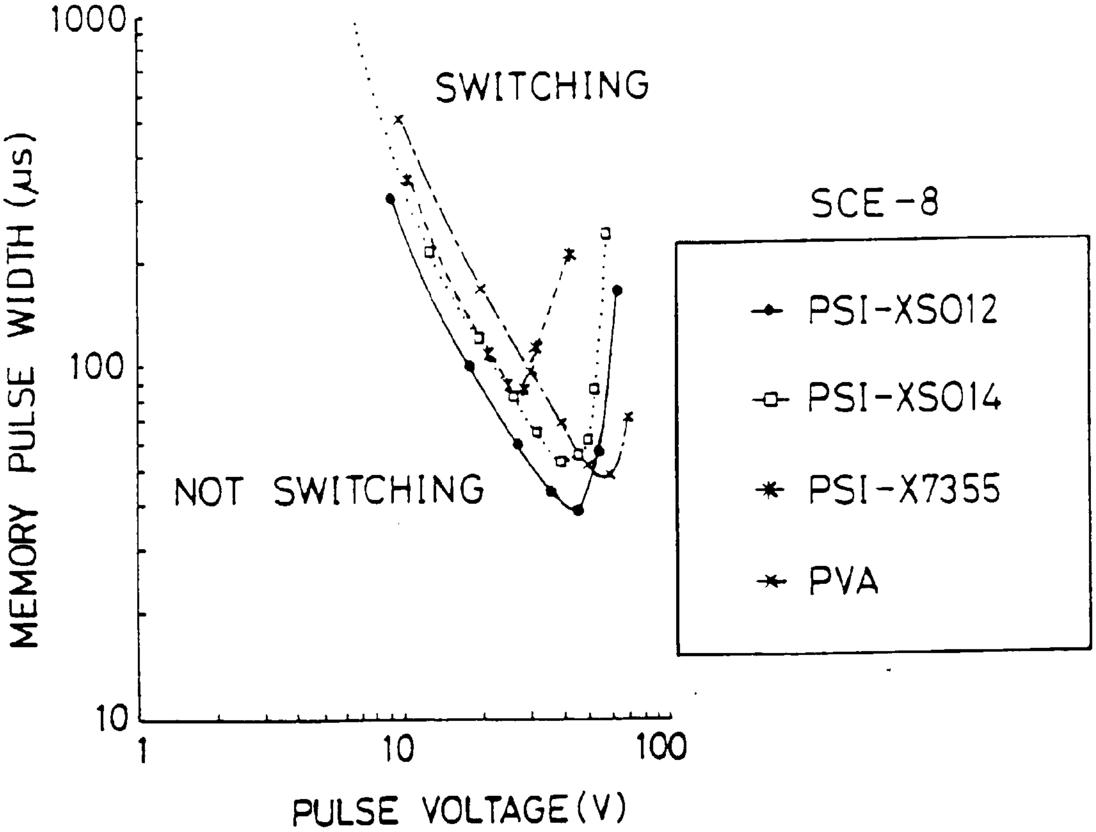
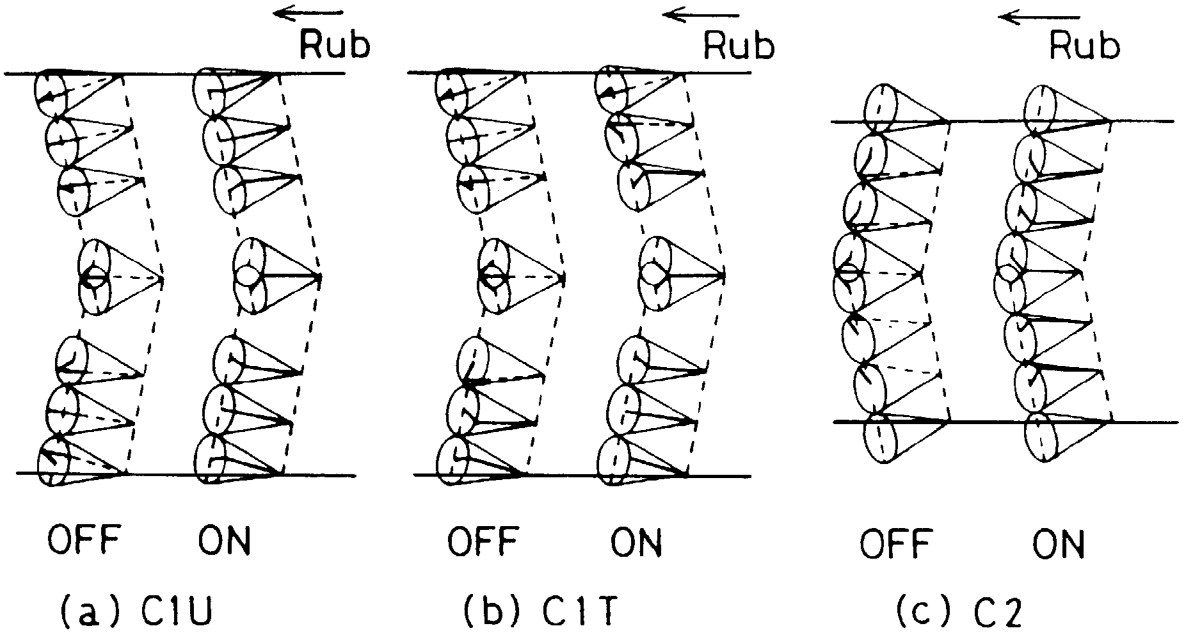

1000
100
10
1
10
100
MEMORY PULSE WIDTH (μs)
PULSE VOLTAGE (V)
SWITCHING
NOT SWITCHING
SCE-8
PSI-XS012
PSI-XS014
PSI-X7355
PVA

FIG. 19



(a) C1U (b) C1T (c) C2

FIG. 20

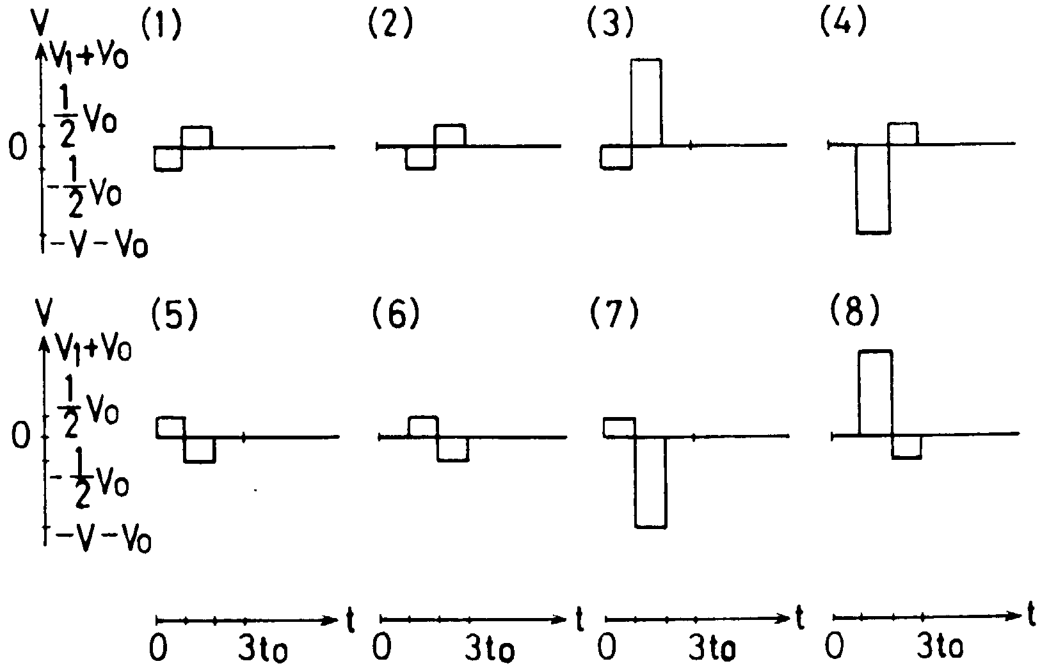


FIG. 21

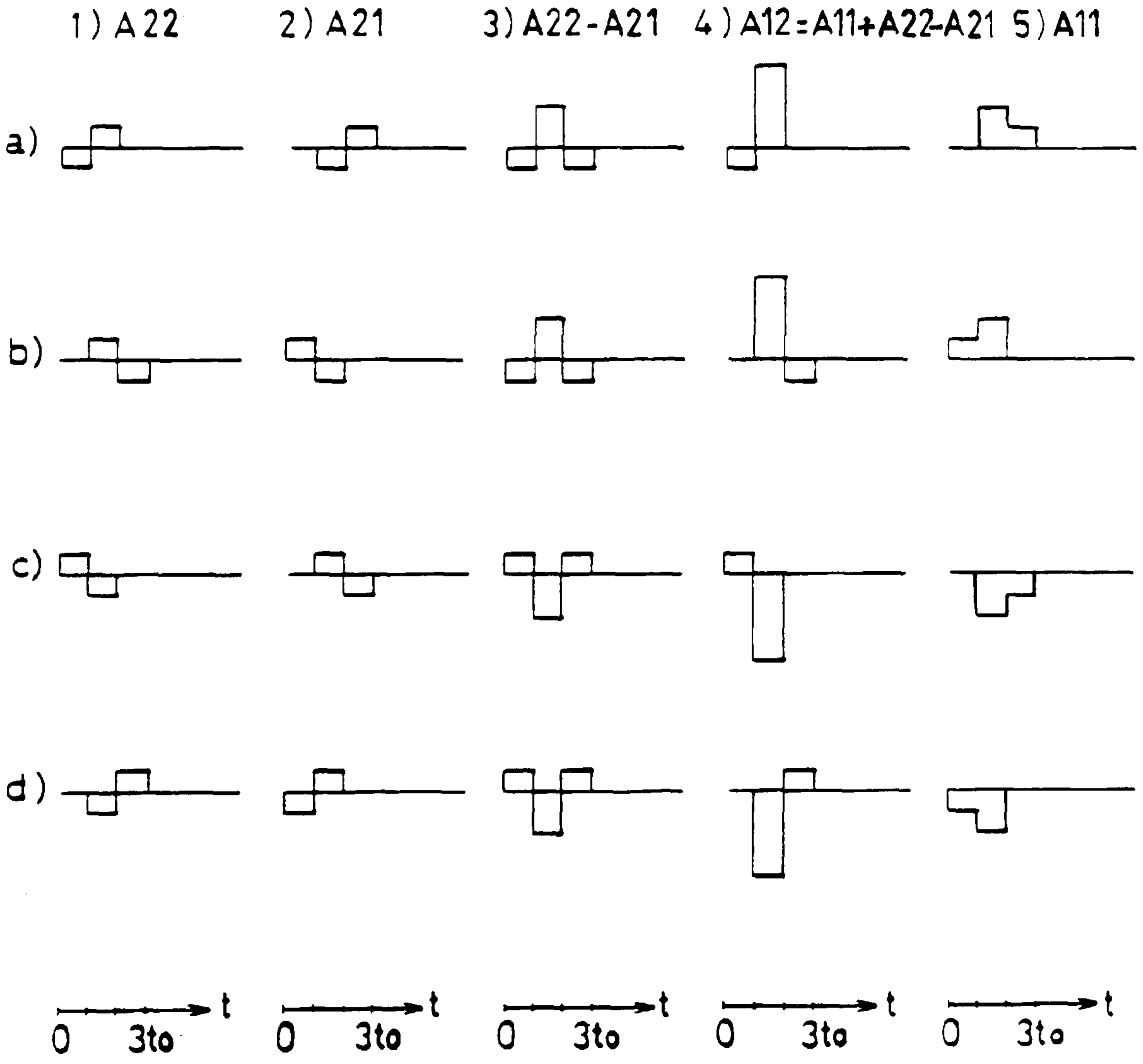


FIG. 22

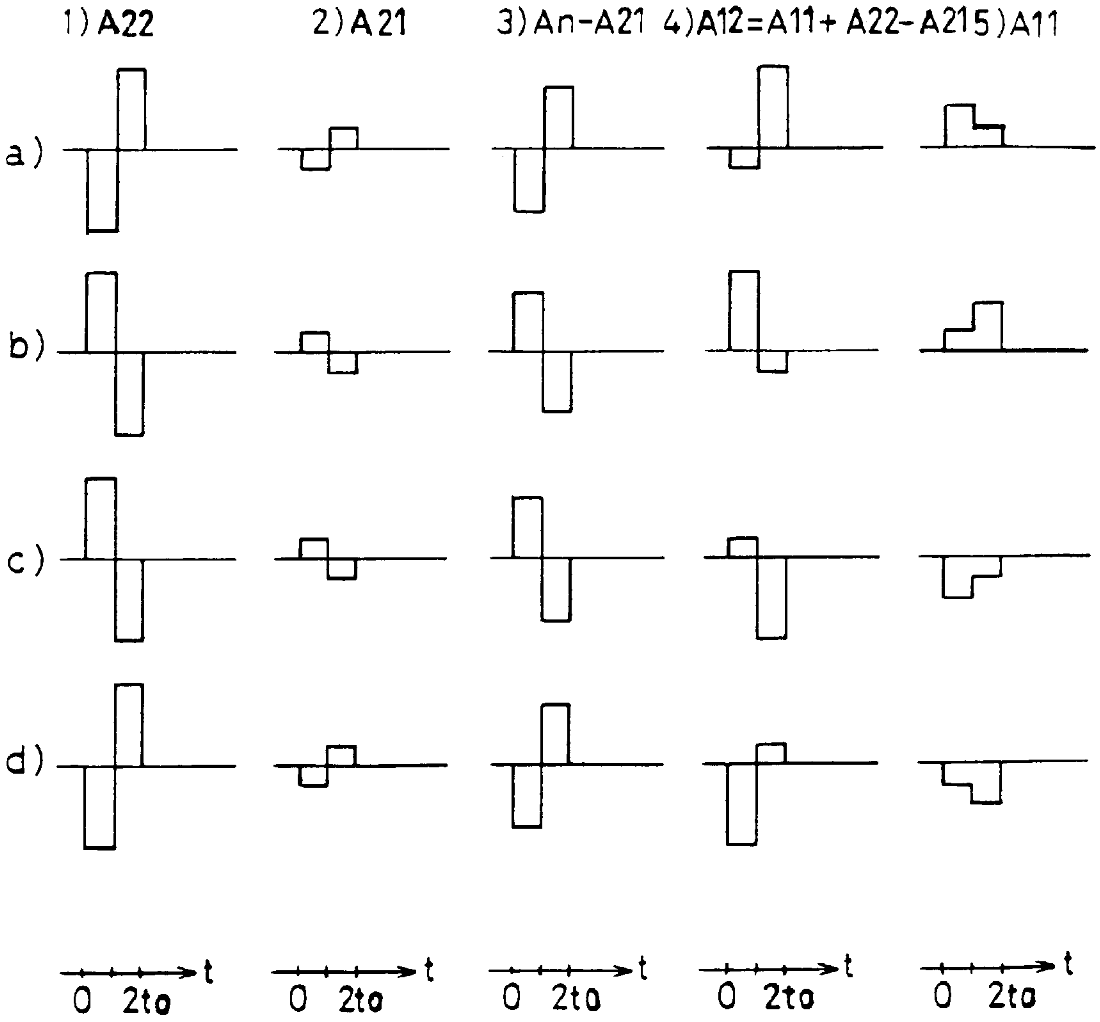


FIG. 23

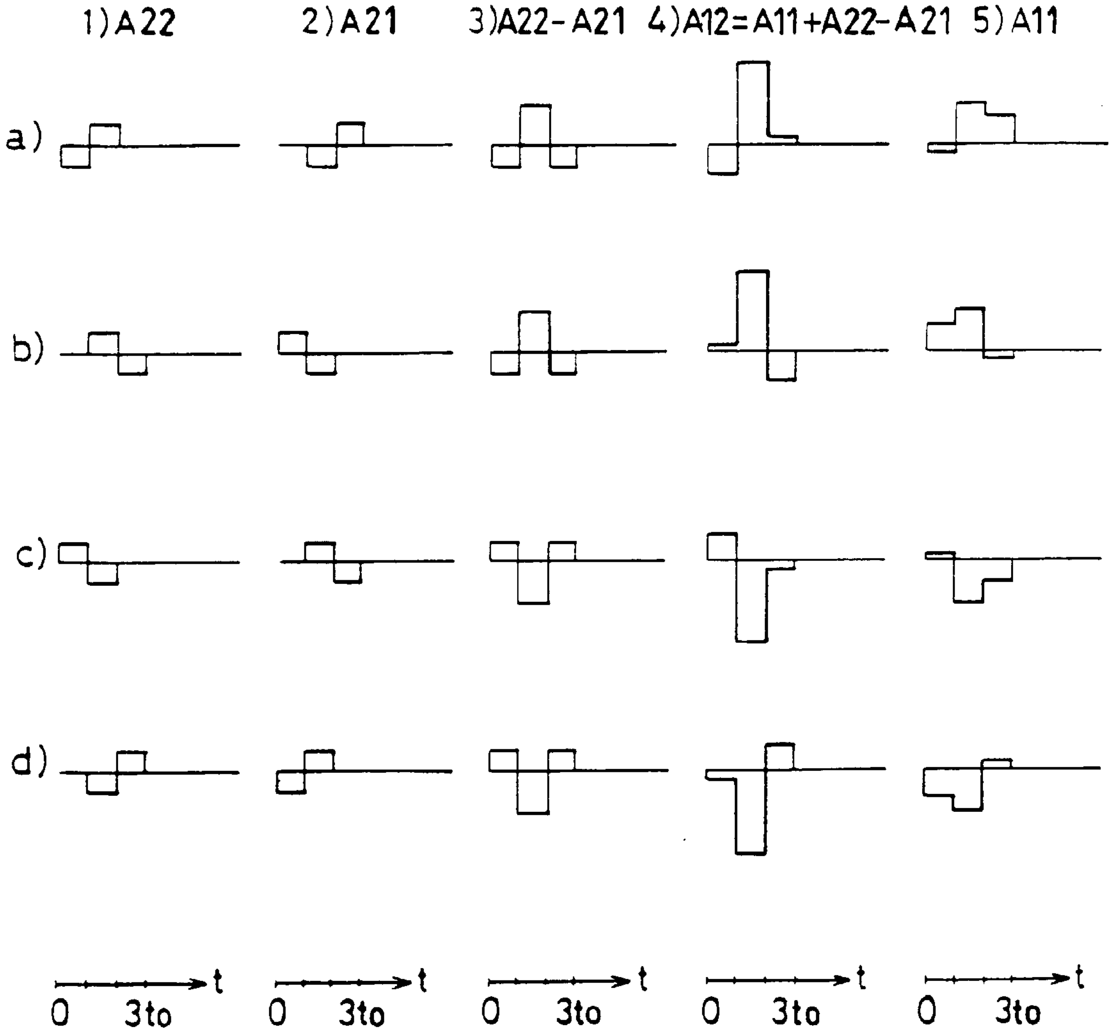


FIG. 24

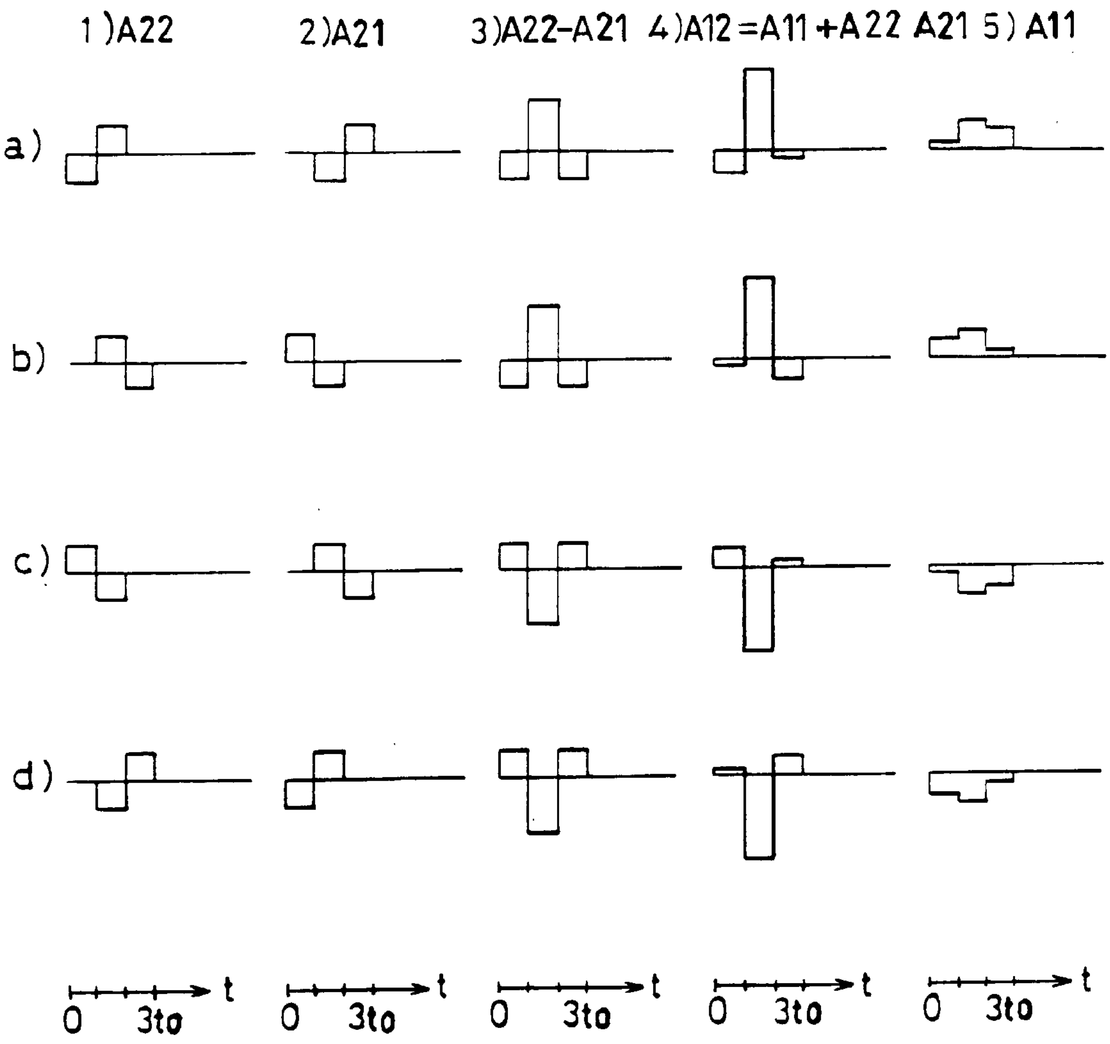


FIG. 25

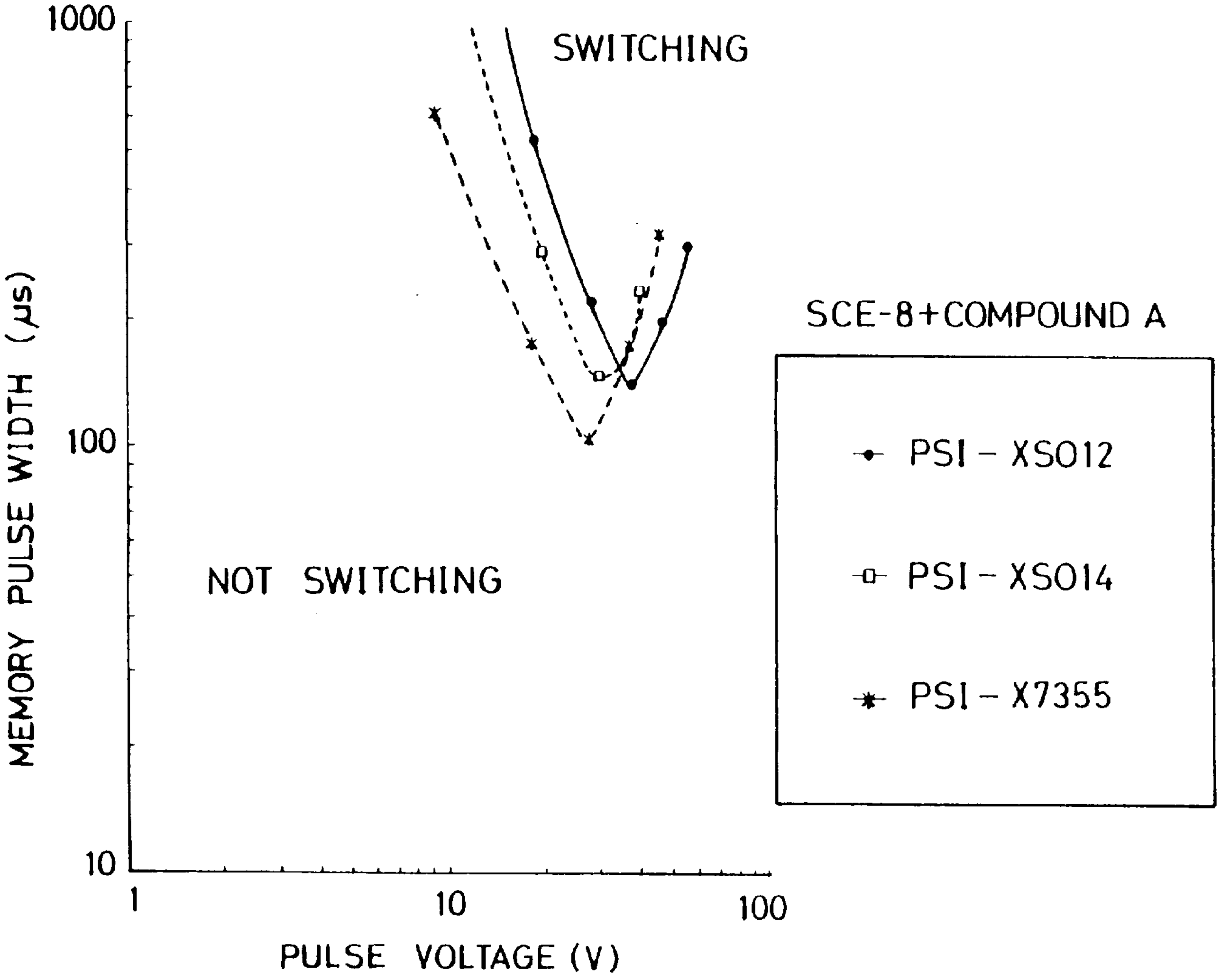
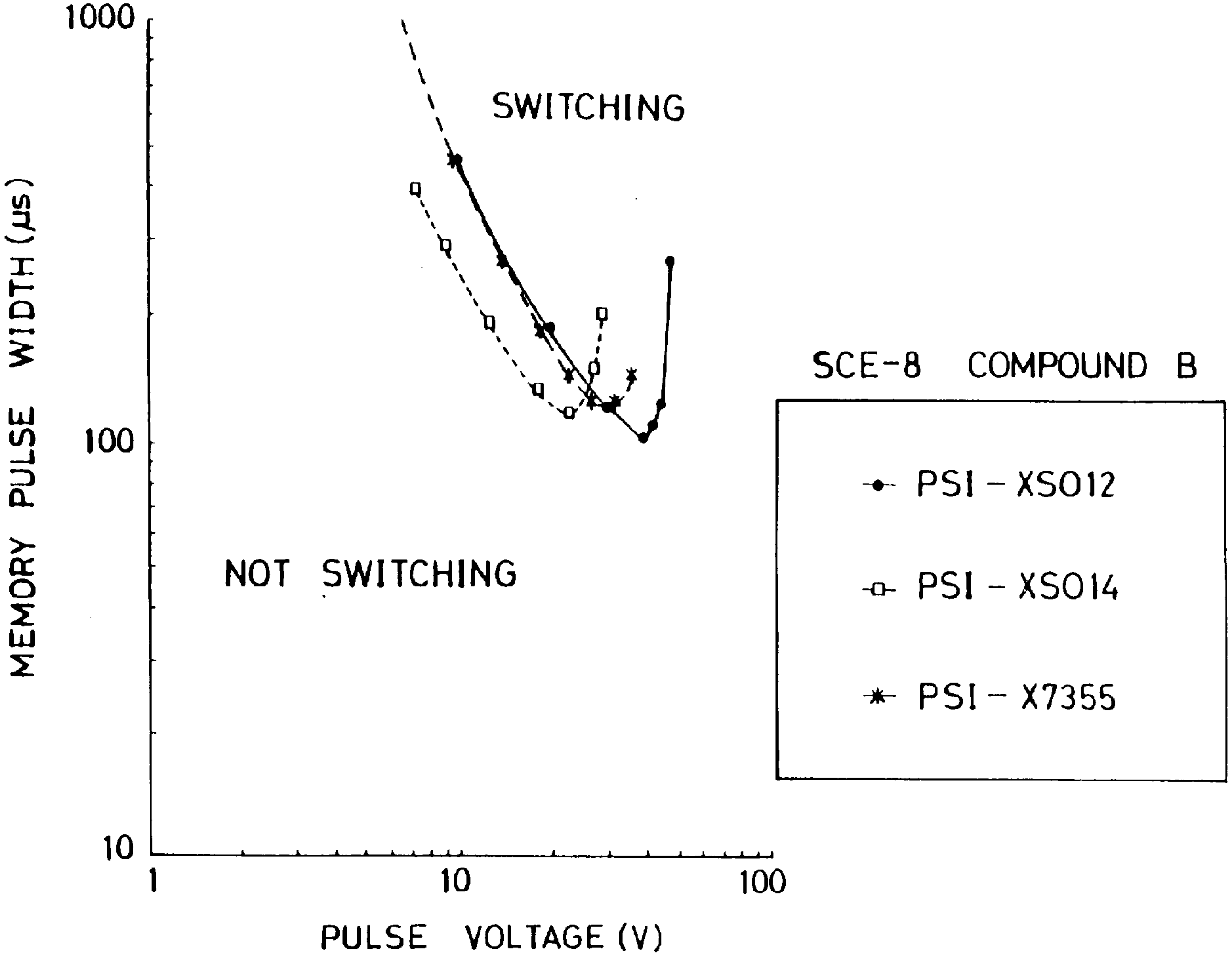

SWITCHING
NOT SWITCHING
MEMORY PULSE WIDTH (μs)
1000
100
10
1
10
100
PULSE VOLTAGE (V)
SCE-8+COMPOUND A
● PSI - XS012
□ PSI - XS014
✱ PSI - X7355

FIG. 26


1000
100
10
1
10
100
MEMORY PULSE WIDTH (µs)
PULSE VOLTAGE (V)
SWITCHING
NOT SWITCHING
SCE-8 COMPOUND B
-●- PSI - XS012
-□- PSI - XS014
-✱- PSI - X7355