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(71) Applicant
White's Electronics, Inc., 1011 Pleasant Valley Road, Sweet Home, Oregon, United States of America
(72) Inventor
George C Payne
(74) Agents
Potts, Kerr & Co., 15, Hamilton Square, Birkenhead, Merseyside L41 6BR

(54) Target Depth Reading Metal Detector

(57) A buried metal detector of the transmit-receive type includes a non-linear amplifier for producing a modified output signal whose amplitude is related to the depth that the detected metal object is buried below the transmit coil (10). A synchronous demodulator means (20) multiplies the receive coil (12) signal by a phase shifted reference signal (22) to eliminate mineral soil signal components from its demodulated output signal. The demodulated output signal is applied to the input of the non-linear amplifier (28) which compresses the signal amplitude variations of the demodulated output signals produced by metal objects buried at different depths. Amplifier (28) is preferably a logarithmic converter amplifier whose output signal amplitude is linearly related to target depth over a predetermined range of distance. The modified output signal is applied to a depth indicator means (30). The detector may also discriminate between different types of metal objects by the polarity of a discriminate demodulator (34) output signal which is combined with an audio oscillator (50) signal to provide a modulated output signal that is applied to an audible indicator means, such as a loud speaker (38), to indicate only desired metal objects.

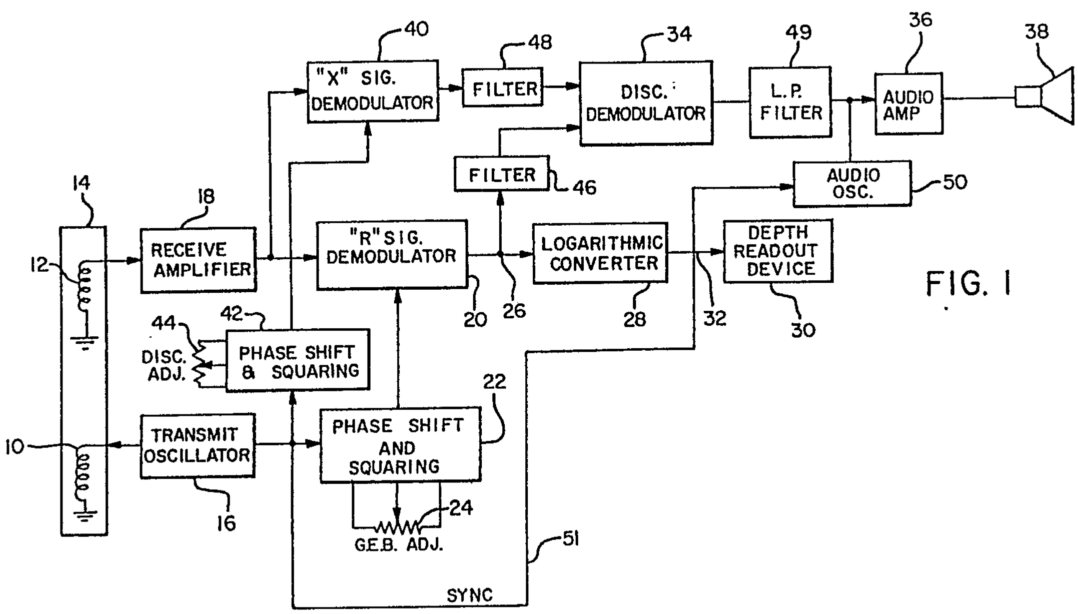

FIG. 1

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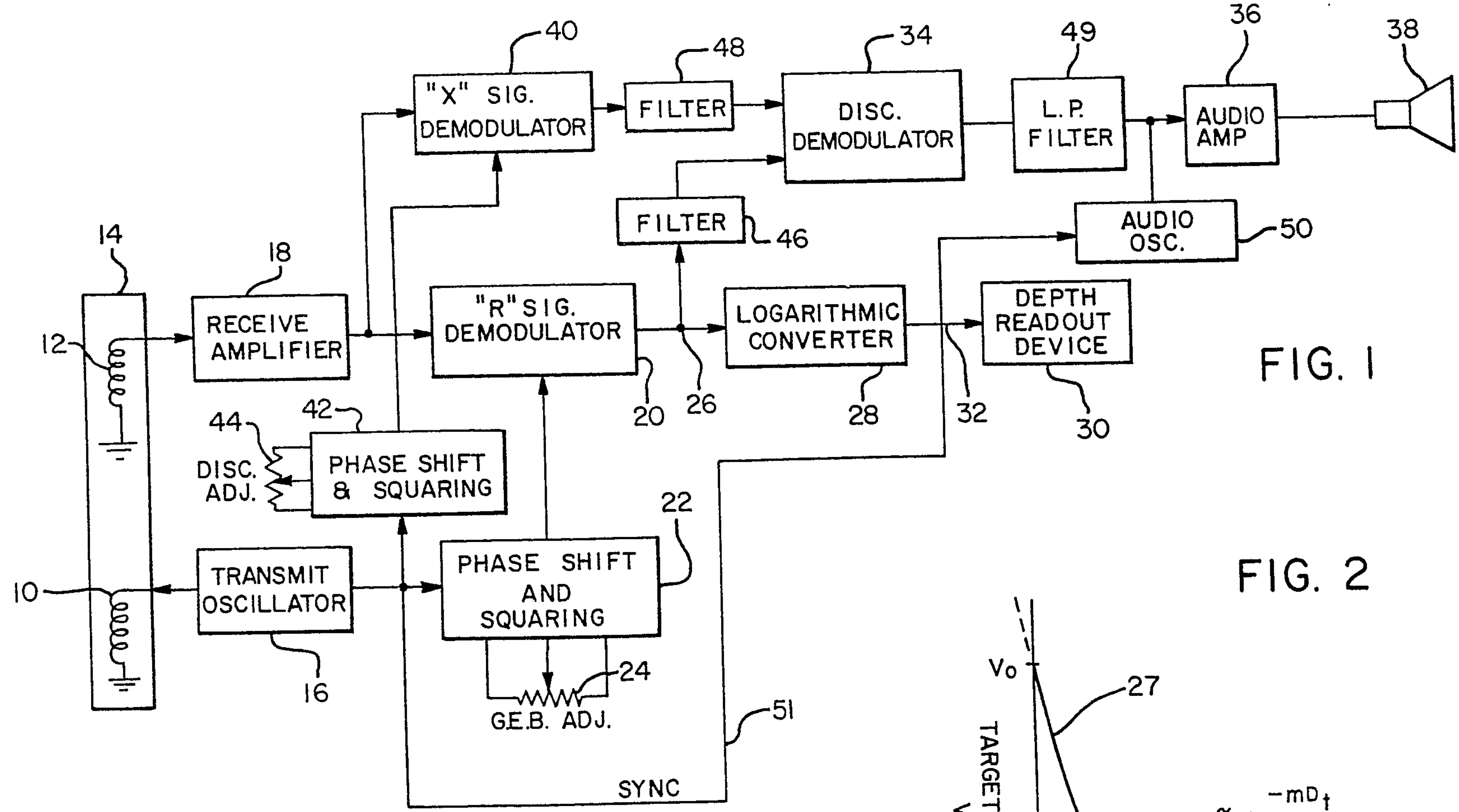

"X" SIG. DEMODULATOR
FILTER
DISC. DEMODULATOR
L.P. FILTER
AUDIO AMP
RECEIVE AMPLIFIER
"R" SIG. DEMODULATOR
FILTER
LOGARITHMIC CONVERTER
AUDIO OSC.
DEPTH READOUT DEVICE
PHASE SHIFT & SQUARING
DISC. ADJ.
TRANSMIT OSCILLATOR
PHASE SHIFT AND SQUARING
G.E.B. ADJ.
SYNC
10
12
14
16
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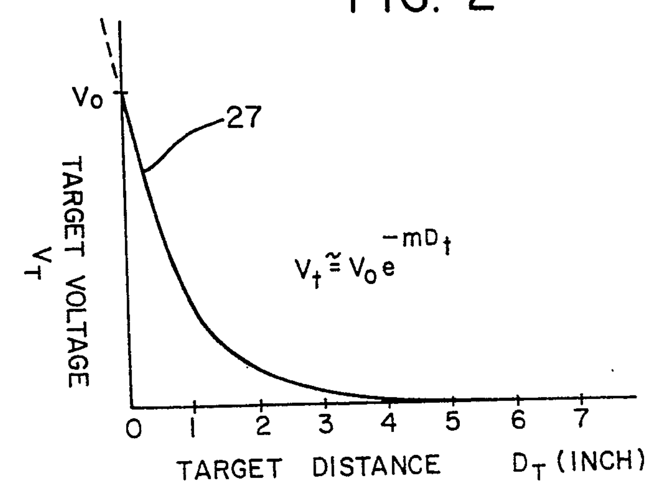
FIG. 1



V_o
27
$V_t \cong V_o e^{-mD_t}$
TARGET VOLTAGE V_T
0 1 2 3 4 5 6 7
TARGET DISTANCE D_T (INCH)

FIG. 2

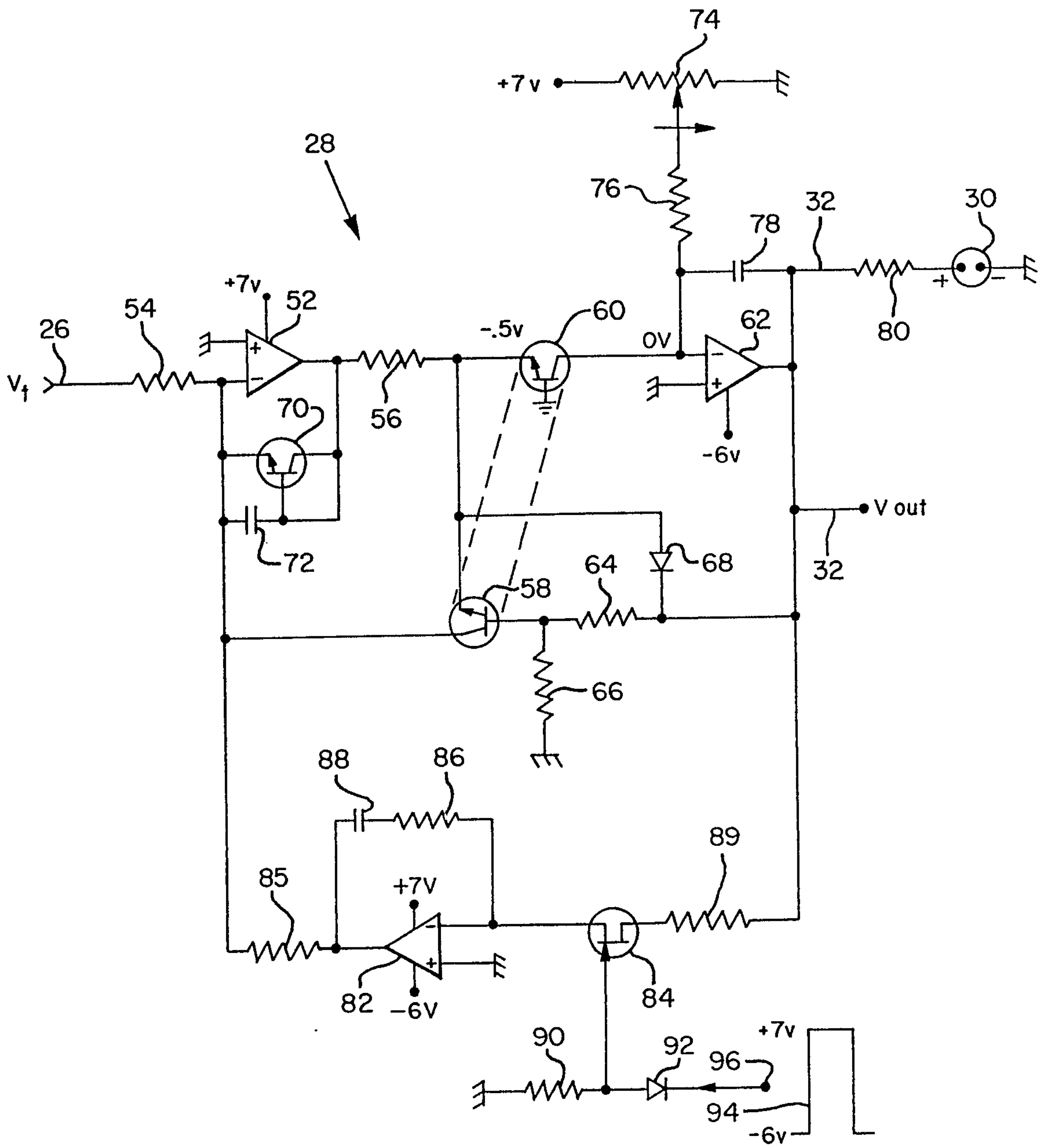

74
+7v
28
76
78
32
30
+
−
80
+7v
52
26
54
60
-.5v
62
0V
V_f
70
56
-6v
V out
72
68
64
32
58
66
88
86
89
85
+7V
82
-6V
84
90
92
96
+7v
94
-6v

FIG.3

SPECIFICATION

Target Depth Reading Metal Detector

Background of Invention

The subject matter of the present invention relates generally to metal detectors for detecting "buried" metal objects including those hidden from view in any manner, and in particular to such metal detectors which are capable of determining the depth that such metal objects are spaced below the transmit coil of such detector within a predetermined range of distance. The metal detector of the present invention is capable of detecting metal objects buried in magnetic mineral soil by employing synchronous demodulation in the manner shown in U.S. Patent No. 4,12Ø,8Ø3 of George C. Payne, issued December 5, 1978. It has been proposed in such patent to provide a buried metal detector which eliminates or reduces any mineral soil signal component of a receive signal while leaving the target signal component, and is also capable of discrimination between desired and undesired metal objects by the polarity of such target signal. However, such prior metal detector is not capable of measuring the depth that the metal object is buried below the surface of the ground. Thus, it does not employ a non-linear amplifier to compress signal amplitude variations in the demodulated receive signals produced by metal objects buried at different depths and thereby produce a modified output signal whose amplitude is related to such depth in the manner of the present invention.

It has been found that a logarithmic converter amplifier can be employed as the non-linear amplifier to produce a modified output signal whose amplitude is linearly related to the distance of the buried metal objects from the transmit coil over a predetermined range of distances. The metal detector of the present invention is particularly useful in detecting buried metal coins and other small objects and determining the depth that such objects are buried within a distance range of about six inches or less. However, it has been found that such metal detector can also be employed to detect large buried metal objects, such as battlefield relics or treasure container cans, a depth of up to five feet and to determine such depth, merely by changing the loop design and electrical component values.

It has been previously proposed in U.S. Patent No. 3,471,772 of Smith, granted October 7, 1969 and U.S. Patent No. 3,893,Ø24 of Humphreys, granted July 1, 1975 to provide a metal detector which employs a pair of receive coils vertically spaced a known distance and associated complex electrical circuitry to determine the distance that the metal object is buried below the transmit coil using a ratio of the receive signals produced by such pair of receive coils. Neither of these metal detectors employs a non-linear amplifier, such as a logarithmic converter amplifier, and a single receive coil to determine the distance a metal object is buried by receive signal amplitude compression in the manner of the present invention. Thus, the metal detector of the present invention is considerably simpler, less expensive and easier to operate than such prior depth measurement metal detectors. It has also been proposed in U.S. Patent No. 3,889,179 of Cutler, granted June 1Ø, 1975 to provide a buried metal detector which determines the depth of a buried electrical cable by means of a directional pick-up coil and an oscillator connected thereto whose frequency changes with coil position. The pick-up coil is moved over the surface of the ground at a predetermined angular relationship to such surface and triangulation based on the position of the pick-up coil is employed to determine the depth the cable is buried beneath the surface of the ground. This prior metal detector and method of measuring target depth is limited to buried electrical conductors with current flowing therethrough and is highly inaccurate. Unlike the present invention, it does not employ a non-linear amplifier, such as a logarithmic amplifier, to compress the receive signal amplitude and produce an output signal whose amplitude is linearly related to the depth that the metal target is spaced from the transmit coil.

In U.S. Patent No. 4,Ø3Ø,Ø26 of Payne, granted June 14, 1977 a sampling metal detector is described which detects metal objects buried in magnetic mineral soil. This metal detector eliminates the magnetic mineral soil signal component of a receive signal by sampling such receive signal at zero cross-over of such component. However, such metal detector does not determine the depth at which such metal objects are buried below the surface of such soil in the manner of the present invention. In this regard, it is similar to the above discussed U.S. Patent No. 4,12Ø,8Ø3 of Payne.

It is frequently desirable to determine the depth that a metal object is buried before digging so that the object is not damaged such as in the case of valuable coins or jewelry and ancient relics, or to determine the amount of digging necessary to uncover a metal object such as in the case of a buried pipe or cable. The metal detector of the present invention has the advantage of being able to not only locate metal objects buried in magnetic mineralized soil, but to also determine the depth that such objects are buried beneath the surface of such soil in a simple and inexpensive manner.

Summary of Invention

It is therefore one object of the present invention to provide an improved metal detector which is capable of detecting metal objects buried in magnetic mineral soil and determining the depths at which subject objects are buried.

Another object of the invention is to provide a metal detector which is capable of detecting buried metal objects and determining the depths at which subject objects are buried below the surface of the soil with an electrical circuit of simple and inexpensive construction employing a non-linear amplifier.

A further object of the invention is to provide such a metal detector in which the depths at which the metal objects are buried is accurately determined within a predetermined range and visually indicated to the operator.

An additional object of the present invention is to provide such a metal detector which determines the depth of a buried metal object by a non-linear amplifier which compresses signal amplitude variations between receive coil signals produced by metal objects buried at different depths.

Still another object of the invention is to provide such a metal detector employing a logarithmic converter amplifier, as the non-linear amplifier, to produce a modified output signal whose amplitude is linearly related to the buried depth of the metal object.

A still further object of the invention is to provide such a metal detector which is also capable of discriminating between desired and undesired metal objects.

Drawings

Other objects and advantages of the present invention will be apparent from the following detailed description of a preferred embodiment thereof and from the attached drawings of which:

Fig. 1 is a block diagram of the electrical circuit of one embodiment of a metal detector in accordance with the invention;

Fig. 2 is a plot of the receive signal target voltage produced by the receive coil at the input of the logarithmic converter in the metal detector of Fig. 1 as a function of the target distance from the transmit coil; and

Fig. 3 is an electrical circuit diagram of a logarithmic converter amplifier which can be employed in the metal detector of Fig. 1.

Description of Preferred Embodiment

As shown in Fig. 1, the metal detector of the present invention includes a transmit inductor coil 1Ø and a receive inductor coil 12 which are mounted in fixed relationship within a sealed search head 14. A transmit oscillator 16 producing a sine wave signal of audio frequency which is preferably about 6,59Ø hertz, is connected at one output to the upper terminal of transmit coil 1Ø whose lower terminal is grounded. The electromagnetic field produced by the transmit coil induces eddy current in buried metal objects or targets positioned within such field. These eddy current generate a secondary electromagnetic field which is sensed by the receive coil 12 to produce a receive signal. The receive signal is transmitted through a preamplifier 18 connected at its input to the receive coil. When a metal target is detected, the receive signal includes target signal components and also a mineral soil signal component if such target is buried in magnetic mineral soil.

The mineral soil signal component of the receive signal tends to obscure the target signal information and to avoid this problem, the receive signal is transmitted through a resistive or "R" signal demodulator 2Ø. The demodulator 2Ø is a synchronous demodulator having its signal input connected to the output of receive amplifier 18 and its reference input connected to the square wave signal output of a phase shift and squaring circuit 22 whose input is connected to another output of the oscillator 16. Such phase shifter circuit changes the sine wave oscillator signal into a square wave reference signal of 5Ø% duty cycle and the same frequency as such oscillator signal. The phase shifter 22 includes a phase adjustment potentiometer 24 which adjusts the phase of the reference signal applied to the demodulator 2Ø until it is approximately 9Ø° to the mineral soil signal so that the mineral soil signal component of the receive signal is eliminated from the demodulated output signal produced at the output 26 of such demodulator. This synchronous demodulation to eliminate the mineral soil signal is discussed in U.S. Patent No. 4,12Ø,8Ø3 of Payne and the advantages to using such a square wave reference signal is discussed in U.S. patent application Serial No. 875,677 of Karbowski, filed February 6, 1978. Thus, the phase adjustment potentiometer 24 is a ground exclusion balance (GEB) control which eliminates the mineral soil or "ground" signal component of the receive signal.

It has been found that the demodulated target voltage, V_t, produced at the output 26 of demodulator 2Ø has a signal amplitude which is related to the buried depth of the target, or more precisely, to the distance such target is spaced from the transmit coil 1Ø over a predetermined range of distances. As shown in Fig. 2, the target voltage, V_t, is related to the target distance, D_t, by a curve 27 which is approximately logarithmic for a predetermined range according to the equation

$$V_t \cong V_o e^{-mD_t} \qquad \text{Equation (1)}$$

where V_o is the target voltage at zero inches, m is a constant 1.14/inch, D_t is the target distance from the transmit coil in inches, and e is the base for a natural logarithm.

This logarithmic relationship between the target voltage and the target distance exists over a range of approximately Ø to 6 inches for small metal objects including coins, such as pennies, nickels, quarters, silver dollars and the like. The preferable portion of this range for close approximation of the logarithmic relationship is from 1 to 5 inches which is sufficient for most coin hunting.

A non-linear amplifier 28 which compresses signal amplitude variations between separately detected demodulated target signals produced by coins at different depths, is connected between the output of the R signal demodulator 2Ø and the input of a suitable depth readout device 3Ø. The readout device may be ammeter whose dial is calibrated in terms of target depth or distance of the metal object from the transmit coil. Preferably, the non-linear amplifier 28 is a logarithmic converter amplifier, such as the type shown in National Semiconductor Application Note AN—3Ø by Robert C. Dobkin, November 1969. As a result, a modified output signal is produced at the output 32 of the non-linear amplifier 28 whose amplitude is linearly related to the depth of the target so that the depth readout device 3Ø visually indicates the depth of such target on the dial of the meter. However, other types of non-linear amplifiers can be employed, including the voltage difference compression amplifiers known as "Companders", which can be used both for compression and expansion of electrical signal amplitudes in accordance with a known mathematical relationship which is not necessarily logarithmic. In this latter case, the amplitude of the modified output signal would not be linearly related to depth, but have another predetermined relationship.

The metal detector circuit of the present invention can also be provided with discrimination circuitry to discriminate between desired and undesired metal objects by the polarity of the output signal of a discrimination demodulator 34. The output of such demodulator is connected through an audio amplifier 36 to an audible indicator means 38 such as a loudspeaker or earphones. The reference input of the synchronous demodulator 34 is supplied by the output of R signal demodulator 2Ø and its signal input is supplied by the output of a reactive "X" signal demodulator 4Ø. The signal input of the X signal demodulator 4Ø is connected to the output of the receive amplifier 18 and the reference input of such demodulator is connected to the output of a second phase shift and squaring circuit 42. The phase shift and squaring circuit 42 has its input connected to the output of the transmitter oscillator 16 and includes a phase shift discriminate adjustment potentiometer 44 which provides an adjustable phase shift to a second reference signal produced at the output of phase shifter 42. Thus, the second reference signal applied to the X signal demodulator 4Ø is phase shifted differently from the first reference signal supplied by phase shifter 22 to the R signal demodulator 2Ø. This discriminate potentiometer 44 is adjusted to provide the output signals of the discriminate demodulator 34 with opposite polarity for desired and undesired metal objects including ferrous objects and non-ferrous objects or different types of non-ferrous metal objects such as coins and pull-tabs for cans, to enable discrimination between such desired and undesired objects. It should be noted that in practice the phase shifters 22 and 42 may be adjusted to a phase difference of 45° to exclude all ferrous objects and some non-ferrous objects such as pull-tabs so that only coins and other desired non-ferrous metal objects are detected.

Low frequency band pass filters 46 and 48 having a bandwidth of 5 Hertz and a center frequency of 15 Hertz are connected between the inputs of the discriminate demodulator 34 and the output of the R demodulator 2Ø and the X demodulator 4Ø, respectively. Each of these filters actually includes a high pass filter input stage and a band pass filter output stage. However, filters 46 and 48 act as band pass filters having a steep roll-off at its low frequency end of about 12.5 Hertz and a moderate roll-off at its high end of about 17.5 Hertz. Thus, filters 46 and 48 only pass low frequency or slowly varying D.C. signals to the discriminate demodulator 34. A low pass filter 49 with a cut-off frequency of about 7 Hertz is connected between discriminator demodulator 34 and audio amplifier 36 to eliminate harmonics.

A second audio frequency oscillator 5Ø which may be a frequency divider, is connected by a synchronizing conductor 51 to the output of the transmit oscillator 16, and has its output connected to the input of the audio amplifier 36. Thus, the audio frequency output signal of oscillator 5Ø is added to the slowly varying D.C. output voltage of the discriminator oscillator 34 to provide an amplitude modulated signal which is transmitted through the amplifier 36 to the loudspeaker 38. The presence of an output signal above a predetermined voltage level at the output of the demodulator 34 switches on the amplifier 36 and operates the speaker 38 to indicate the detection of a metal object.

If the discrimination feature is not required then the output of the R demodulator 2Ø can be connected directly to the input of the audio amplifier 36 by passing the discrimination demodulator 34 which can be eliminated. In this case, all detected metal objects will cause the audio indicator means, such as the loudspeaker 38, to produce a sound. However, in most cases it is preferred to have only desired metal objects detected and indicated by a sound output from the loudspeaker 38, in which case the discriminate demodulator 34 is employed along with the X signal demodulator 4Ø. As such, the discriminator operation of the present metal detector is similar to that described in U.S. Patent No. 4,128,8Ø3 of Payne.

Fig. 3 shows a logarithmic converter amplifier which can be employed as the non-linear amplifier 28 in the metal detector circuit of Fig. 1. Such logarithmic converter amplifier includes a first integrated circuit operational amplifier 52 of type LM 324 having its negative input terminal connected through a coupling resistor 54 of 3.3 kilohms to output 26 of the R signal demodulator 2Ø of Fig. 1. The positive input of such operational amplifier is grounded and its output terminal is connected through a coupling resistor 56 of 2.7 kilohms to the emitter of a first NPN transistor 58 of type MP31Ø. Transistor 58 has its collector connected to the negative input of operational amplifier 52 to provide a first negative feedback path from the output to the negative input of such operational amplifier. The output of operational amplifier 52 is also connected to the emitter of a second NPN transistor 6Ø of type MP31Ø whose collector is connected to the negative input of a second integrated circuit operational amplifier 62 of type LM324. The base of the second transistor 6Ø is grounded to provide a common base amplifier which is connected in a second feedback path from the output of the second operational amplifier 62 through a coupling resistor 64 and the emitter to base junction of the first transistor 58 to the negative input of the second operational amplifier to provide negative voltage feedback for such operational amplifier. As a result of such negative feedback, the negative input of amplifiers 52 and 62 is maintained at the zero volts D.C. level output voltage of such amplifiers.

A pair of voltage divider resistors 64 and 66 are connected in series from the output of the second operational amplifier 62 to ground with their common terminal connected to the base of first transistor 58. Voltage divider resistor 64 may be 29.4 kilohms while resistor 66 is 1 kilohm. An overvoltage protection diode 68 of type IN4148 is connected around the emitter to base junction of the first transistor 58 with its anode connected to the emitter and its cathode connected to the output terminal 32. Diode 68 prevents reverse bias voltage breakdown across the emitter to base junction of transistor 58. Another overvoltage protection diode in the form of a diode-connected transistor 7Ø of type MPS652Ø having its base shorted to its collector is connected between the output and negative input of the first operational amplifier 52. An AC coupling capacitor 72 of .ØØ1 microfarad is connected between the emitter and base of such transistor 7Ø and together with coupling resistor 56 stabilizes the feedback loop around the operational amplifier 52 to prevent oscillation.

A depth calibration potentiometer 74 of 5ØØ kilohms is connected by its movable contact through a coupling resistor 76 of 2.2 megohms to the negative input of the second operational amplifier 62. The opposite end terminals of the potentiometer 74 are connected to a positive D.C. voltage source of +7 volts and ground. The potentiometer supplies D.C. calibration current through the collector of transistor 6Ø because the negative input of operational amplifier 62 is kept at zero volts by negative feedback. A shunt capacitor 78 is connected from the output to the negative input of the second operational amplifier 62 for high frequency filtering and to prevent oscillation, such shunt capacitor having a value of .ØØ47 microfarads. The output terminal of the second operational amplifier 62 is connected to the output conductor 32 of the logarithmic amplifier circuit and supplies modified output signal of linearized amplitude through a coupling resistor 8Ø of 4.12 kilohms to the meter 3Ø which indicates the depth of the metal object detected.

The first transistor 58 is operated as the non-linear amplifier element of the logarithmic amplifier since the relationship between its collector current and its emitter to base voltage is logarithmic. This non-linear logarithmic amplifier operation is achieved in the following manner. The negative input terminal of the second operational amplifier 6Ø is maintained at zero volts by the second negative feedback path from its output through transistors 58 and 6Ø to the negative input of such operational amplifier. Since the negative terminal of operational amplifier 62 is maintained at zero volts, the collector current of the second transistor 6Ø is equal to the calibration current flowing through resistor 76. The base of second transistor 6Ø is grounded so that the emitter of the transistor is held at a constant negative D.C. voltage of about –Ø.5 volts to forward bias such transistor.

Similarly, first negative feedback path through transistor 58 from the output to the negative input of the first operational amplifier 52 maintains its negative input terminal at Ø volts. Therefore, all the input current flowing through input coupling resistor 54 flows through the collector of the first transistor 58. Such collector current also includes a D.C. reference current supplied by a third integrated circuit operational amplifier 82 of type CA314Ø having its negative input connected through a field effect transistor 84 of type 2NA3Ø2 and a coupling resistor 89 of 6.8 kilohms to the output of the second operational amplifier 62. Since the collector of first transistor 58 is maintained at the constant zero volts on the negative input of amplifier 52 and its emitter is kept at the constant –Ø.5 volts on the emitter of second transistor 6Ø, the voltage on the base of transistor 58 varies in a logarithmic relationship with its collector current including the input current applied to input terminal 26. This base voltage across resistor 66 is increased by the voltage divider operation to the modified output voltage produced across both resistors 64 and 66 of the voltage divider at the output terminal 32.

The output voltage on output 32 is reset to zero when transistor 84 is switched on to complete a third negative feedback loop through operational amplifier 82 from the output of amplifier 62 to the negative input of amplifier 52. The positive input of operational amplifier 82 is grounded and its output is connected through a coupling resistor 85 of 7.5 kilohms to supply reference current to the collector of first transistor 58. A shunt impedance including series resistor 86 of 75Ø ohms and capacitor 88 of 1.Ø microfarads, is connected from the negative terminal to the output of the third operational amplifier 82. Capacitor 88 is charged to a sufficient voltage to provide such reference current when the field effect transistor is switched off and causes the non-linear amplifier 28 to transmit a depth reading signal to meter 3Ø. The third operational amplifier 82 includes field effect transistor amplifier stages of extremely high input impedance to prevent the capacitor 88 from rapidly discharging through such amplifier.

The gate of PN junction field effect transistor 84 is connected to the common terminal of a shunt resistor 9Ø of 1 megohm having its other terminal grounded and the anode of a coupling diode 92 type

IN4148 whose cathode is connected to a source of control voltage signals 94 at control input 96. A square wave control voltage 94 which switches between a reset level of +7.Ø volts and a read level of −6.Ø volts is applied to input 96. Diode 92 is cut off by the +7.Ø volts positive reset pulse of control voltage 94 which switches the field effect transistor on and completes the third negative feedback loop through operational amplifier 82. This causes the output voltage on the output terminal 32 of the non-linear amplifier 28 to reset to zero volts. When the −6.Ø volts negative read pulse of the control voltage is applied, the diode 92 turns on and transmits such negative pulse to the gate of field effect transistor 84 to switch off such transistor. This opens the third feedback loop and capacitor 88 supplies the D.C. reference current through resistor 85 to the collector of first transistor 58 to produce a sufficient D.C. bias voltage on the base of such transistor to render it conducting. As a result, the first transistor is enabled to produce a modified output voltage across resistors 64 and 66 in response to the input signal current applied to input terminal 26. Of course, such input signal includes the target signal produced by any detected metal objects or targets. As a result the modified output voltage signal is linearly related to the logarithmic target voltage signal applied to input 26.

The output voltage, V_{out}, at output 32 is given by the equation:

$$V_{out}=\frac{KT}{q}\left[\frac{R_6+R_8}{R_7}\right] Ln \left[\frac{I_{c1}}{I_{c2}}\right] \quad \text{Equation (2)}$$

where I_{c1} and I_{c2} are the collector currents of the first and second transistors 58 and 6Ø, K is Boltzmann's constant, T is temperature in degrees Kelvin, g is the change of an electron, and R_6 and R_7 are voltage divider resistors 64 and 66.

Recalling that:

$I_{c2}=I_{cal}$, where I_{cal} is the calibration current through resistor 76.

$I_{c1}=I_{in}+I_{ref}$, where I_{in} is the input current through resistor 54 and I_{ref} is the reference current through resistor 85.

Then by substitution:

$$V_{out}=\frac{KT}{q}\left[\frac{R_6+R_7}{R_7}\right] Ln \left[\frac{I_{in}+I_{ref}}{I_{cal}}\right] \quad \text{Equation (3)}$$

An overall feedback loop is provided around the entire log circuit by amplifier 82. When the control voltage goes high, transistor 84 turns on and acts as a low resistance. The output voltage is applied directly to the negative terminal of amplifier 82. Negative feedback due to amplifier 82 will force the output voltage to zero by changing I_{ref} independently of I_{in}. Equation 3 reduces to:

$$V_{out}=\emptyset=\frac{KT}{q}\left[\frac{R_6+R_7}{R_7}\right] Ln \quad \frac{[I_{in}+I_{ref}]}{I_{cal}} \quad \text{Equation (4)}$$

Equation 4 can only be correct if:

$$I_{in}+I_{ref}=I_{cal}$$

With the control voltage high the circuit is initialized. The output voltage is at zero volts and the collector currents of transistors 58 and 6Ø are equal. Operational amplifier 82 will establish a voltage across capacitor 88 necessary to support the current required by I_{ref}. Since amplifier 82 is a FET amplifier with negligible bias current, the voltage across capacitor 88 will not change when the control voltage goes low. Then I_{ref} will note change. Equation 2 will now be:

$$V_{out}=\frac{KT}{q}\left[\frac{R_6+R_7}{R_7}\right] Ln \left[\frac{I_t+I_{cal}}{I_{cal}}\right] \quad \text{Equation (5)}$$

Where I_t is the target current signal transmitted through R_1 resistor 54.

Since:

$$I_t=V_t/R_1$$

The transfer function is given by:

$$V_{out}=\frac{KT}{q}\left[\frac{R_6+R_7}{R_7}\right] Ln \left[\frac{V_t+1}{R_1 I_{cal}}\right] \quad \text{Equation (6)}$$

For the condition:

$$\frac{V_t}{R_1 I_{cal}} \gg 1 \qquad \text{Equation (7)}$$

Equation 6 reduces to:

$$V_{out} \cong \frac{KT}{q} \left[\frac{R_6+R_7}{R_7}\right] \operatorname{Ln} \left[\frac{V_t}{R_1 I_{cal}}\right],$$

when

$$\frac{V_t}{R_1 I_{cal}} \gg 1 \qquad \text{Equation (8)}$$

Data taken of the logarithmic relationship of target distance versus target voltage shows that the relationship only holds over about two orders of voltage magnitude. At a large target to loop distance, this relationship changes. Intrinsic circuit noise and other limitations that exist when the target voltage is small make Equation 7 a practical restriction. Therefore, the log circuit follows equation 8 accurately for all practical purposes. Then the output voltage is proportional to the logarithm of the input voltage. Initially the base of transistor 58 will be at zero volts with its bulk emitter base voltage off-set by the emitter base voltage of transistor 6Ø. A target present will cause an incremental change in the collector current of transistor 58. Since the emitter voltage of transistor 58 cannot change, the full logarithmic incremental emitter base voltage increase will exist across resistor 66. An amplified version due to resistor 64 will be present at the output.

There are two major sources of temperature dependence in this circuit. Associated with both transistors 58 and 6Ø is the emitter saturation current (I_{es}). This current is highly temperature sensitive. The bulk change in emitter to base voltage with temperature is due to a change in I_{es}. Transistors 58 and 6Ø are a matched pair of monolithic transistors. Due to their construction they track thermally. The saturation currents of both transistors tend to track as well. By subtracting the emitter to base voltage of both transistors, it is possible to eliminate the circuit's temperature dependence due to variations in I_{es}. Any change in the emitter base voltage of transistor 58 due to temperature will be cancelled by an equal change in transistor 6Ø. The second source of temperature dependence will be discussed later. Specifically, it relates to the "T" term in the above equations.

Incremental Voltage Gain

The incremental voltage gain of the logarithmic converter circuit can be obtained as follows. Given that:

$$V_{out} = \frac{KT}{q} \left[\frac{R_6+R_7}{R_7}\right] \operatorname{Ln} \left[\frac{V_t+1}{R_1 I_{cal}}\right] \qquad \text{Equation (6)}$$

then:

$$\frac{dV_{out}}{dV_t} = \frac{KT}{q} \left[\frac{R_6+R_7}{R_7}\right] \left[\frac{R_1 I_{cal}}{V_t+R_1 I_{cal}}\right] \left[\frac{1}{R_1 I_{cal}}\right] \qquad \text{Equation (9)}$$

The incremental voltage gain is then simplified as:

$$\frac{dV_{out}}{dV_t} = \frac{KT}{q} \left[\frac{R_6+R_7}{R_7}\right] \left[\frac{1}{V_t+R_1 I_{cal}}\right] \qquad \text{Equation (1Ø)}$$

The initial circuit sensitivity after resetting is then:

$$\frac{dV_{out}}{dv_t} = \frac{KT}{q} \left[\frac{R_6+R_7}{R_1 R_7}\right] \left[\frac{1}{I_{cal}}\right], \text{ when } V_t = \emptyset \qquad \text{Equation (11)}$$

The initial sensitivity is inversely proportional to the calibration current, I_{cal}.

Scale Factor

$$V_{out} \cong \frac{KT}{q} \left[\frac{R_6+R_7}{R_7}\right] \operatorname{Ln} \left[\frac{V_t}{R_1 I_{cal}}\right],$$

$$\text{when } \frac{V_t}{R_1 I_{cal}} \gg 1 \qquad \text{Equation (8)}$$

The Equation for the scale factor is calculated as follows:

$I_o=V_o/R_5$, where R_5 is resistor 8Ø Equation (12) and I_o is the output current therethrough.

$$V_t=V_oe^{-mDt} \qquad \text{Equation (1)}$$

$$I_o\cong\frac{KT}{q}\left[\frac{R_6+R_7}{R_5R_7}\right]\ \mathrm{Ln}\left[\frac{V_oe^{-mDt}}{R_1I_{cal}}\right] \qquad \text{Equation (13)}$$

$$I_o\cong\frac{KT}{q}\left[\frac{R_6+R_7}{R_5R_7}\right]\ [-mD_t+\mathrm{Ln}(V_o/R_1I_{cal})]. \qquad \text{Equation (14)}$$

The scale factor,

$$\frac{dI_o}{dD_t},$$

for the meter is given by

$$\frac{dI_o}{dD_t}\cong-m\ \frac{KT}{q}\left[\frac{R_6+R_7}{R_5R_7}\right] \qquad \text{Equation (15)}$$

For $\frac{KT}{q}\cong25.27$ mv at 2Ø°C and m=1.14/inch,

and for the circuit component values selected, the scale factor is:

$$\frac{dI_o}{dD_t}\cong-2ØØ \text{ microamperes per inch at 2Ø°C (for small coins)}$$

Circuit Errors

The logarithmic converter circuit has two sources of error. The scale factor, Equation 15, is directly proportional to absolute temperature, T. The temperature sensitivity is +Ø.33%/°C at 25°C.

$$\frac{dI_o}{dD_t}=2ØØ \text{ microamperes per inch } \pm8\%\ Ø°C \text{ to } 5Ø°C.$$

For low target voltages Equation 8 is invalid. The circuit will not accurately take the logarithm of the input voltage. Typical circuit errors introduced by the approximation in Equation 8 are shown in Table 1.

Table 1

Circuit Error	*Target Distance Penny*
Ø.4%	3 Inches
1.7%	4 Inches
5.6%	5 Inches
17%	6 Inches

The errors shown here do not effect the overall circuit performance. Table I errors are offset by the calibration of the readout device (meter). The effective contribution of the scale factor temperature sensitivity is lower than that calculated. Generally the distance readings will be in error by only ±4% over the 5Ø degree temperature range. The temperature dependence of the scale factor and transfer function can be corrected by using a temperature sensitive resistor in place of resistor 66. The resistor should have a temperature coefficient of +Ø.35%/°C to achieve thermal stability. However, without compensation and over a limited temperature range the errors are already low. Because of the added cost in a temperature sensitive component its use is not presently being considered.

It will be obvious to those having ordinary skill in the art that many changes can be made in the above-described preferred embodiment without departing from thu invention. Therefore, the scope of the present invention should be determined by the following claims.

Claims

1. A metal detector circuit comprising: transmit coil means; oscillator means for generating transmit signals and providing reference signals corresponding thereto, and for applying said transmit signals to said transmit coil means to produce an electromagnetic field; receive coil means for producing receive signals in response to the detection of the presence of metal objects in said field, said receive signals including mineral soil signal components when the metal objects are buried in magnetic mineral soil; phase adjustment means for adjusting the phase of said reference signals relative to said receive signals to provide phase shifted reference signals; synchronous demodulator means for multiplying said receive signals by said phase shifted reference signals to produce a demodulated output signal from which mineral soil signal components have been removed; non-linear amplifier means for amplifying said demodulated output signal non-linearly to compress the signal amplitude variations of demodulated output signals produced by metal objects buried at different depths and thereby produce a modified output signal whose amplitude corresponds to the distance of the buried metal objects from the transmit coil; and depth indicator means connected to the output of said non-linear ampiifier means, for visually indicating said distance in response to receipt of said modified output signal.

2. A metal detector circuit in accordance with claim 1 in which the non-linear amplifier means produces a modified output signal whose amplitude is linearly related to said distance over a predetermined range of distances.

3. A metal detector circuit in accordance with claim 2 in which the non-linear amplifier means is a logarithmic converter amplifier.

4. A metal detector circuit in accordance with claim 1 in which the non-linear amplifier means is a voltage difference compression amplifier.

5. A metal detector circuit in accordance with claim 1 in which the depth indicator is a meter whose dial is calibrated in terms of distance.

6. A metal detector in accordance with claim 1 in which the synchronous demodulator means includes first and second synchronous demodulators for detecting the resistive and reactive signal components, respectively, of the receive signals by using two reference signals of different phase, and a third synchronous demodulator having inputs connected to outputs of said first and second demodulators to produce a discriminating output signal whose polarity indicates the type of metal object being detected.

7. A metal detector circuit in accordance with claim 6 which also includes an audible indicator means connected to the output of said third synchronous demodulator, for producing an audio output signal in response to the receipt of said discriminating output signal to indicate when a metal object is detected and to discriminate between different types of objects.

8. A metal detector circuit in accordance with claim 7 in which said audible indicator means includes a second oscillator producing an indicator signal of audio frequency and modulator means having inputs connected to said second oscillator and said third demodulator for amplitude modulating said indicator signal with said discriminating output signal.

9. A metal detector circuit in accordance with claim 2 in which the metal objects detected are coins and the range of distance is less than about six inches.

1∅. A metal detector circuit in accordance with claim 1 in which the oscillator produces the transmit signal as a sine wave of audio frequency.

11. A metal detector circuit in accordance with claim 1 in which the demodulated output signal includes a target voltage, V_t, for each detected metal object which approximately follows the relationship:

$$V_t = V_o e{-}mD_t$$

where V_o is the target at zero inches from the transmit coil, D_t is the target distance from the transmit coil, e is the base for a natural logarithm, and m is a constant.

12. A metal detector circuit in accordance with claim 3 in which the logarithmic converter amplifier circuit includes: a pair of first and second operational amplifiers; a pair of first and second transistors; input means for applying said demodulated output signal to one input of said first operational amplifier; first connection means for connecting said first transistor in a first negative feedback path from the output to said one input of said first operational amplifier; second connection means for connecting said second transistor in a second negative feedback path from the output to one input of said second operational amplifier through said first transistor, and for connecting the input of said second transistor to the output of said first operational amplifier; and output means connected between the output of said second operational amplifier and said first transistor for supplying said modified output signal to said indicator means.

13. A metal detector circuit in accordance with claim 12 in which the output means includes a pair of voltage divider resistors connected in series and having their common connection connected to the base of said first transistor.

14. A metal detector circuit in accordance with claim 12 in which the second transistor is

connected as a common base amplifier with its emitter connected to the output of said second operational amplifier and to the emitter of said first transistor.

15. A metal detector circuit in accordance with claim 12 which includes reference current means for supplying D.C. reference current to a common connection of the collector of said first transistor and said one input of said first operational amplifier; and adjustable calibration current means for applying a variable D.C. calibration current to a common connection of the collector of said second transistor and said one input of said second operational amplifier.

16. A metal detector circuit in accordance with claim 15 in which the reference current means includes an electronic switch means and a third operational amplifier connected in a third negative feedback path between the output of said second operational amplifier and said one input of said first operational amplifier, said switch means being operated by a control signal to vary the reference current supplied to said first transistor and thereby control the operation of the logarithmic amplifier circuit.

17. A metal detector circuit comprising: antenna means; oscillator means for generating transmit signals and for applying said transmit signals to said antenna means to produce an electromagnetic field; receive means in said antenna means, for producing receive signals in response to the detection of the presence of metal objects in said field; demodulator means for demodulating said receive signals to produce a demodulated output signal; non-linear amplifier means for amplifying said demodulated output signal non-linearly to compress the signal amplitude variations therein caused by metal objects buried at different depths and thereby produce a modified output signal whose amplitude is related to the distance of the buried metal objects from the antenna means; and depth indicator means connected to the output of said non-linear amplifier means, for visually indicating said distance in response to receipt of said modified output signal.

18. A metal detector circuit in accordance with claim 17 in which the non-linear amplifier means produces a modified output signal whose amplitude is linearly related to said distance over a predetermined range of distances.

19. A metal detector circuit in accordance with claim 18 in which the non-linear amplifier means is a logarithmic converter amplifier.

2Ø. A metal detector in accordance with claim 17 in which the demodulator means includes first and second synchronous demodulators for detecting the resistive and reactive signal components, respectively, of the receive signals by using two reference signals of different phase, and a third synchronous demodulator having inputs connected to outputs of said first and second demodulators to produce a type of metal object being detected.

21. A metal detector circuit in accordance with claim 2Ø which also includes an audible indicator means connected to the output of said third synchronous demodulator, for producing an audio signal in response to the receipt of said discriminating output signal to indicate when a metal object is detected and to discriminate between different types of objects.

22. A metal detector circuit in accordance with claim 21 in which said audible indicator means includes a second oscillator producing an indicator signal of audio frequency and modulator means having inputs connected to said second oscillator and said third demodulator for amplitude modulating said indicator signal with said discriminating output signal.

23. A metal detector circuit in accordance with claim 19 in which the logarithmic converter amplifier circuit includes: a pair of first and second operational amplifiers; a pair of first and second transistors; input means for applying said demodulated output signal to one input of said first operational amplifier; first connection means for connecting said first transistor in a first negative feedback path from the output to said one input of said first operational amplifier; second connection means for connecting said second transistor in a second negative feedback path from the output to one input of said second operational amplifier through said first transistor, and for connecting the input of said second transistor to the output of said first operational amplifier; and output means connected between the output of said second operational amplifier and said first transistor for supplying said modified output signal to said indicator means.

24. A metal detector circuit in accordance with claim 23 in which the output means includes a pair of voltage divider resistors connected in series and having their common connection connected to the base of said first transistor.

25. A metal detector circuit in accordance with claim 23 in which the second transistor is connected as a common base amplifier with its emitter connected to the output of said second operational amplifier and to the emitter of said first transistor.

26. A metal detector circuit in accordance with claim 23 which includes reference current means for supplying a D.C. reference current to a common connection of the collector of said first transistor and said one input of said first operational amplifier; and adjustable calibration current means for applying a variable D.C. calibration current to a common connection of the collector of said second transistor and said one input of said second operational amplifier.

27. A metal detector circuit in accordance with claim 26 in which the reference current means includes an electronic switch means and a third operational amplifier connected in a third negative feedback path between the output of said second operational amplifier and said one input of said first

operational amplifier, said switch means being operated by a control signal to vary the reference current supplied to said first transistor and thereby control the operation of the logarithmic amplifier circuit.

28. A metal detector circuit constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawings.

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