FPGA experience and SoC design methodology

SEFUW, ESTEC 2018

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Contents

FPGA Experience at Airbus Defence and Space

Antifuse FPGAs

	RTSX32/72	RTAX2000/4000	RTAX2000D/4000D
Complexity	Small	Medium	Medium
Special features	5V compatible	RAM	RAM+MATH
Applications	Control	Complex Control Data handling	Signal processing
Product examples	Power, Motor	Mass memory, ICU, OBC, Power, Motor	Instrument
Prototyping	Commercial device	Progr. Adapter Commercial device (AX)	Progr. Adapter PROTO device
Export restriction	Yes	Yes	Yes
Comment	Almost 20 years on the market	High runner with well established development flow.	Special devices which are only used if no other solution reasonable.

Reprogrammable FPGAs

	(RT-)PA3	RTG4	Spartan-6	Virtex XQR5VFWX130	BRAVE-Medium	BRAVE-Large
Technology	FLASH	FLASH	SRAM	SRAM	SRAM	SRAM
Complexity	Medium	Large	Large	Large	Medium	Large
Hardened	SW-TMR	Technology	SW-TMR	Technology	Technology	Technology
Special features	RAM	RAM+MATH+ PLL+HSSL	RAM+MATH+ PLL+HSSL	RAM+MATH+ PLL+HSSL	RAM+MATH+ PLL	RAM+MATH+ PLL+HSSL
Applications	Control	SoC, High perf. data handling	GNSS, Compression	Compression	evaluation	evaluation
Products examples	Motor	Mass memory	Communication, Navigation		evaluation	evaluation
Prototyping	Commercial device	Proto-Device	COTS	Commercial device		
Export restriction	RT only	Yes	No	yes	No	No
Comment			AIRBUS COTS		SW+HW Evaluation ongoing	

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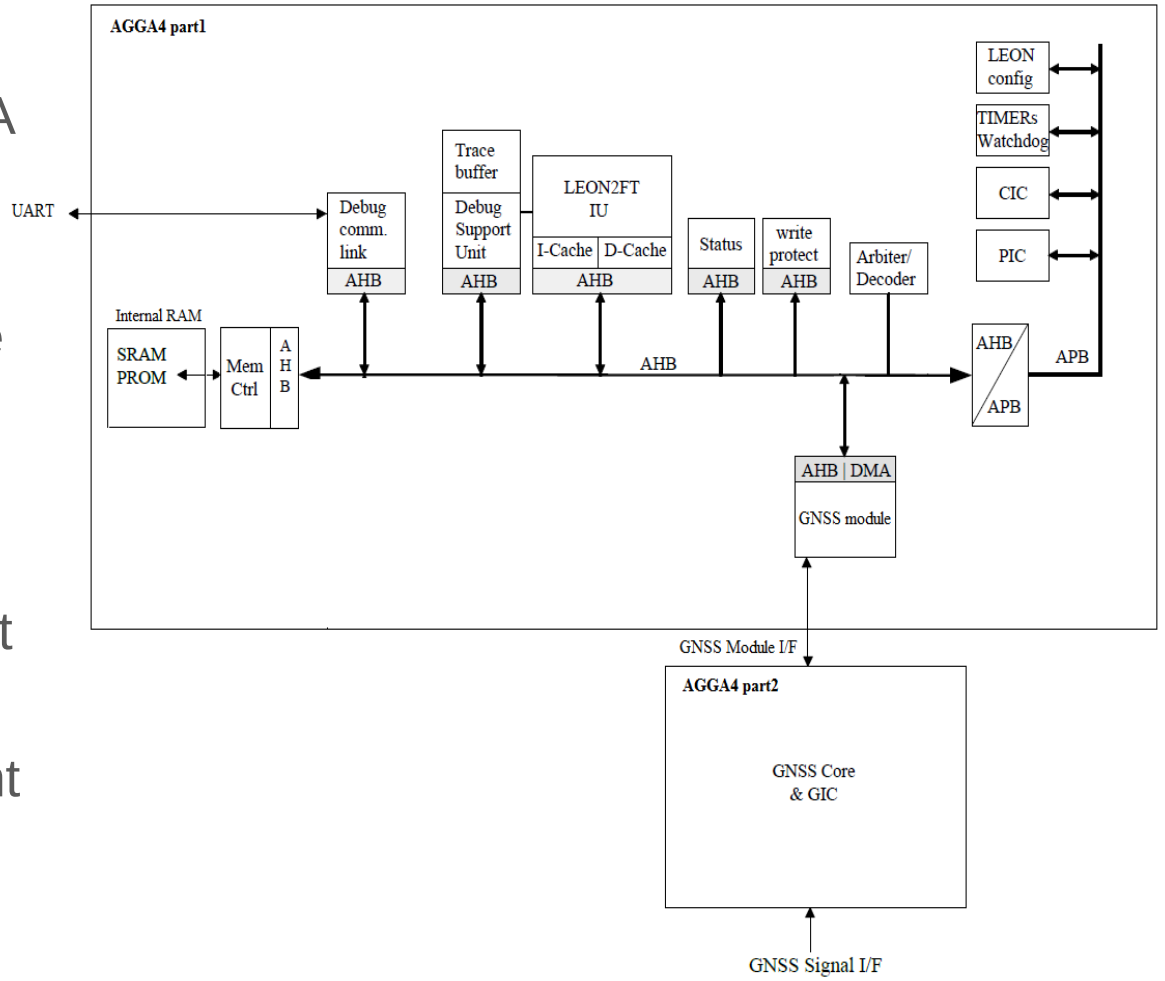
BRAVE-Medium 1/2

AGGA4 ASIC ported to BRAVE NG-MEDIUM:

- Design split in 2 parts, since too big for 1 FPGA
  - LEON2 + AMBA bus + peripherals is Part1
  - GNSS receiver is Part2
- Multiple iterations of synthesis, place and route with various NanoXmap settings to achieve best results
- Functional verification through simulations with the netlist generated after synthesis, placement and routing.
- Physical tests on Part1 with the development kit board: Demo SW program ran on LEON2



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BRAVE-Medium 2/2

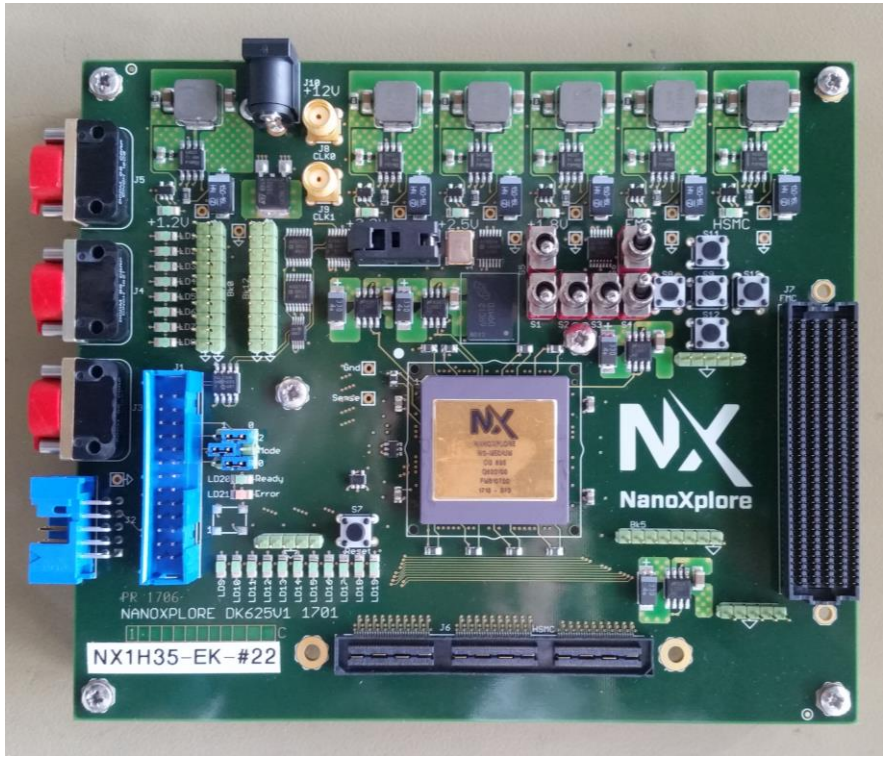
Digital Signal Processing algorithm (Radix-2) synthesized, placed and routed.

- Resource utilization and maximal frequency results comparable to RTG-4

Technology demonstrated to work by porting LEON2FT and executing correctly simple application.

SW tools are brand new

- Main challenges on synthesis stage
- SW tools are constantly improved.
- Better performance with each version.



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FPGA Trends

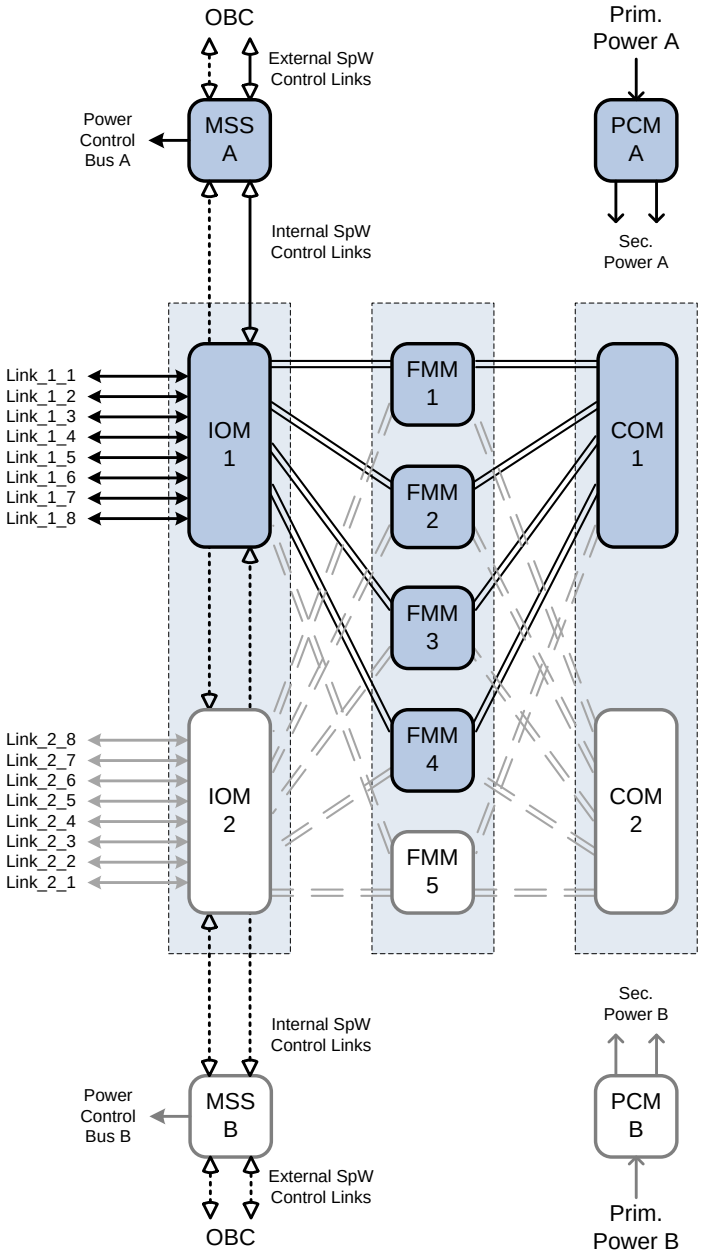
More complex FPGA’s and designs

Higher integration of boards

More COTS devices used

HSSL will dominate the communication

SW and HW will come together in SoC



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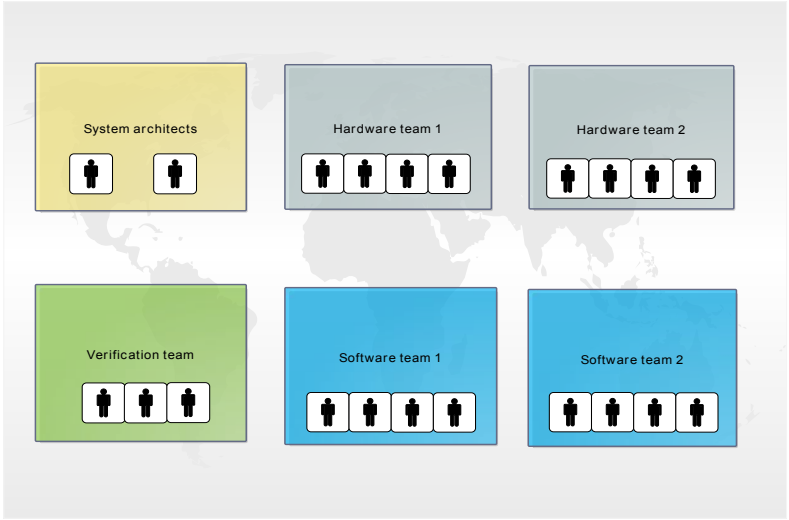
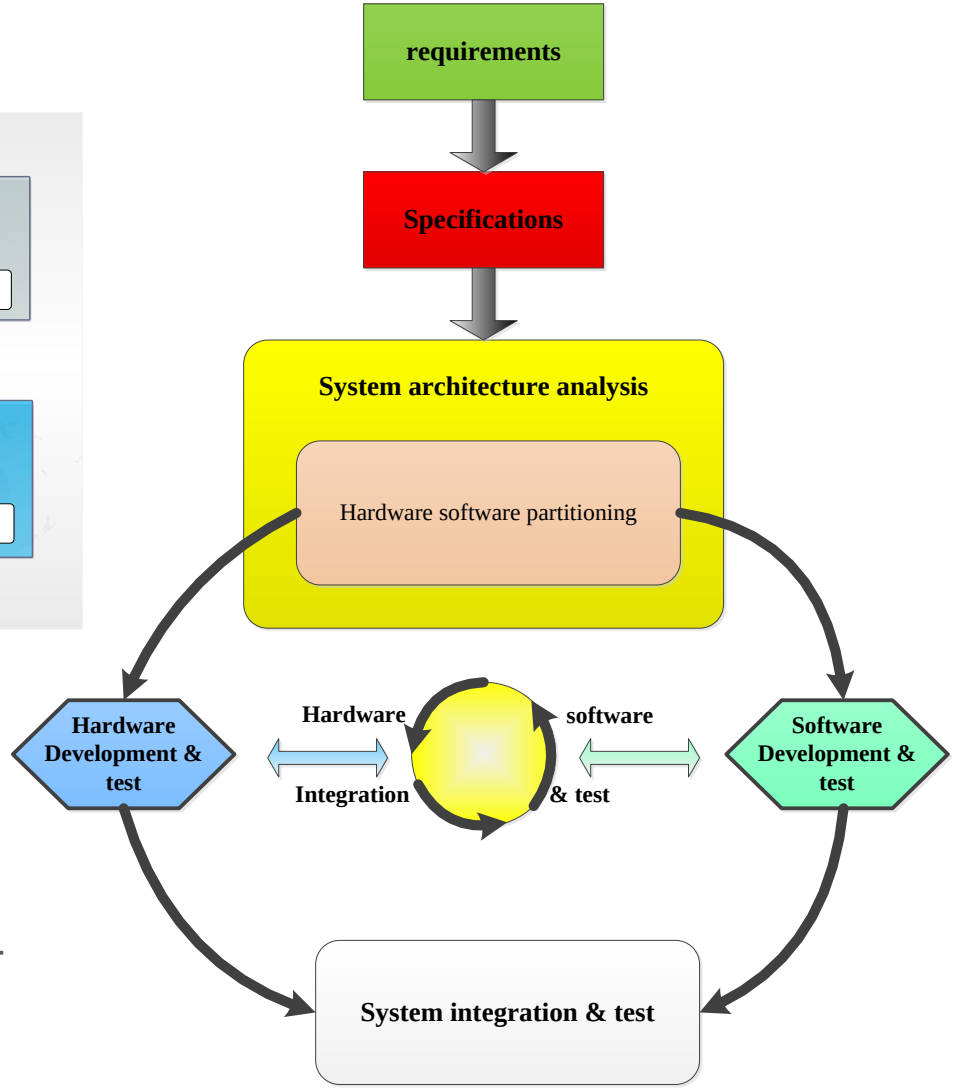
SoC Design Methodology

Development organisation

Even if the methodology is the same, the capacity and performances of large FPGA make that :



- Large design teams may be distributed in several companies
- Several HW and SW modules are designed separately by different teams
- The use of IP are increased
- The use of high level languages to describe the FPGA behaviour is necessary to perform the HW/SW partitioning



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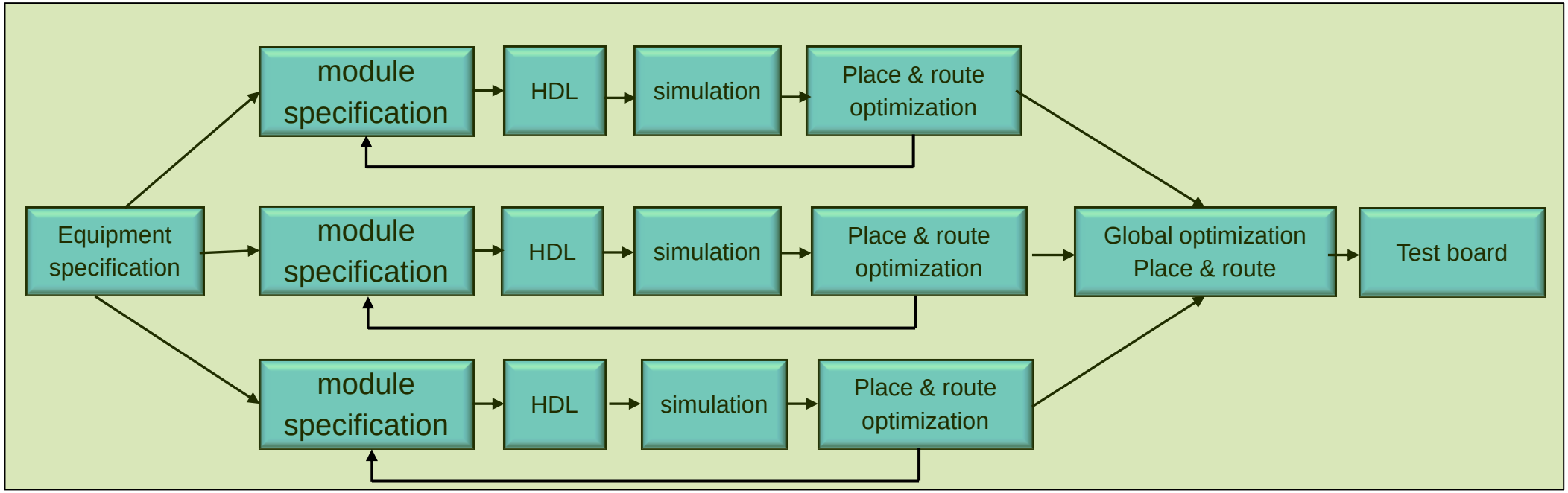
Design phase

The equipment specification is distributed in module specifications which are designed separately
A first place & route analysis is done at local level, second is done if necessary during the synthesis of all functions
Software is integrated at this level.



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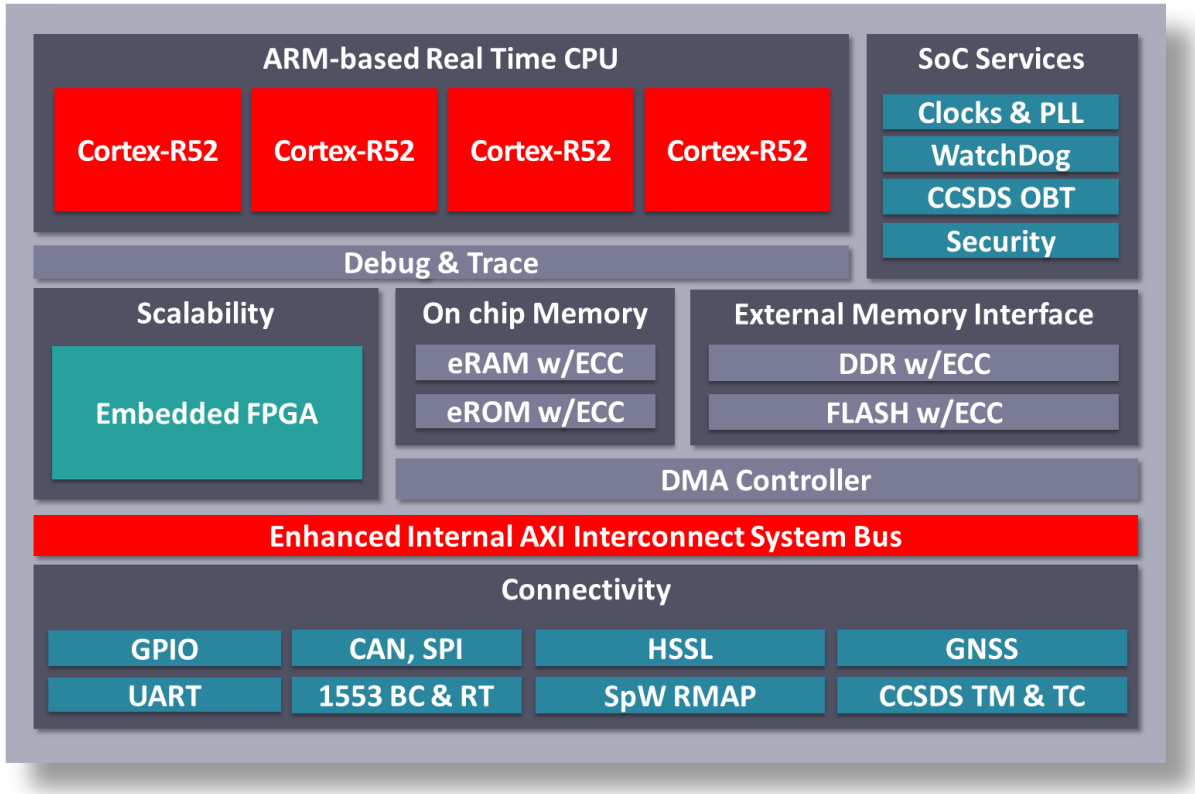
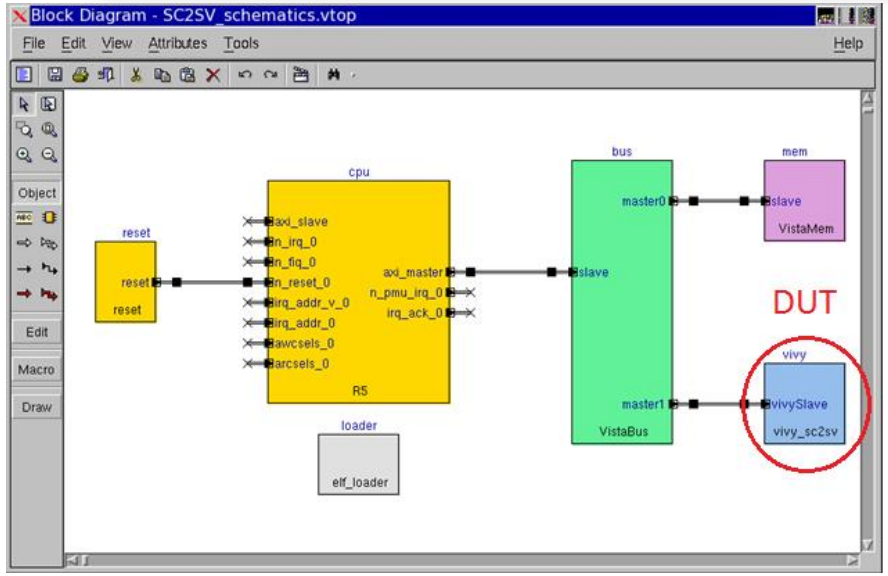
Mentor Vista evaluation 1/2

- Integration and system functionality verification with the use of Vista and Questa.
- Evaluation in frame of DAHLIA project.
- Vista provides model library in SystemC (CPU, Memories, Interconnects, etc.).
- Vista providing software stimulus to the RTL DUT for peripheral accesses through interconnect.
- System Verilog Testbench for Data transfer from Vista model (SystemC) to RTL DUT (conversion from generic payload to AXI transactions).





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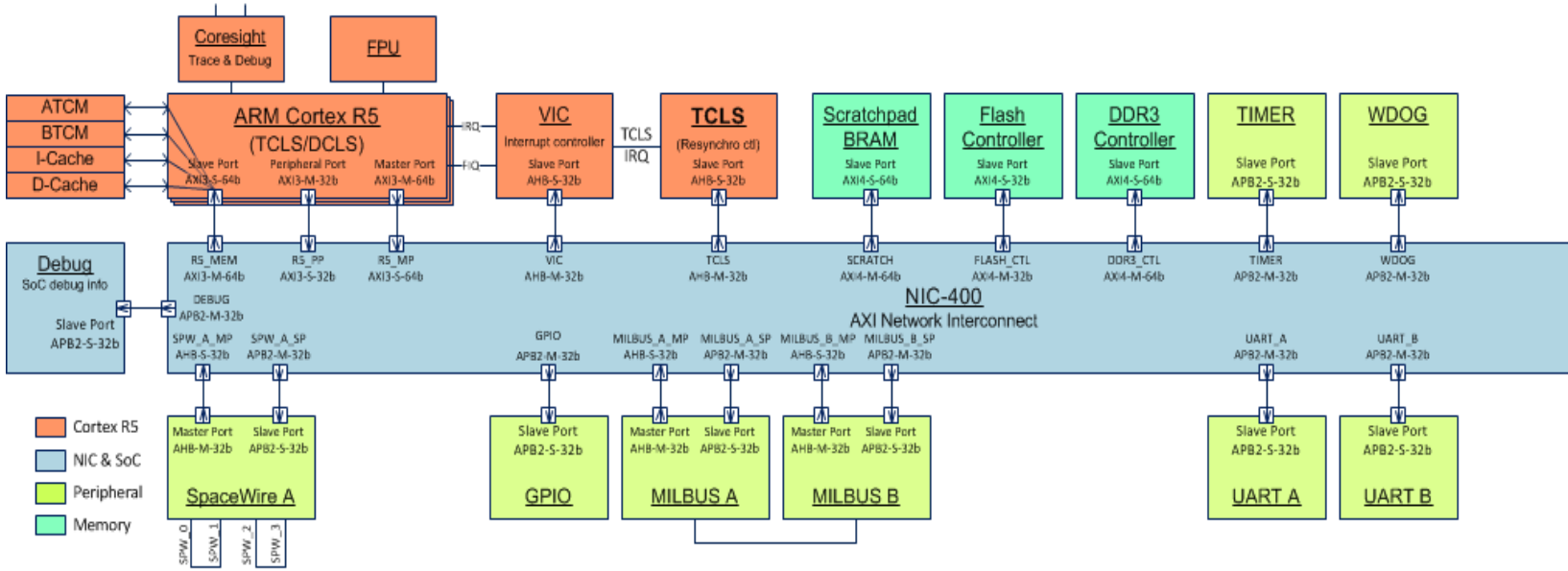
Mentor Vista evaluation 2/2

- Successful conversion of generic payload into AXI transactions.
- Successful peripheral AXI read and write accesses through the Interconnect.
- Replacement of RTL modules with Vista models reduces the simulation time allowing software test-case execution (~60-80% of the design is modelled in Vista).
- Easy usage of the model libraries of Vista and easy model configuration.
- Easy AXI protocol violations monitoring.

- No cycle accurate simulation results for the SystemC parts

- Future use for evaluation of the overall performance of SoC and debugging purposes.



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Conclusion

The complexity of FPGAs will further grow into the System on Chip area

The development flow must be adapted to distributed System on Chip design

Tools shall support efficiently the handling of this complexity

Thank you

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