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COMMUNICATIONS

A METHOD FOR CONTINUOUS TUNING OF MOSFET–RC FILTERS WITH EXTENDED CONTROL RANGE

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In this paper a tuning structure for a MOSFET?RC filters is presented. The proposed tuning structure is composed of switched resistor banks with voltage controlled transistors. The voltage controlled transistors use active feedback with extended control range for continuous filter parameter tuning, without degrading the total linearity performance of the filter. The proposed tuning structure is tested by implementing it in a second order low pass biquadratic filter cell in 65 nm CMOS technology. The designed filter has a highly reconfigurable response, ranging from Chebyshev to Bessel, a tuneable -3 dB bandwidth from 10 MHz to 100 MHz and can be used for multiple standard wireless solutions. Filter IIP3 performance is not degraded when the bandwidth is continuously tuned by 40 % with a 1 V pp input. The maximum power dissipation, including active feedback circuits, is 17.2 mW from a 1.2 V source when the filter is tuned to 100 MHz bandwidth.

K e y w o r d s: continuous tuning, integrated filter, linearity, MOSFET-RC, reconfigurable, software-defined radio

1 INTRODUCTION

The ever-growing number of wireless communication standards has created a new trend in designs of wireless transceivers. Modern mobile transceivers should comply with a multitude of existing or developing wireless standards as the industry shifts to the software-defined radio (SDR) technology [1, 2]. Due to its simplicity, direct conversion transceiver architecture is best suited for SDR implementation [3]. The reconfigurable nature of the SDR requires that the baseband channel selection filters, used in direct conversion architectures, should have a high degree of filter configuration capabilities, mainly centered, but not limited to: bandwidth, power dissipation, filter response and order.

Most of the time, flexible channel selection filters are based on active-RC, gm-C or current amplifier designs [4, 5]. High bandwidth applications usually use gm-C filters, but for application that require high linearity active-RC filter are still the best due to their large dynamic range, although they suffer from variations in process, voltage and temperature (PVT) [6, 7]. PVT variation problem can be partially mitigated by the use of switched-R-MOSFET-C circuits, where accurate time-constants can be achieved based on duty cycle tuning [7]. Due to a more digital nature of the switching gates, even fully synthesizable solutions for switched-R-MOSFET-C circuits are reported [8]. One major drawback of such filters is the need of a high frequency clock signal to implement filter blocks with wide bandwidths. Moreover, a highly reconfigurable filter design, intended for SDR technology, could only be achieved by adding complex divider circuits and a dedicated PLL, both of which increase the complexity and design time of the transceiver.

Compared to active-RC filters with fixed capacitor and resistor tuning steps [9], MOSFET-RC filter structures are more suited for SDR transceivers due to their tuning flexibility and accuracy. While high bandwidth MOSFET-RC filters usually dissipate more power than other filter types, precise Q tuning methods can reduce the total power consumption by optimizing the operational amplifier biasing currents [10, 11]. Nonetheless, one of the major drawbacks of continuous MOSFET-RC tuning is the linearity degradation due to the non-linear transistor behavior. In this work a tuning method with active feedback for structures of MOSFET-RC filter is proposed, which overcomes the linearity degradation problem when the filter is tuned over its bandwidth or Q settings and does not increase the noise generation as in the case of [12]. A low pass biquadratic filter cell is designed to test the proposed tuning structure. It uses only one type of resistor and capacitor blocks for the whole feedback chain, which reduces component mismatch variation and enables layout re-use.

2 CIRCUIT DESIGN AND IMPLEMENTATION

The structure of the low pass biquadratic filter cell implemented in a fully-deferential Tow-Thomas configuration is shown in Fig. 1(a). The filter uses the same capacitor tuning bank for the entire structure. The capacitor bank, shown in Fig. 1(b), is used for coarse frequency tuning and is made of n capacitors connected in

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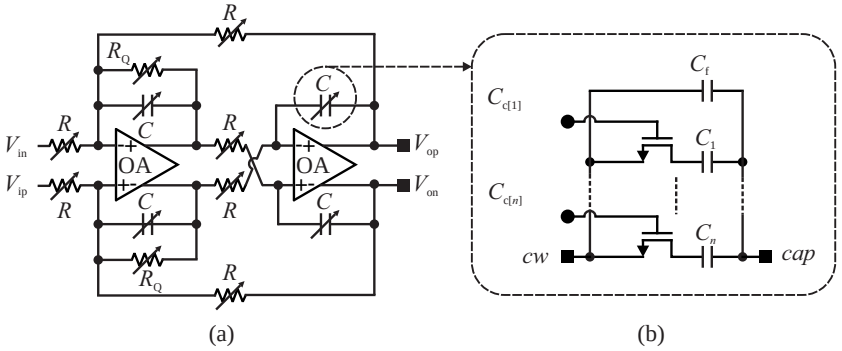

Fig. 1. (a) — structure of the filter, (b) — switched capacitor bank

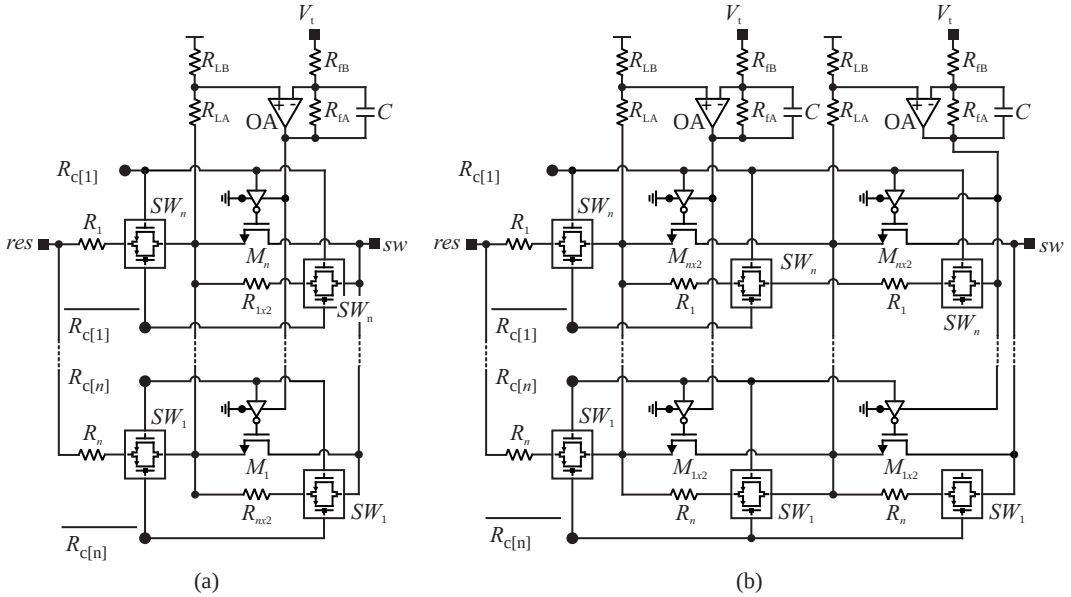

Fig. 2. The proposed tuning resistor bank: (a) — SAFB structure, (b) — DAFB structure

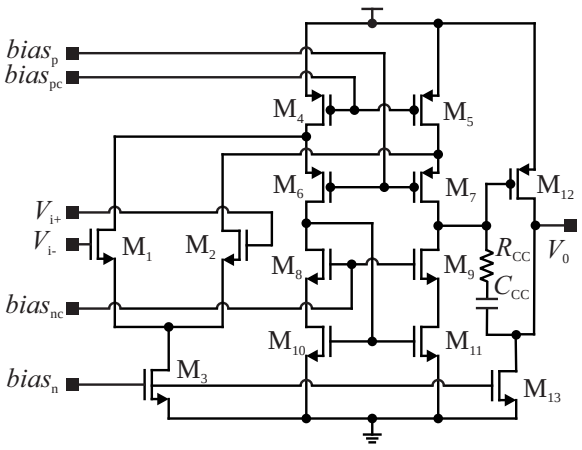

Fig. 3. Active feedback amplifier

parallel, which are controlled by n number of $C_{c[n]}$ control bits. The capacitors, with the exception of C_f, are made by multiplying the structure of C_1 and doubles with each bit. The two-staged Miller compensated operational amplifier (OA) uses a long-tailed pair as input and a push-pull output stage to achieve wide bandwidth and low power consumption [13].

The proposed continuous tuning structure is shown in Fig. 2(a). This structure uses a single active feedback element (SAFB). A further extension to this structure is shown in Fig. 2(b), where dual active feedback elements (DAFB) are used. One type of structure is used for both filter resistors R and RQ, but their fixed and continuous control signals are independent. The proposed continuous tuning structure is made of fixed resistors $R_1 - R_n$. The series-connected pair made of an accordingly scaled n-type MOSFET transistor together with a parallel connected fixed resistor acts as the continuous variable tuning element. DAFB structure MOSFET width is doubled and the parallel connected resistor value reduced by a factor of 2 for each branch, when comparing it to the SAFB structure. The resistors branches are controlled by a binary (BCD) to decimal converted digital control word, meaning only one branch can be active at a time. The high impedance resistors R_{LA} and R_{LB} are used to linearize the MOSFET.

Active feedback amplifier (OA), shown in Fig. 3, is used to extend the range of voltage control for the active tuning MOSFET. Furthermore, the use of such an active feedback configuration removes the need of increased supply voltage for MOSFET control, compared to only passive realization. It uses a high gain folded cascade structure, with an output stage used to drive the feedback resistors R_{fA} and R_{fB}. SAFB structure control voltage

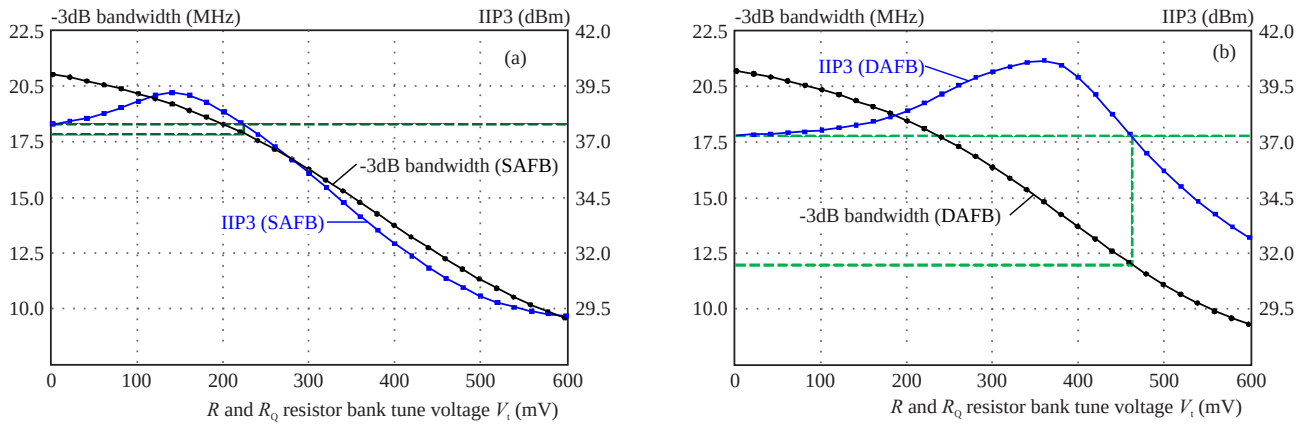

Fig. 4. Designed filter IIP3 and -3 dB bandwidth versus continuous control voltage: (a) — SAFB structure, (b) — DAFB structure

Table 1. Performance summary

Bandwidth (MHz)	10			100		
Filter response	Bessel	Butterworth	Chebyshev 1 dB ripple	Bessel	Butterworth	Chebyshev 1 dB ripple
In-band IP3 (dBm) [1]	37.5 [3]	35.8 [3]	35.0 [3]	-	-	-
	37.1 [4]	36.4 [4]	35.9 [4]	-	-	-
In-band IP3 (dBm) [2]	-	-	-	36.7 [3]	35.2 [3]	34.9 [3]
	-	-	-	36.7 [4]	35.4 [4]	35.1 [4]
Integrated input-reffered noise (μV) rms	123 [3]	115 [3]	111 [3]	290.0 [3]	267.0 [3]	263.0 [3]
	126 [4]	119 [4]	115 [4]	305.0 [4]	291.0 [4]	283.0 [4]
In-band SFDR (dB)	72.0 [3]	71.4 [3]	71.5 [3]	66.4 [3]	66.0 [3]	66.4 [3]
	71.5 [4]	71.6 [4]	71.9 [4]	66.2 [4]	65.6 [4]	66.2 [4]
Power (mW)	8.3			15		
Power of continuous tuning circuits(mW)	1.1 [3]					
	2.2 [4]					
Frequency range(MHz)	10-100					
Supply voltage (V)	1.2					
Technology (nm)	CMOS 65					

[1] $f_1 = 1$ MHz, $f_2 = 1.9$ MHz, input =1 V pp; [2] $f_1 = 10$ MHz, $f_2 = 19.0$ MHz, input = 1 V pp;
[3] SAFB structure; [4] DAFB structure; [5] Integrated from 1 to 10/100 MHz

V_0 can be calculated according to

$$V_0 = A_0(V_{i+} - V_{i-}) = \frac{R_{fB}V_{i+} + R_{fA}(V_{i+} - V_t)}{R_{fB} + \frac{R_{fB} + R_{fA}}{A_0}} \quad (1)$$

$$V_{i-} = V_t + \frac{R_{fB}}{R_{fA}} + R_{fB}(V_0 - V_t) \quad (2)$$

$$V_{i+} = \frac{V_s(R_n + R_{LA}) + R_{LB}V_r + R_n\frac{R_{LB}V_{sw} + R_{LA}V_s}{R_{0Mn}||R_{nx2}}}{R_n + R_{LA} + R_{LB} + R_n\frac{R_{LA} + R_{LB}}{R_{0Mn}||R_{nx2}}} \quad (3)$$

Here, A_0 is the open-loop gain of the active feedback amplifier; V_r and V_{sw} are common mode voltage levels at nodes res and sw respectively; R_n and R_{nx2} is the value of selected resistor, including the channel resistance of series-connected switch (SWn); R_{0Mn} is the channel resistance of the continuously tunable MOSFET, where the resistance for the region of linear operation can be calculated from (4), [14]. Control voltage for DAFB structure can be derived in the same manner as for the SAFB structure.

$$R_{0Mn} = \frac{L}{W\mu_n C_{0x}\left([V_{GS} - V_{th}] - \frac{V_{DS}}{2}\right)} \quad (4)$$

3 SIMULATION RESULTS

The filter was designed and simulated in 65 nm CMOS technology. The proposed design uses 5 fixed branches to

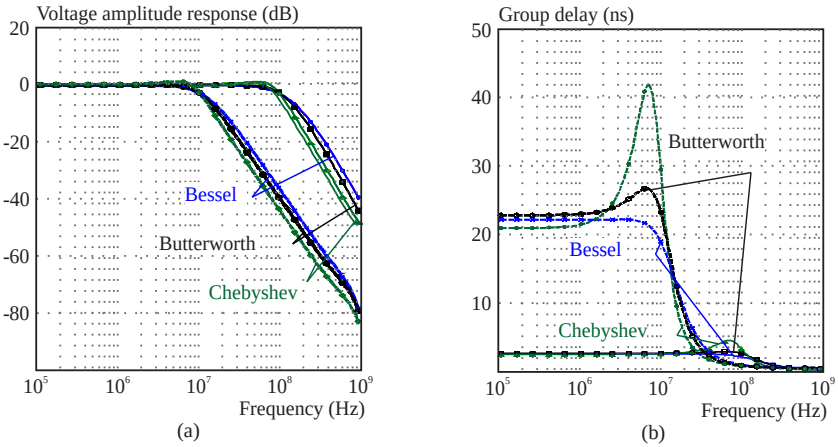

Fig. 5. Phase Noise simulation results at DCO and divide-by-2 outputs, when operating at highest operating frequency

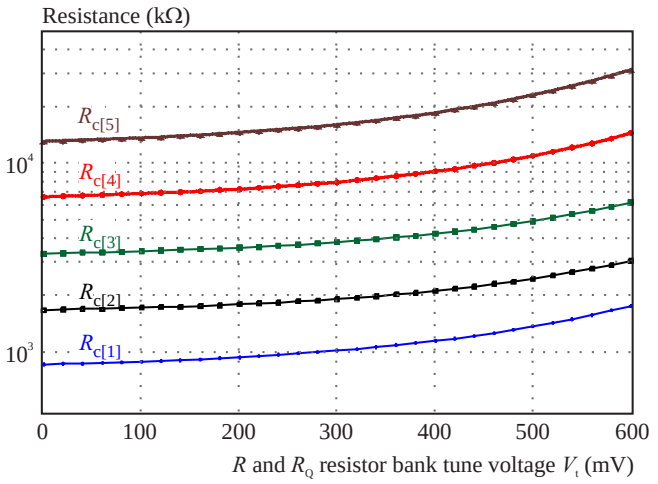

Fig. 6. R and RQ resistance versus the continuous control voltage

implement a resistor bank with a continuously variable resistance from 800 to 30 kΩ.It occupies an area of 0.16 mm^2 excluding supply and ground lines. A filter with a SAFB structure occupies and area of 0.14 mm^2.

Filter, designed with a SAFB and DAFB tuning structure, in-band IP3 performance over the tuned bandwidth is shown in Fig. 4 when a 1 V pp signal is applied to its input. Fore a SAFB tuning structure, the in-band IP3 performance is not affected when the bandwidth is continuously tuned by 15 %. When DAFB structure is used instead, the in-band IP3 performance is not affected for a 40 % of the continuous bandwidth tuning range.

Fig. 5 shows the voltage amplitude and group delay responses of the designed filter at 10 and 100 MHz. Using either SAFB or DAFB continuous tuning structures, the filter can be tuned to achieve Bessel, Butterworth and Chebyshev with 1 dB in-band ripple responses. Both SAFB and DAFB structures can be tuned to conditions shown in Fig. 5.

Figure 6 shows the graphs of resistor banks R and RQ resistance versus the continuous control voltage. The proposed design uses 5 fixed branches to implement a resistor bank with a continuously variable resistance from 800 to 30 kΩ. Table I gives the overall performance summary for the designed 2nd order low pass biquadratic filter with the proposed continuous tuning structure.

4 CONCLUSIONS

A new tuning structure of resistor bank for MOSFET-RC filters was proposed in this work. The structure was tested by designing a 2-nd order low pass biquadratic filter in 65 nm CMOS technology, with a layout size of 0.16 mm^2. Post layout simulations verify that designed filter bandwidth can be tuned from 10 to 100 MHz. By using the proposed continuous tuning structure, the designed filter response can be electronically reconfigured to meet a broad range of responses, ranging from Bessel to Chebyshev. Furthermore, the proposed tuning structure does not degrade in-band IP3 performance when the filter is continuously tuned up to 40 % of its bandwidth and can be used for multiple standard wireless solutions.

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