DESIGN OF GIGAHERTZ TUNING RANGE 5 GHz LC DIGITALLY CONTROLLED OSCILLATOR IN 0.18 μm CMOS

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In this paper design and simulation of a 4.3 – 5.4 GHz LC digitally controlled oscillator (LC DCO) in IBM 7RF 0.18 μm CMOS technology are presented. Wide gigahertz tuning range is achieved by using two LC DCOs, sharing same structure. DCO is made of one NMOS negative impedance transistor pair and LC tank, which consists of high quality inductor and two switched capacitor arrays for coarse and fine frequency tuning. Coarse and fine tuning switched capacitor arrays are controlled using 6-bit and 3-bit binary words. To increase available frequency values, frequency divider is used. Structure of frequency divider is based on extended-true-single-phase-clock flip-flops. Divider is made of eight divide-by-2 cells connected in daisy chain, thus division values from 2 to 256 are available. Wide tuning range and high division values allows using such DCO with frequency divider in multi-standart transceivers. Whole device is supplied from a single 1.8 V voltage source. At highest frequency proposed device draws 90 mA current including all buffers. Phase noise is −116.4 dBc/Hz at 1 MHz offset from 5.44 GHz carrier. Designed dual DCO and frequency divider occupies about 0.4 mm × 0.5 mm of chip space and whole chip, including pads, occupies 1.5 mm × 1.5 mm area of silicon.

K e y w o r d s: CMOS, integrated circuit, high frequency, digitally controlled oscillator, frequency divider, extended true-single-phase-clock

1 INTRODUCTION

Interest in design and implementation of advanced wireless communication systems is rapidly increasing. It can be seen from fast-growing coverage of high-speed mobile networks, such as UMTS, LTE, WiMAX. Also wireless networks, working at 5 GHz frequency (802.11n, 802.11ac), become common for home users. To support many different wireless standarts and services based on them, there is need for multi-band multi-standart RF transceivers.

One of the main requirement of such transceivers is relatively wide operating frequency range. This coincides with one of the challenges in high-speed integrated circuit design – wide range frequency synthesis. Usually phase locked loop (PLL) is used for frequency synthesis. There are two main types of phase locked loops: conventional (or charge-pump) PLL and all-digital PLL. In conventional PLL all blocks, except of phase-frequency detector, is analog. And as name states, all blocks forming all-digital PLL are digital. Former type of PLL is getting more attention in recent years, since it becomes harder to design analog blocks in advancing CMOS technologies, due to reduced supply voltage, increasing impact of leakage currents. Also, it is faster and easier to redesign all-digital PLL in different technology [1–4].

Digitally controlled oscillator (DCO) is significant block in the structure of all-digital PLL. There are two main types of DCO: LC tank based and ring DCO. Ring DCO occupies small chip area and there is an option to synthesize it using digital implementation tools [5]. LC tank based DCO occupies larger area of silicon because of large inductor sizes and are harder to simulate compared to ring DCOs. However, due to high-Q tank, LC DCOs can offer higher phase noise performance and thus are common choice for RF applications [2, 4].

Advantages of all-digital PLL can also be used in more mature and low-cost manufacturing technology, such as 0.18 μm CMOS. Although all-digital PLLs and DCOs, implemented in 90 nm – 0.18 μm CMOS technologies often suffer from relatively low frequency or narrow tuning range [6–11].

In this paper we propose wide 1.1 GHz tuning range, high frequency 4.3–5.4 GHz LC tank based digitally controlled oscillator, suitable for applications in multi-standart transceivers, implemented in low-cost IBM 7RF 0.18 μm CMOS technology.

2 STRUCTURE OF LC DCO WITH FREQUENCY DIVIDER

The simplified block diagram of proposed fully integrated oscillator and frequency divider is presented in Fig. 1. It consists from two LC tank based DCOs, decoupling stage, differential to single ended converter, tri-state buffers and frequency divider.

2.1 Core of the DCO

Proposed structure can be scalable to use multiple DCOs to fulfil requirements of operating frequency and tuning range. However, used area of silicon is growing rapidly by adding more DCOs. In our design two DCOs are enough to cover gigahertz tuning range. Schematic

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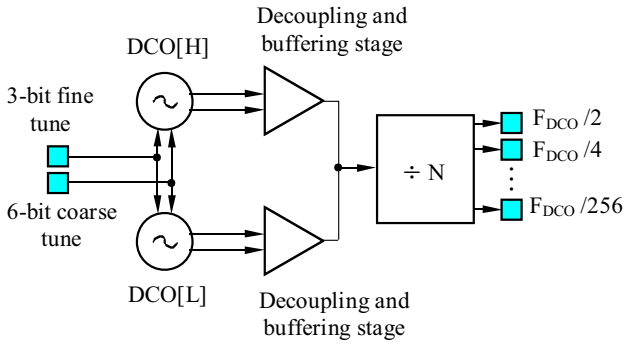
Fig. 1. Simplified block diagram of proposed oscillator with frequency divider. DCO[H] — high frequency DCO, DCO[L] — low frequency DCO, ÷N — frequency divider

of the core of DCO is shown in Fig. 2. Both LC DCOs share same architecture and are based on the structure of conventional LC tank based controlled oscillator. Main components of the DCO are high quality factor inductor, two (coarse and fine) switched-capacitor arrays and cross-coupled transistor pair, which generates negative impedance for energy loss in LC tank. Main difference between two DCO's is inductor size.

Oscillation frequency is tuned using 6-bit and 3-bit binary words. 6-bit word switches value of coarse tuning capacitor array and 3-bit word switches value of fine tuning capacitor array. As it is seen, from the conventional voltage controlled oscillator digitally controlled oscillator differs in fine tuning circuit — it does not have analog varactors. Frequency range is not continuous because of digital control. Frequency tuning step is defined by lowest capacitor value in fine tuning array. Capacitance of NMOS transistors was used in tuning arrays.

The following design guidelines can be used to optimize tuning range of the LC DCO using Cadence software:

– Choose high quality inductor, provided with your process design kit and suitable for aimed operating frequency;

– Choose smallest capacitor for lowest fine frequency tuning step;

– Choose capacitor for coarse frequency tuning step. It should be at least several times larger, than smallest fine tuning capacitor. Populate coarse tuning array by doubling capacitor count for each bit, if binary control is used;

– Run simulation and check highest operating frequency with all capacitors being turned off. Frequency should be higher, than aimed frequency. If frequency is too low, reduce coarse tuning capacitor size (or bit count) or reduce tank inductance;

– Populate fine tuning capacitor array by doubling count of smallest capacitor for each bit. Bit count should be sufficient for fine tuning frequency range to cover one step of coarse tuning;

– Add more capacitors to coarse frequency tuning bank, to expand tuning range towards lower frequencies;

– Check highest (all capacitors turned off) and lowest (all capacitors turned on) frequencies of DCO. If highest frequency is not reducing rapidly, more capacitors to coarse tuning array can be added and required frequency can be restored by changing inductor size. If added capacitors are greatly reducing high frequency, return to previous capacitor size (or bit count);

– To further increase tuning range, create second DCO with larger inductance and repeat all steps above;

– Output frequencies of low and high frequency DCOs should overlap, to avoid frequency gap after manufacturing.
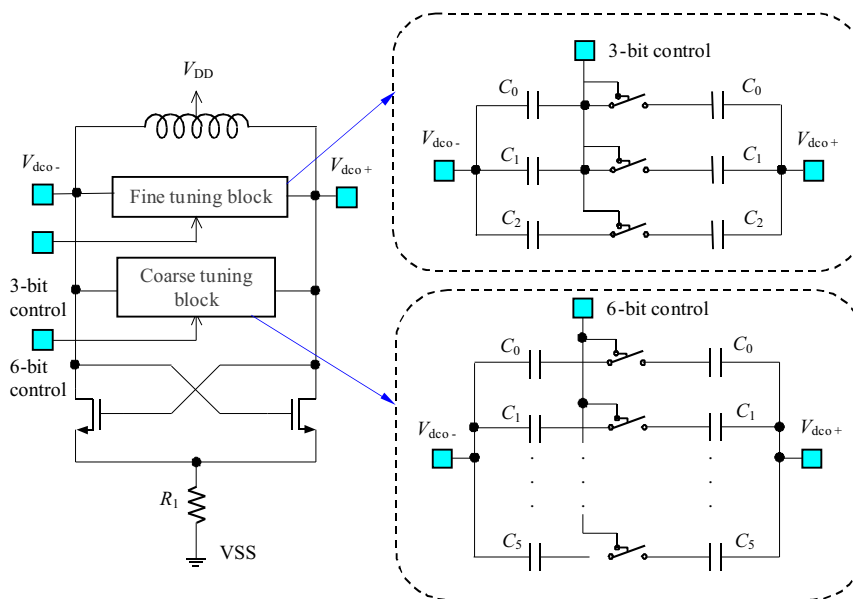

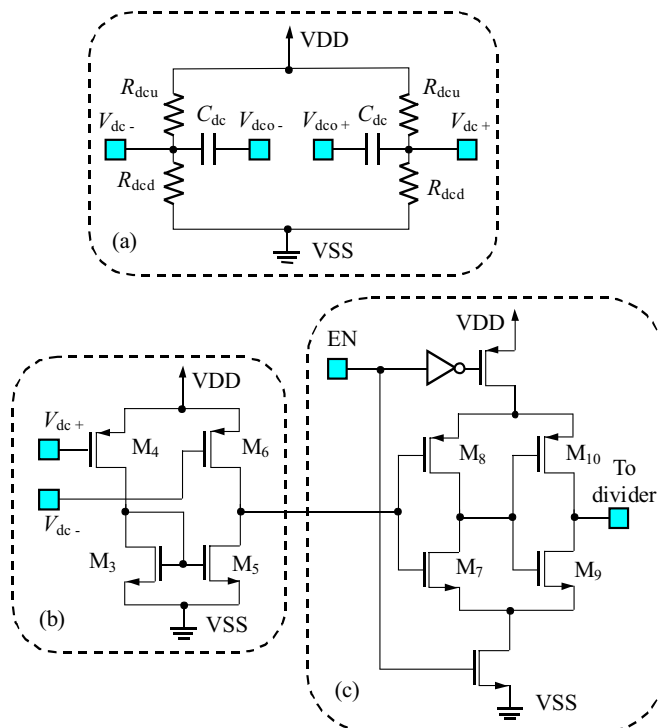**Fig. 2.** Schematic of core of the DCO

Fig. 3. Schematics of DC decoupling stage (a), differential to single ended converter (b), and tri-state buffer stage (c)
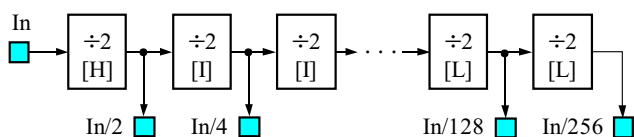

Fig. 4. Structure of divide-by-N frequency divider. $\div 2$ [H] — divider working at highest frequency, $\div 2$ [I] — divider working at intermediate frequency, $\div 2$ [L] — divider working at low frequency. In — input signal, In/N — input signal divided by coefficient N, where $N = 2^1 - 2^8$

2.2 DC decoupling stage

The voltage swing at output nodes of designed LC DCO can reach twice of supply voltage. To make DCO compatible with other circuits, DC decoupling stage is needed, which is shown in Fig. 3 (a). It is made of decoupling capacitor C_{dc} and resistors R_{dcu} and R_{dcd}, which sets DC voltage at the output of DCO. The value of C_{dc} is 1.6 pF and the values of R_{dcu} and R_{dcd} are 15 kΩ each. These values set DC voltage at about 0.9 V *ie* half of the supply voltage.

2.3 Differential to single ended converter

In proposed architecture, frequency divider is based on ETSPC flip-flops. They are single ended devices. Thus differential to single ended converter, shown in Fig. 3 (b), is used. Such converter loads equally both output nodes of LC DCO and outputs single ended rail-to-rail signal, suitable as input for ETSPC frequency divider.

2.4 Tri-state buffer

Tri-state buffers are used to isolate signal path to powered-down DCO and allow only one DCO to interface with frequency divider. Tri-state buffer is made from two inverters with connected power supply and ground isolating PMOS and NMOS transistors, as shown in Fig. 3 (c). Additional control inverter is added to control both transistors using single 1-bit signal.

2.5 Frequency divider

Frequency divider is used to increase variety of available frequencies and for clock distribution, what increase range of applications of proposed device.

Main block of frequency divider is flip-flop. To achieve multi gigahertz operating frequency, flip-flop topologies, such as Wang's, Razavi's or CML are often choice. But technology scaling allows using true-single-phase-clock (TSPC) and extended TSPC (ETPSC) dividers for specified purpose. These topologies stand out with relatively simple structure and low power consumption. These flip-flops were thoroughly analysed in [12] and also was used in our previous work [13].

The proposed structure of frequency divider is shown in Fig. 4. It is ETSPC flip-flop based frequency divider, made of eight divide-by-2 dividers, connected in a daisy chain fashion. Division rates are ranging from 2^1 to 2^8. These rates allow using proposed device for wide range (high and low speed) of on-chip digital circuit clocking.

Advantage of connecting dividers in daisy-chain is that each divider stage relaxes requirements for next divider since it is reducing input frequency by half. We are using
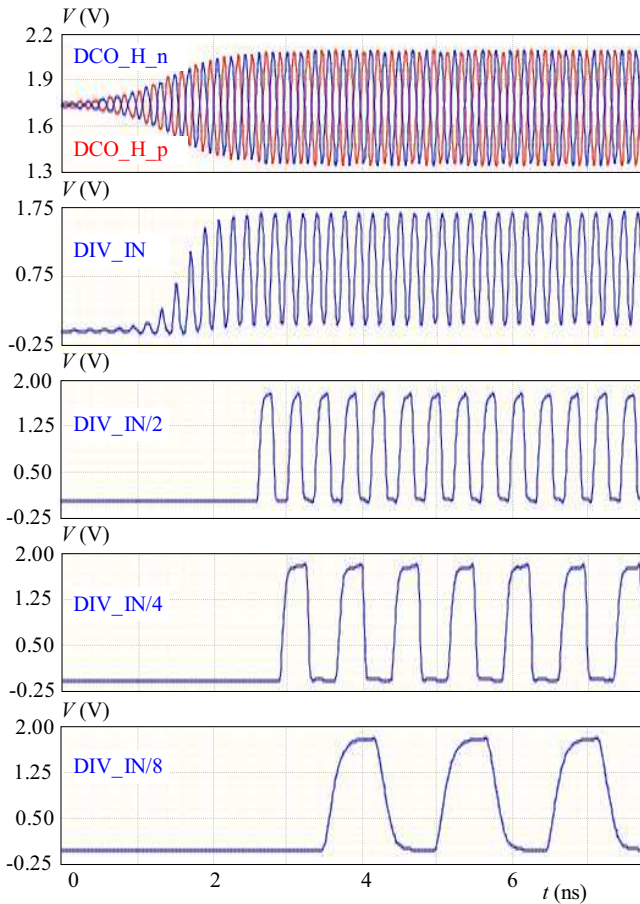
Fig. 5. Transient simulation results at highest operating frequency. DCO_H_p, DCO_H_n — output signals of designed high frequency DCO; DIV_IN — decoupled and converted to single-ended signal; DIV_IN/2, DIV_IN/4 and DIV_IN/8 — respectively divide-by-2, divide-by-4 and divide-by-8 divider's outputs

Fig. 6. Transient simulation results at lowest operating frequency. DCO_L_p, DCO_L_n — output signals of designed low frequency DCO; DIV_IN — decoupled and converted to single-ended signal; DIV_IN/2, DIV_IN/4 and DIV_IN/8 — respectively divide-by-2, divide-by-4 and divide-by-8 divider outputs
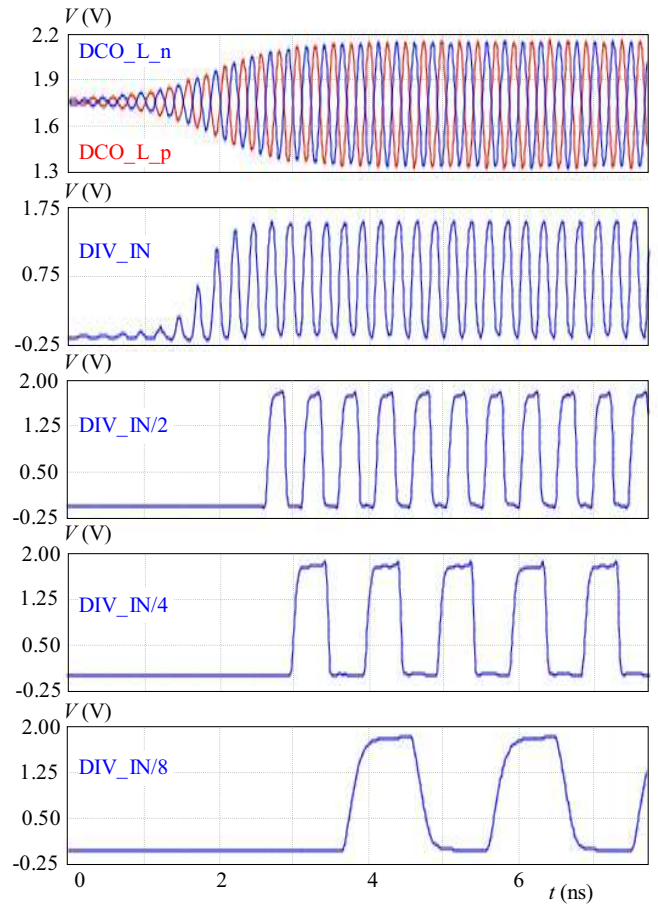
Table 1. Summary of performance for the DCO with frequency divider

Characteristics		Value
Technology		IBM 7RF 0.18 μm CMOS
Supply Voltage		1.8 V
Operating Current	DCO core	10 mA
	Whole chip	90 mA
DCO's Tuning Range		4.3 GHz – 5.44 GHz
Phase Noise at 1 MHz offset from carrier	5.44 GHz	−116.4 dBc/Hz
	2.72 GHz	−122.5 dBc/Hz
	4.30 GHz	−117.6 dBc/Hz
	2.15 GHz	−123.7 dBc/Hz
Area	Active area	0.4 mm × 0.5 mm
	Whole chip	1.5 mm × 1.5 mm

3 types of division cells. One cell (Fig. 4, ÷2[H]) is operating at frequency of DCO (4.3 GHz – 5.4 GHz), five cells are optimised for operation at frequencies from 2.7 GHz to 134 MHz (Fig. 4, ÷2[I]) and two cells are working at lowest frequencies (Fig. 4, ÷2[L]) from 84 MHz to 33 MHz. Such structure allows to achieve needed operating frequency, lower used chip area and power consump-

tion. Also it allows reusing same divide-by-2 cells, what minimizes design time.

3 SIMULATION RESULTS

Proposed DCO and frequency divider were designed in IBM 7RF 0.18 μm CMOS technology and was simu-
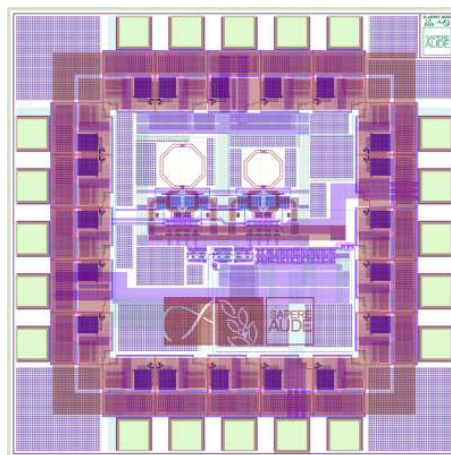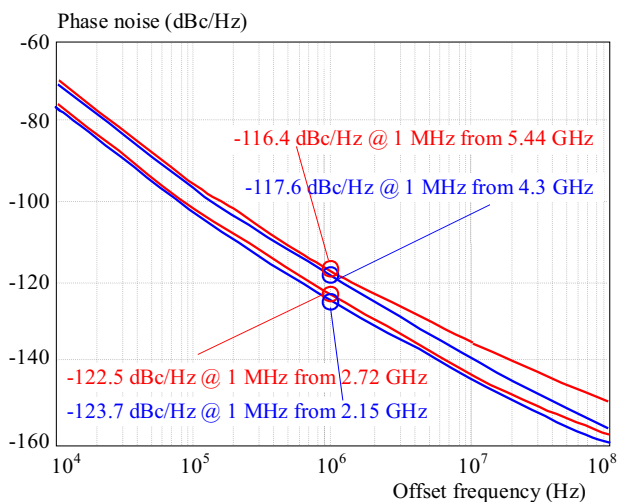
Fig. 7. Phase Noise simulation results at DCO and divide-by-2 outputs, when operating at highest operating frequency

Fig. 8. Layout of designed LC DCO and ETSPC frequency divider

Table 2. Comparison with other published DCO designs

Characteristics	This Work	[6]	[7]	[8]	[9]*	[10]*	[11]*
CMOS Technology	$0.18\,\mu$m	$0.13\,\mu$m	$0.13\,\mu$m	$90\,$nm	$0.13\,\mu$m	$0.13\,\mu$m	$0.18\,\mu$m
Supply Voltage, V	1.8	0.5	2.5	1.2	1.2	1.2	1.8
Operating Current, mA	10	0.372	3.2	2	10	12.7	6.33
Minimum Frequency, GHz	4.3	1.63	3.45	3.05	1.7	1.99	0.004
Maximum Frequency, GHz	5.44	1.77	4.45	3.65	3.1	2.5	0.416
Carrier frequency, GHz	5.44	1.7	4	3.35	2.4	2.185	0.416
Phase Noise at 1 MHz offset from carrier, dBc/Hz	-116.4	-109	-114	-118	-120.5	-107	N/A
Area, mm^2	0.2	4	0.19	N/A	0.8	0.43	0.2

* Data in reference is provided only for whole PLL

lated using Cadence software. All results provided in this section are from post-layout simulations.

Single 1.8 V voltage supply was used for the whole chip. Each DCO draws about 10 mA current, frequency divider uses about 27 mA, DC decoupling stage, buffers and other chip circuitry draws about 53 mA current. Total chip current is about 90 mA.

Figure 5 shows transient simulation results at highest operating frequency, equal to 5.44 GHz: waveforms of designed high frequency DCO (DCO_H_p, DCO_H_n), decoupled and converted to single-ended signal (which also is divider input signal - DIV_IN) and three divider outputs (divide-by-2 signal DIV_IN/2, divide-by-4 signal DIV_IN/4 and divide-by-8 signal DIV_IN/8). It can be seen from these waveforms, that DCO's output signal swings from about 1.37 V to 2.13 V, decoupled, converted to single ended and divider's output signals are rail-to-rail. Startup time of high frequency DCO is about 2 ns.

Highest frequency is set when coarse tuning control word is set to 63, fine tuning control word is set to 7.

Figure 6 shows transient simulation results at lowest operating frequency, equal to 4.3 GHz. It can be seen from these waveforms, that DCO's output signal swings

from about 1.41 V to 2.12 V, decoupled, converted to single ended and divider's output signals are rail-to-rail. Start-up time of low frequency DCO is about 3 ns.

Lowest frequency is set when both coarse tuning and fine tuning control words are set to 0.

Phase noise at designed DCO outputs and at divide-by-2 output of frequency divider, when operating at lowest and highest frequencies, is shown in Fig. 7. It is seen, when highest operating frequency is set, phase noise at output of DCO is -116.4 dBc/Hz at 1 MHz offset from 5.44 GHz carrier and phase noise at divide-by-2 divider's output is -122.5 dBc/Hz at 1 MHz frequency offset from 2.72 GHz carrier. While working at lowest frequency, phase noise at output of DCO is -117.6 dBc/Hz at 1 MHz offset from 4.3 GHz carrier and phase noise at divide-by-2 divider's output is -123.7 dBc/Hz at 1 MHz frequency offset from 2.15 GHz carrier.

Summary of performance for designed DCO and frequency divider is shown in Tab. 1.

Comparison to other DCOs, designed in more mature ($90\,$nm – $0.18\,\mu$m CMOS) technologies, is provided in Tab. 2.

As we can see from the Tab. 2, proposed DCO achieves higher operating frequency of 5.44 GHz and wide tuning range, equal to 1.14 GHz, compared to the similar devices implemented in similar technologies.

4 LAYOUT

Layout of the designed LC DCO and ETSPC frequency divider is presented in Fig. 8. The whole chip, including pads, occupies $1.5\,\mathrm{mm} \times 1.5\,\mathrm{mm}$ area of silicon. Two DCOs with DC decoupling stage and tri-state buffers occupy $500\,\mu\mathrm{m} \times 340\,\mu\mathrm{m}$ area of silicon and frequency divider takes $55\,\mu\mathrm{m} \times 270\,\mu\mathrm{m}$ of chip space.

5 CONCLUSIONS

Wide tuning range, high frequency 5 GHz LC tank based digitally controlled oscillator, suitable for applications in multi-standart transceivers was implemented in low-cost IBM 7RF $0.18\,\mu\mathrm{m}$ CMOS technology. The structure of proposed device consists of two (high and low frequency) DCOs, decoupling stage, differential to single-ended converter, tri-state buffer and frequency divider. Frequency of DCO is tuned by using 6-bit coarse tuning ant 3-bit fine tuning binary words. Tuning range of the DCO is 4.3– 5.4 GHz. Frequency divider was implemented to increase variety of available frequencies and applications. It is based on ETSPC flip-flops. Divide values from 2 to 256 are available. Supply voltage for designed device is 1.8 V. Phase noise at output of DCO is -116.4 dBc/Hz at 1 MHz offset frequency from 5.44 GHz carrier and phase noise at divide-by-2 divider output is -122.5 dBc/Hz at 1 MHz offset frequency from 2.72 GHz carrier.

References

[1] STASZEWSKI, R. B.—HUNG, C.—BARTON, N.—LEE, M.—LEIPOLD, D.: A Digitally Controlled Oscillator in a 90 nm Digital CMOS Process for Mobile Phones, IEEE J. Solid-State Circuits **40** No. 11 (2005), 2203–2211.

[2] LU, P.—SJÖLAND, H.: A 5 GHz 90 nm CMOS All Digital Phase-Locked Loop, Analog Integrated Circuits and Signal Processing **66** No. 1 (2010), 49–59.

[3] HSU, C.—STRAAYER, M.—PERROTT, M.: A Low-Noise Wide-BW 3.6 GHz Digital $\Delta\Sigma$ Fractional-N Frequency Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation, IEEE J. Solid-State Circuits **43** No. 12 (2008), 2776–2786.

[4] TEMPORITI, E.—WELTIN-WU, C.—BALDI, D.—TONIETTO, R.—SVELTO, F.: A 3 GHz Fractional All-Digital PLL with a 1.8 MHz Bandwidth Implementing Spur Reduction Techniques, IEEE J. Solid-State Circuits **44** No. 3 (2009), 824–834.

[5] LIU, Y.—CHEN, W.—CHOU, M.—TSAI, T.—LEE, Y.—YUAN, M.: A 0.1–3 GHz Cell-Based Fractional-N All Digital Phase-Locked Loop using $\Delta\Sigma$ Noise-Shaped Phase Detector, Proceedings of the IEEE 2013 Custom Integrated Circuits Conference, 2013.

[6] PLETCHER, N.—RABAEY, J.: A $100\,\mu\mathrm{W}$, 1.9 GHz Oscillator with Fully Digital Frequency Tuning, Proceedings of the 31st European Solid-State Circuits Conference, 2005, pp. 387–390.

[7] PITTORINO, T.—CHEN, Y.—NEUBAUER, V.—MAYER, T.—MAURER, L.: A UMTS-Complaint Fully Digitally Controlled Oscillator with 100 Mhz Fine-Tuning Range in $0.13\,\mu\mathrm{m}$ CMOS, 2006 IEEE International Solid State Circuits Conference – Digest of Technical Papers, 2006, pp. 770–779.

[8] ZHUANG, J.—DU, Q.—KWASNIEWSKI, T.: A 3.3 GHz LC-Based Digitally Controlled Oscillator with 5 kHz frequency resolution, 2007 IEEE Asian Solid-State Circuits Conference, 2007, pp. 428–431.

[9] PU, Y.—PARK, A.—PARK, J. S.—LEE, K. Y.: Low-Power, All Digital Phase-Locked Loop with a Wide-Range, High Resolution TDC', ETRI J, **33** No. 3 (2011), 366–373.

[10] SAMARAH, A.—CARUSONE, A.: A Digital Phase-Locked Loop With Calibrated Coarse and Stochastic Fine TDC, IEEE J. Solid-State Circuits **48** No. 8 (2013), 1829–1841.

[11] CHEN, X.—YANG, J.—SHI, L.: A Fast Locking All-Digital Phase-Locked Loop via Feed-Forward Compensation Technique, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, **19** No. 5 (2011), 857–868.

[12] DENG, Z.—NIKNEJAD, A. M.: The Speed-Power Trade-Off in the Design of CMOS True-Single-Phase-Clock Divider, IEEE Journal of Solid-State Circuits **45** No. 11 (2010), 2457–2465.

[13] JURGO, M.—KIELA, K.—NAVICKAS, R.: Design of Low Noise 10 GHz divide by 16 ... 511 Frequency Divider, Electronics and Electrical Engineering **19** No. 6 (2013).

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