FPGA Implementation of a BPSK Modulator with Frequency Hopping

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Abstract

PSK modulations are very widespread in communication due to their robustness to the noise. In order to avoid interference or for anti-jamming purposes, frequency hopping may be applied. In this work we present an FPGA implementation of a BPSK modulator based on frequency hopping. The results shows good performance, more than 300 MHz of clock system, low area occupation and low power dissipation (about 100 mW).

Keywords

Frequency Hopping, DDS, BPSK, FPGA, Spread Spectrum, Anti-jamming

1. Introduction

Phase-Shift Keying (PSK) modulations are the best known and most used numerical modulations in the field of communications. The information is encoded in the carrier phase which assumes discrete values as a function of the bits or sequence of bits to be transmitted. The signal amplitude and frequency remain constant. Since the information is coded in the phase, this type of modulation has an excellent robustness towards amplitude errors of the received symbols [1, 2]. In modern applications there was the necessity to strengthen the communication protocols mostly for avoiding interference both voluntary (such as the case of jammers, very used in electronic warfare [3]) and involuntary (such as the transmission of several devices on the same frequency [4]). One of the most used technique useful to avoid these issues is the Spread Spectrum [5]. The Spread Spectrum was initially developed in the military field to avoid radio interceptions. Originally, any type of transmission that guaranteed a non-stationary spectrum was considered a spread spectrum. With the introduction of the Code Division Multiple Access (CDMA) [6], the spread spectrum is generated by multiplying the information by a code. Spread Spectrum can be also generated by using the frequency hopping technique, the so called Frequency-Hopping Spread Spectrum (FHSS) [7]. As for CDMA, FHSS is a transmission technique used to increase the bandwidth of a signal. It consists in varying the transmission frequency at regular intervals in a pseudo-random way through a pre-established code. Several modern applications make use of Frequency Hopping to avoid interference, among them, the most known is the Bluetooth technology [8]. If several terminals transmit on the same carrier, collisions are created. By applying Frequency Hopping according to a certain law, this problem is avoided. Obviously only those who transmit and receive know the sequence of frequency jumps and where there should be interference in a given instant, it will be of short duration because at the next instant, the frequencies will most likely be different. With the diffusion of the IoT, secure communications will be always more required. Sensible data, locally processed by smart nodes equipped with machine learning algorithms[9] (that nowadays find application in always more fields [10],[11],[12],[13],[14],[15],[16] must be transmitted over the internet in the safest way possible In such a context, FPGAs can be a powerful and valuable ally for the de-centralization of computing as for example in [17].

The paper is structured as follows: Section 2 gives a brief introduction on PSK modulation, Section 2.1 gives some info about frequency hopping and its implementation by using Digital Direct Synthesis, in Section 3 simulation and implementation results are shown, end, finally, in Section 4 some conclusion are discussed.

2. PSK Modulation

There are several types of PSK modulation. Among the most used are:

- Binary phase-shift keying (BPSK): it associates the two binary digits 1 and 0 with two different carrier phase values, such as 0° and 180°.
- Quadrature phase-shift keying (QPSK): in this case we have 4 equally spaced phases to represent

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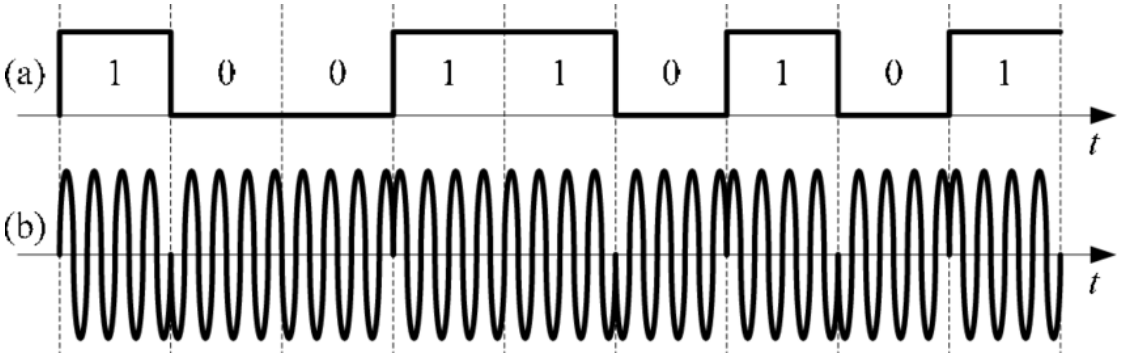

Figure 1: Time behavior of a BPSK modulation

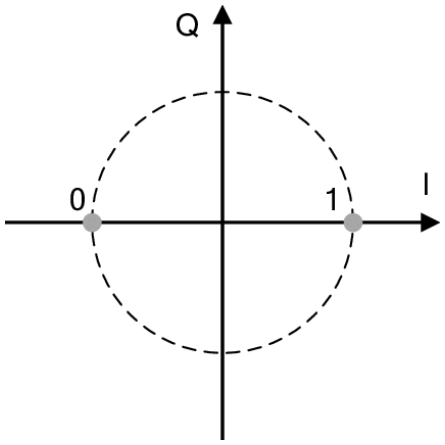

Figure 2: BPSK constellation

2 bits.

- 8-PSK: similar to QPSK, but it uses 8 phases to represent 3 bit.

In [7] the authors present a frequency hopping system based on Frequency Shift Key (FSK), in this work, we focused our attention on PSK modulation. In detail, we implemented a BPSK modulatior but the developed system is suitable for any PSK modulation. Fig.2 depicts the time behavior of a BPSK modulation. The carrier phase (b) changes at varying of binary signal (a).

In Fig.2, is instead shown the constellation of a BPSK.

2.1. Frequency Hopping with Digital Direct Synthesis (DDS)

The aim of a frequency-hopping-based system is to jump to different frequencies. An example is depicted in Fig.2.1, where are shown all 79 frequencies where a device Bluetooth may work.

An easy way to generate the carrier is the use of a Digital Direct Synthesizer [18] based on a 2^N locations memory where the samples for the wave generation are stored. The binary information, i.e. the shift phase, is given by adding an offset to the read-address. Offset 0 means 0° phase (bit 0), offset 2^{N-1} means 180° phase (bit 1). A simplified scheme of our system is depicted in Fig.2.1.

In our experiments the number of bit N for the address has been set to 10, as consequence the number of memory locations is 1024. Also the number of bit of each memory word is N=10 bit, but in general these two parameter can be different. The tuning word is the input used to set the carrier frequency following the law:

$$F_{out} = \frac{N \cdot F_{clk}}{2^N} \tag{1}$$

The input SEL is used to generate the binary information: SEL=0 → bit 0, SEL=1 → bit 1.

3. System simulation and FPGA Implementation

Before the implementation, the system has been simulated first in floating point and then in fixed point by using Simulink. After the system simulation the system has been coded in VHDL and implemented in a Xilinx Zynq 7020 FPGA. Fig.3 shows the exact correspondence between the simulink simulation and the Xilinx Vivado.

The Fig.3 shows the positive timing closure of the system with a clock period of 3 ns corresponding to 333 MHz.

About the power consumption, we did first an estimation without considering the switching activity of the circuit nodes (see Fig.3), and then we repeated the same estimation by using the value of switching activity provided by the simulation (see Fig.3). In the latter case, the value depends on the input test vectors.

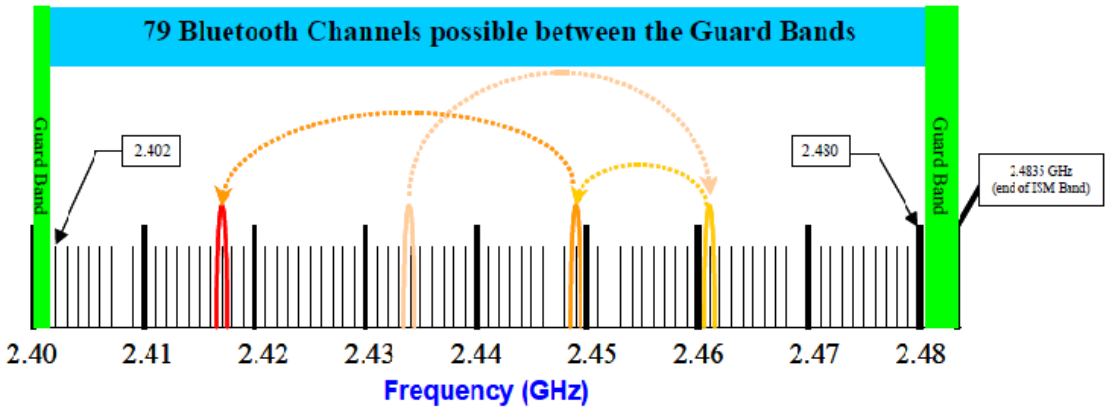

Figure 3: Channel frequencies in Bluetooth communication

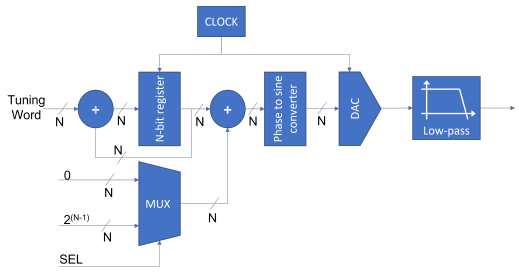

Figure 4: Developed System

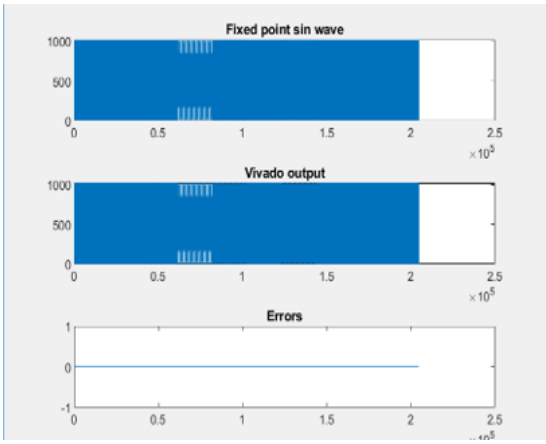

Figure 5: Correspondence between Simulink and Vivado simulations

In both cases the estimated power is similar and is 147 mW for vectorless estimation and 120 mW for vector-based estimation.

The last aspect of the system implementation is the resources utilization on FPGA. The synthesis results are shown in Fig.3

As can be seen, the resource utilization is very low. By increasing the value of N, the resource utilization will increase linearly with the exception of the memory used to store the wave samples that will increase exponentially.

4. Conclusion

We propose the FPGA implementation of a BPSK modulator based on frequency hopping. The system can be used both for anti-jamming applications or to avoid collision when two devices transmit on the same carrier. The system has been tested with a clock frequency of 333 MHz on a Xilinx Zynq 7020 device. The system makes use of a very limited number of hardware resources with a power dissipation of 120 mW.

Acknowledgments

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Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0,426 ns	Worst Hold Slack (WHS):	0,079 ns	Worst Pulse Width Slack (WPWS):	0,407 ns
Total Negative Slack (TNS):	0,000 ns	Total Hold Slack (THS):	0,000 ns	Total Pulse Width Negative Slack (TPWS):	0,000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	31	Total Number of Endpoints:	31	Total Number of Endpoints:	36

All user specified timing constraints are met.

Figure 6: System time closure results

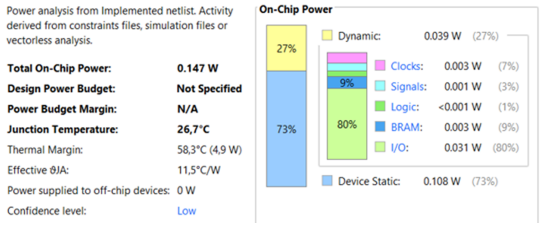


Figure 7: Vectorless power estimation

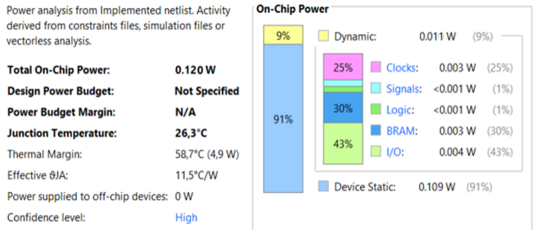
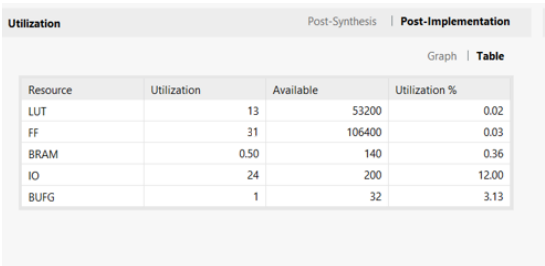


Figure 8: Power estimation by considering the switching activity



Resource	Utilization	Available	Utilization %
LUT	13	53200	0.02
FF	31	106400	0.03
BRAM	0.50	140	0.36
IO	24	200	12.00
BUFG	1	32	3.13

Figure 9: Resource utilization

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