Electrical Specifications

All pinout tables in this section are written from the Processor point of view when referencing signal directions.				
Signal Group	**Signal**	**I/O**	**Description**	**Voltage**
Power	3.3V	I	3.3 V source	3.3V
	GND		Return current path	0 V
	USB_VIN	I	USB VIN compliant to the USB 2.0 Specification. Connect to any pins on processor that require 5V for USB functionality.	4.8-5.2V
	RTC_3V_BATT	I	3V provided by external coin cell or mini battery. Max draw = 100uA. Connect to pins that maintain an RTC during power loss. Can be left NC.	3V
	3.3V_EN	O	Controls the carrier board's main voltage regulator. Voltages above 1V will enable 3.3V power path. Can be left NC. If implemented, carrier board must supply pullup resistor and 3.3V clamping on regulator enable pin.	3.3V
	BATT_VIN/3	I	Carrier board raw voltage over 3. 1/3 resistor divider is implemented on carrier board. Amplify the analog signal as needed to enable full 0-3.3V range.	3.3V
Reset	Reset	I	Input to processor. Open drain with pull up on processor board. Pulling low resets processor.	3.3V
	Boot	I	Input to processor. Open drain with pull up on processor board. Pulling low puts processor into special boot mode. Can be left NC.	3.3V
USB	USB_D+, USB_D-	I/O	USB Data ± Differential serial data interface compliant to the USB 2.0 Specification. If a UART is required for programming, USB+/- must be routed to a USB-to-serial conversion IC on the processor board.	
USBHOST	USBHOST_D+, USBHOST_D-	I/O	For processors that support USB Host Mode. USB Data ± Differential serial data interface compliant to the USB 2.0 Specification. Can be left NC.	
CAN	CAN_RX	I	CAN Bus Receive Data	3.3V
	CAN_TX	O	CAN Bus Transmit Data	3.3V
UART	UART_RX1	I	UART Receive Data	3.3V
	UART_TX1	O	UART Transmit Data	3.3V
	UART RTS1	O	UART Ready To Send	3.3V
	UART CTS1	I	UART Clear To Send	3.3V
	UART_RX2	I	2nd UART Receive Data	3.3V
	UART_TX2	O	2nd UART Transmit Data	3.3V
	Note: UART1/2 must be unencumbered (not attached to a USB-to-serial conversion IC).			
	Note: UART0 is not shown. Primary debug serial is done over USB. Serial.print() should print over USB, not TX1.			
I2C	I2C_SCL	I/O	I2C clock. Open drain with pull up on carrier board.	3.3V
	I2C_SDA	I/O	I2C data. Open drain with pull up on carrier board.	3.3V

	I2C_INT#	I	Interupt notification from carrier board to processor. Open drain with pull up on carrier board. Active Low.	3.3V
	I2C_SCL1	I/O	2nd I2C clock. Open drain with pull up on carrier board.	3.3V
	I2C_SDA1	I/O	2nd I2C data. Open drain with pull up on carrier board.	3.3V
SPI / SDIO	SPI_COPI	O	SPI Controller Output Peripheral Input	3.3V
	SPI_CIPO	I	SPI Controller Input Peripheral Output	3.3V
	SPI_SCK	O	SPI Clock.	3.3V
	SPI_CS#	O	SPI Chip Select. Active low. Can be routed to GPIO if hardware CS is not used.	3.3V
	SPI_SCK1/SDIO_CLK	O	2nd SPI Clock. Secondary use: SDIO Clock.	3.3V
	SPI_COPI1/SDIO_CMD	I/O	2nd SPI Controller Output Peripheral Input. Secondary use: SDIO Command Interface.	3.3V
	SPI_CIPO1/SDIO_DATA0	I/O	2nd SPI Controller Input Peripheral Output. Secondary use: SDIO data exchange bit 0.	3.3V
	SDIO_DATA1	I/O	SDIO data exchange bit 1.	3.3V
	SDIO_DATA2	I/O	SDIO data exchange bit 2.	3.3V
	SPI_CS1/SDIO_DATA3	I/O	2nd SPI Chip Select. Active low. Secondary use: SDIO data exchange bit 3.	3.3V
AUDIO	AUD_MCLK	O	Audio master clock	3.3V
	AUD_OUT/PCM_OUT/ I2S_OUT/CAM_MCLK	O	Audio data output. PCM synchronous data OUTput. I2S Serial Data OUT. Camera master clock.	3.3V
	AUD_IN/PCM_IN/ I2S_IN/CAM_PCLK	I	Audio data input. PCM synchronous data INput/ I2S Serial Data IN. Camera peripheral clock.	3.3V
	AUD_LRCLK/PCM_SYNC/ I2S_WS/PDM_DATA	I/O	Audio left/right clock. PCM synchronous data SYNC. I2S Word Select. PDM Data.	3.3V
	AUD_BCLK/PCM_CLK/ I2S_SCK/PDM_CLK	O	Audio bit clock. PCM Clock. I2S Continuous Serial Clock. PDM Clock.	3.3V
SWD	SWDIO	I/O	Serial Wire Debug I/O. Connect if processor supports SWD. Can be left NC.	3.3V
	SWDCK	I	Serial Wire Debug Clock. Connect if processor supports SWD. Can be left NC.	3.3V
ADC	A0	I	Analog to digital converter 0. Amplify the analog signal as needed to enable full 0-3.3V range.	3.3V
	A1	I	Analog to digital converter 1. Amplify the analog signal as needed to enable full 0-3.3V range.	3.3V
PWM	PWM0	O	Pulse width modulated output 0.	3.3V
	PWM1	O	Pulse width modulated output 1.	3.3V
Digital	D0	I/O	General digital input/output pin.	3.3V
	D1/CAM_TRIG	I/O	General digital input/output pin. Camera trigger.	3.3V
General/Bus	G0/BUS0	I/O	General purpose pins. Any unused processor pins should be assigned to Gx with ADC + PWM capable pins given priority (0, 1, 2, etc) positions. The intent is to	3.3V

	G1/BUS1	I/O	ADC + PWM capable pins given priority (0, 1, 2, etc) positions. The intent is to guarantee PWM, ADC, and Digital Pin functionality on ADC/PWM/Digital specific pins. Whereas Gx pins do not guarantee ADC/PWM function. Alternatively, pins can be used to support a fast read/write 8-bit wide or 4-bit wide bus.	3.3V
	G2/BUS2	I/O		3.3V
	G3/BUS3	I/O		3.3V
	G4/BUS4	I/O		3.3V
	G5/BUS5	I/O		3.3V
	G6/BUS6	I/O		3.3V
	G7/BUS7	I/O		3.3V
	G8	I/O	General purpose pin.	3.3V
	G9/ADC_D-/CAM_HSYNC	I/O	Differential ADC input if available. Camera horizontal sync.	3.3V
	G10/ADC_D+/CAM_VSYNC	I/O	Differential ADC input if available. Camera vertical sync.	3.3V
	G11/SWO	I/O	General purpose pin. Serial Wire Output.	3.3V