18th Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes

Workshop Proceedings

Workshop Chairman/Editor: B.L. Sopori

Program Committee:
M. Al-Jassim, P. Basore, T. Buonassisi, J. Gee,
J. Kalejs, B. Mulligan, J. Rand, T. Saitoh, R. Sinton,
M. Stavola, T. Tan, E. Weber, J. Werner, and
B. Sopori

Vail Cascade Resort
Vail, Colorado
August 3–6, 2008

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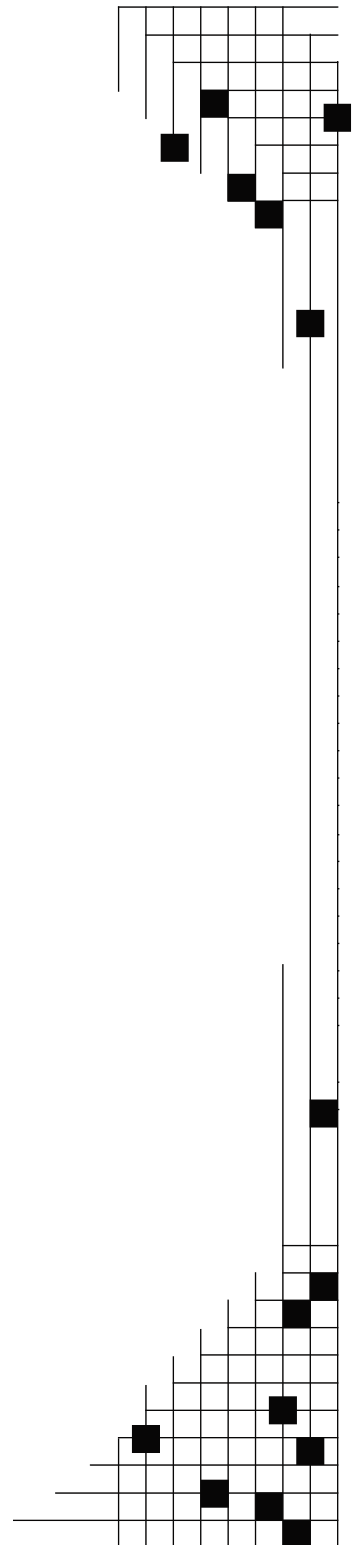M. Stavola, T. Tan, E. Weber, J. Werner, and
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TABLE OF CONTENTS

Workshop Theme: New Directions for Rapidly Growing Silicon Technologies

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A rapidly growing demand for photovoltaic (PV) energy during last few years has led to a very fast expansion of existing production facilities and a great deal of investment into new start-up companies. PV manufacturers have increased production to reach full capacities, and many new manufacturing facilities have been established whose production has either already started or will do so in the near future. The increased demand, in conjunction with high costs of conventional energy, has fostered a copious flow of venture capital funds into new silicon technologies.

In many cases, these technologies are founded on concepts from cross-cutting fields such as microelectronics, the display industry, and equipment manufacturing. These technologies address new device structures capable of higher commercial cell efficiencies, novel light-trapping structures, use of low-concentration designs, new thin-film silicon structures, and a host of ideas that have been dormant for lack of funds.

A major advancement in the PV industry will come from equipment manufacturers as they address larger cell/module areas, standardized machines, and larger sales in terms of number of machines. New companies bring novel technologies into wafer-based solar cells and also provide a strong impetus to thin-film Si solar cell technologies.

This sharp increase in the Si-PV industry and concomitant emergence of a host of new technologies will bring a multitude of new challenges. Currently, this growth seems to be limited only by the availability of the silicon. While the feedstock issue appears to be at a brink of resolution, there will be new fallouts ranging from a lack of experienced technical population to shortage of other materials needed for wafers, cells, modules, and PV systems.

The theme of this year's workshop reflects potential future changes in the PV industry, expected to arise from synergism of a very rapid growth in PV energy production and a large infusion of investments into many new technologies. These issues will be discussed in a combination of oral presentations by invited speakers, poster sessions, and discussion sessions. Special sessions will be devoted to:
- Feedstock Issues: Monitoring and Qualifying Poly Feedstock
- Progress in Thin-Film Silicon
- Advanced Crystal Growth
- Impurities and Defects in Si: Influence on Solar Cell Performance

In addition, a rump session—"R&D Strategies for a High-Growth Industry (Under Heavy Investment)"—will be held on Sunday evening, August 3.

I hope you enjoy this workshop.

Stimulating Commercialization CRADAs

John P. Benner
Manager PV Industry Partnerships
National Center for Photovoltaics
National Renewable Energy Laboratory

The CRADA (Cooperative Research and Development Agreement) is one of several legal documents used for industry to fund research at NREL. The "C" in CRADA is most important as its intent is to permit NREL and a company to work in partnership to move technology to the market faster. The CRADA is unique in providing clear and extensive coverage of ownership and protection for intellectual property (IP), providing simple mechanisms for protecting confidential information and providing clear descriptions of the work each partner will perform. As DOE was developing the Technology Pathway Partnerships (TPP) Announcement they looked carefully at the National Laboratories' interactions with industry and concluded that collaborations fall in two distinct categories – support and partnership – distinguished primarily by the extent of intellectual property involved. The TPPs also established a precedent that DOE was willing to cost-share NREL's contribution to partnerships. In 2008, the PV Program created a new project to fund work at NREL needed to stimulate and expand partnerships with industry. The scope ranges from completion of experiments needed to protect our IP before discussing the technology with potential partners through cost-sharing an expansion to ongoing collaborations. This talk will describe the various agreements for working with NREL, management values related to NREL IP, and this new program to make our industry partnerships even more fruitful.

THE SOLAR AMERICA INITIATIVE PV TECHNOLOGY INCUBATOR PROGRAM

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INTRODUCTION

The Solar America Initiative (SAI) PV Technology Incubator Program, funded by the U.S. Department of Energy (DOE) through the National Renewable Energy Laboratory (NREL), has the objective of shortening the timeline for companies to transition prototype and precommercial PV modules into pilot and full-scale manufacture. Entrance opportunities for the incubator project are anticipated every 9–12 months as funding becomes available. This program targets U.S. small businesses with a minimum entrance criterion of a demonstrated PV cell process, lab device, or module. The successful exit criterion is anticipated to be prototype modules and pilot production demonstration of approximately 3 MW/year.

Ten U.S. small businesses received subcontracts from NREL in the fall of calendar year 2007, averaging approximately $3.0 million each of NREL/DOE funding over an 18-month period. The subcontracts were awarded in two 9-month phases, with the second phase of funding contingent upon successful completion of the first phase deliverables and a Stage-Gate review. The award winners represent a diverse range of technologies including: polycrystalline thin films; thin- and wafer-silicon devices; high-efficiency III-V devices; thin-film organics; and concentrating systems.

SAI PV INCUBATOR OVERVIEW

The SAI is an integral part of the President's Advanced Energy Initiative (AEI). The AEI is designed to reduce the nation's dependence on foreign sources of energy by promoting broader research and development (R&D) to achieve substantive breakthroughs in a variety of energy resources, including solar photovoltaic (PV) systems. The SAI, authorized under the Energy Policy Act of 2005, represents a significant enhancement of DOE's business strategy of partnering with U.S. industry to accelerate commercialization of PV system R&D to meet cost and installed capacity goals. These SAI goals are to 1) substantively accelerate development of U.S.-produced PV systems so that PV-produced electricity reaches parity with the cost of electricity in select grid-tied target markets across the nation and 2) expand the U.S.-installed domestic capacity of PV systems to 5–10 gigawatts (GW). The Solar Energy Technology Program's (SETP's) Posture Plan (www.eere.energy.gov/solar/solar_america/publications.html) illustrates how the SETP aligns with the SAI mission and the President's Advanced Energy Initiative.

To accomplish the goals of the SAI, a multi-tiered, multi-phased program was established that addresses the near-, mid-, and long-term technological and scientific advances for improved performance, lower cost, and improved reliability of PV system components and installed systems.

The SAI PV Technology Incubator Program is designed to accelerate technologies/processes that have successfully demonstrated a proof-of-concept/process in a lab, but are not yet mature enough for large-scale commercial production. The emphasis is currently on the barriers to entering commercialization by 2010. Prototypes of these PV systems and components will be produced on a pilot scale in a relevant operational environment with their demonstrated cost, reliability, or performance advantages. PV and concentrating PV modules are targeted in this phase of the technology development pipeline with goals that include more efficient use of materials, better performance, higher reliability, and improved manufacturing. Details on the current solicitation requirements can be found at www.eere.energy.gov/solar/solar_america/pv_incubator.html

Responses to past solicitations indicated a need for a "pre-incubator" solicitation. This would include small businesses that had a concept/patent and would proceed to establishing a prototype that would eventually be manufacturable. It is anticipated that this solicitation will be released late this year.

EXISTING SUBCONTRACTS

Ten U.S. companies were awarded subcontracts through a competitive merit review-based process. Analysis of project metrics was conducted for all technology areas. The resulting projects include a diverse set of technological approaches: Inexpensive and Thin-Film Si; Low and High Concentration; Innovative Thin-Film Manufacturing; and Low-Cost Multi-Junction Cell Production. The $27M in DOE funds awarded to these ten subcontracts represents 29% of the $93M worth of R&D taking place under the PV Incubator Program. The current subcontracted projects and recent accomplishments are described below.

AVA Solar
AVA Solar has demonstrated fully automated, continuous in-line fabrication of CdS/CdTe PV. This project will enable the demonstration of extremely low manufacturing and equipment costs, improved module efficiencies, and the ability for rapid manufacturing capacity expansion.

To date, NREL has verified average efficiency of over 11.0% for small-area thin-film CdTe solar cells. The subcontractor has also demonstrated uniformity of +/–10% on 16.5" x 16.5" substrates. All processing steps for the fabrication of modules of 16.5" x 16.5' are now installed in the pilot line.

Blue Square Energy
Manufacture of thin crystalline silicon solar cells by growing a high-purity silicon layer onto a low-cost metallurgical-grade silicon substrate. This approach can produce the high performance and reliability of traditional solar cells with reduced material use and manufacturing costs.

Accomplishments to date include front-surface passivation, resulting in a surface recombination velocity of <100 cm/s; light-trapping increases in J_{sc}; and efficiencies >14% on 4-cm^2 Cz-Si substrates and >11% on 100-cm^2 Cz-Si substrates.

CaliSolar
Production of cost-effective solar cells from low-cost and abundant, but impurity-laden, Si feedstock materials. The focus will be on a novel and adapted metallization method that is suitable specifically for using metallurgical Si to manufacture solar cells with over 17% efficiency using multicrystalline Si—and within the next 18 months.

Recently, NREL verified 15%-efficient cells with an optimized front- and rear-contact grid structure.

EnFocus Engineering
A lightweight, low-profile, high-concentration PV module that is fully encapsulated and protected from wind, hail, dust, and moisture. This module will use high-efficiency multi-junction cells to generate higher power outputs in area-constrained applications such as rooftops.

Accomplishments to date include improving initial module subassembly efficiency to >23%; developing and implementing design improvements that have increased mechanical durability; implementing damp-heat and mechanical stress testing; designing and building an improved Fresnel optic with >75% transmission efficiency; and demonstrating long-term tracking accuracy of less than 1°.

MicroLink Devices
MicroLink Devices will develop a low-cost, high-efficiency, dual-junction GaAs-based solar cell for use in 500x concentrator systems. The developed solar cell minimizes GaAs material usage while improving heat dissipation with a potential to reduce cost by 50%.

To date, MicroLink Devices has demonstrated an average cell efficiency of 22% under 1-sun illumination for multiple dual-junction devices. These 1-cm^2 devices were processed on a 4-inch wafer using the epitaxial liftoff fabrication method; this was also demonstrated on a 6-inch wafer.

Plextronics
Commercialization of thin-film organic photovoltaic (OPV) technology. Plextronics will develop higher-efficiency cells while increasing module-lifetime design to enable this ultra-low cost material to compete with traditional PV technology.

Plextronics has confirmed a cell efficiency of 5.4% measured at NREL. This is the highest efficiency ever confirmed for an OPV cell at NREL. Plextronics delivered to NREL a submodule (108-cm^2 active area) that had an efficiency >1.5% after 2000 hours of illumination.

PrimeStar Solar
Development of commercial CdTe module production based on the NREL 16.5% world record CdTe laboratory solar cell technology. The increased module energy conversion efficiency will lower installation costs and open new markets for CdTe-based thin-film modules.

To date, NREL has verified small-area thin-film CdTe solar cells with efficiencies >12.0%. For 6" x 6" minimodules, NREL has verified a conversion efficiency >10.0%.

Solaria
Solaria's PV-multiplying process yields two to three highly efficient cells from one, via solar cell singulation and optical amplification. Solaria's project aims to produce a non-tracking, standard module form factor with 2x–3x concentration manufactured in a reliable, high-volume, automated process.

Recently, Solaria representatives stated that they have a purchase agreement with Q-Cells

for 1 GW of cells, and that they have contracted sales for 500 MW of 2x concentrator "supercells."

SolFocus

Project involves 500x concentrating PV module emphasizing high reliability and high efficiency to enable large-scale commercial and utility market penetration. A folded reflective design allows for a high optical efficiency and acceptance angle in a compact frame.

Accomplishments to date include developing and constructing a higher-efficiency optic design; optimizing reflectivity and durability of optic coatings for the primary and secondary mirrors; implementing and stress-testing a new module sealant; developing and implementing cell, receiver, and panel performance test methodologies and equipment; and developing a dFMEA (design failure mode effects analysis) process to identify and prioritize initial performance and reliability risks.

SoloPower

Development of an electroplating-based, high-efficiency, low-cost CIGS cell and module manufacturing technology. Advantages of this deposition technique include lower equipment costs, reduced processing times, and increased material utilization.

Recently the company achieved a 1-m^2 module that yielded 8.9% efficiency as measured by NREL.

CURRENT AND FUTURE SOLICITATIONS

The current PV Incubator subcontracts are undergoing a Stage-Gate review process during the summer of 2008. At this time, an evaluation of progress will occur and a determination to continue with the second 9-month phase of the subcontract will be made. In addition, announcement of the second round of incubator awards stemming from the spring 2008 solicitation are anticipated in August 2008.

Finally, as mentioned above, future entrance opportunities for the incubator project are anticipated every 9–12 months as funding opportunities become available. This would put the next solicitation in early 2009.

ACKNOWLEDGEMENTS

The Leading Edge of Silicon Casting Technology and BP Solar's Mono^2 Wafers

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Abstract. A novel crystal growth method has been developed for the production of ingots, bricks and wafers for solar cells. Monocrystallinity is attainable over large volumes with minimal dislocation incorporation. With a novel defect profile of impurities and structural defects, as-grown wafers have averaged 40-80 microseconds in minority carrier lifetime with significantly less lifetime variability than multicrystalline cast wafers. Solar cells of 156 cm^2 size have been produced ranging up to 17.2% in efficiency using a variety of production-ready cell processes. Simulations indicate potential for over 22% efficiency for a back contact cell.

Introduction

Cast silicon has been used in the manufacture of solar cells for over 30 years. As alternatives to single crystal silicon grown by Czochralski (CZ) or Float Zone (FZ) methods, lower quality cast and ribbon silicon substrates have disadvantages compared with the considerable perfection achieved in standard single crystal silicon manufacturing. Solar cells made from multicrystalline silicon (multi Si) wafers have historically been limited in electrical efficiency by grain boundaries to some extent but, more significantly, by the high density of dislocations in many grains[1], and the metallic impurities that aggregate at these structural defects[2]. Many dislocations are generated during growth from high stress points in grain boundaries.[3] Additionally, the difficulty in texturing the multi Si wafer surface has been an optical disadvantage. Nevertheless, multi Si has steadily grown in market share due to higher throughput in kg/hr, simpler manufacturing and resulting lower cost inherent in its growth. Today, multi Si wafers have the largest market share of any technology in the solar industry. The development of multi Si solar cell processing, primarily limited to screen printing, has resulted in efficiency improvements with elements such as silicon nitride passivation, aluminium back surface field and thinner front print line widths. The substrate itself has not changed dramatically since the inception of casting. While ingot sizes have increased 3x in horizontal dimensions and somewhat vertically, the average crystallinity has been little affected. Furthermore, the best lab results of cell efficiency on p-type multi Si have had to rely on relatively long time phosphorus gettering in

order to deal with defect clusters: pockets of transition metals or oxygen precipitates aggregating at tangled dislocations[4].

It has long been recognized that a cast single crystal product would have inherent advantages over both CZ and multi Si. Early attempts to cast single crystal silicon using the 'heat exchanger method' encountered problems due to multicrystalline nucleation on the floor of the crucible[5]. Despite maximizing the curvature in the crystal growth interface, only bricks with significant multicrystalline volumes could be produced. Conversely, cold crucible casting techniques have been unable to avoid the in-growth of randomly nucleated crystals from the cold walls to the center of the ingot, and generally suffer from even smaller grain sizes than traditional casting.[6]

Recent work at BP Solar has resulted in a new technique for casting ingots with the potential for producing silicon with extremely low defect densities: Mono^2 silicon[7]. The technique involves a proprietary growth nucleation process for the casting of ingots and is used to produce single crystal bricks and wafers, or wafers with specifically chosen grain boundaries. First, the state of the art for industrial casting will be reviewed and then recent production and research results for Mono^2 will be discussed.

State of the Industry

Recent developments in casting have focused on a few key aspects: grain boundaries, ingot size and doping. Usami *et al.* conducted a number of studies aimed at achieving electrically inactive grain boundaries in p-type silicon.[8,9] In a clever experiment, they were able to watch the nucleation of dendritic crystals from the corner of a crucible, and they contend that the columnar crystals formed by evolution of the dendritic crystals have lower grain boundary energy than the average random grain boundary.[10] In production ingots produced with standard recipes, it is typical to see a dendritic network at the bottom of an ingot, so we may already be benefiting to some extent from this phenomenon. In a cross-over subject, Deutsche Solar has reported low grain boundary activity in ingots cast with n-type material.[11] To date, n-type multi has not been commercialized due to the lack of a production-ready cell process for the substrate. Deutsche Solar has also reported casting of both taller and larger cross-section ingots at increased growth rates indicating good scalability to the casting process.[12]

There has also been a major effort to commercialize electromagnetically cast silicon. Up to 2 ton ingots have been cast using the 'bottomless cold crucible' technique where a copper inductor is used to support a domed mass of liquid by electromagnetic (EM) repulsion. Silicon is metered into the dome from the top while the ingot is solidified and extracted through the bottom. The silicon produced from such a process suffers in a couple ways. Attempts to produce large or seeded crystals have been foiled by the high curvature of the growth interface due to the $1400\,^{\circ}C$ thermal gradient between the water cooled copper and the liquid silicon, which leads to random nucleation of very small crystals at the sides of the ingot. While the central crystals are somewhat higher in quality and can be several millimeters in diameter, there is generally a pronounced low lifetime band protruding in from every side of the ingot and associated with very small crystals and very high dislocation densities.[13] Other issues include the high energy consumption involved in melting in a cold crucible, as well as potential copper contamination and light-induced degradation of solar modules made with EM cast cells.

The final issue undergoing heavy experimentation is the incorporation of solar grade, electrically compensated silicon into cast material. In general, this material is around "6N's" pure, or 99.9999% pure, with the primary impurities being carbon, boron, phosphorus and iron. According to the literature, starting with roughly matched levels of boron and phosphorus produces a mostly p-type ingot due to the differing distribution behaviors between the liquid and solid phases.[14] Boron, which incorporates readily at the solidification interface, is prevalent at fairly steady levels throughout the ingot while phosphorus preferably remains in the liquid. As a result, the ingot will be nominally p-type through 80-90% of the ingot, and n-type at the top, see Fig. 1. A number of new suppliers offer solar grade silicon of varying impurity profiles. In general, silicon feedstock with higher phosphorus leads to higher levels of boron being needed, which produces ingots of lower average resistivity and potentially lower lifetime. In the shortage of high purity polysilicon, some silicon manufacturers have chosen to go to an extreme in this tradeoff, producing highly doped wafers that can only produce 11-13% efficiency using screen print cell processing. Another issue with solar grade silicon is carbon content. While cast ingots are typically saturated with carbon and nitrogen from *in situ* contamination, liquid-grown precipitates generally form most heavily at the end of the growth cycle. When using solar grade feedstock that contains silicon carbide particles initially, the chances are higher for incorporating yield-reducing inclusions into the final ingot.
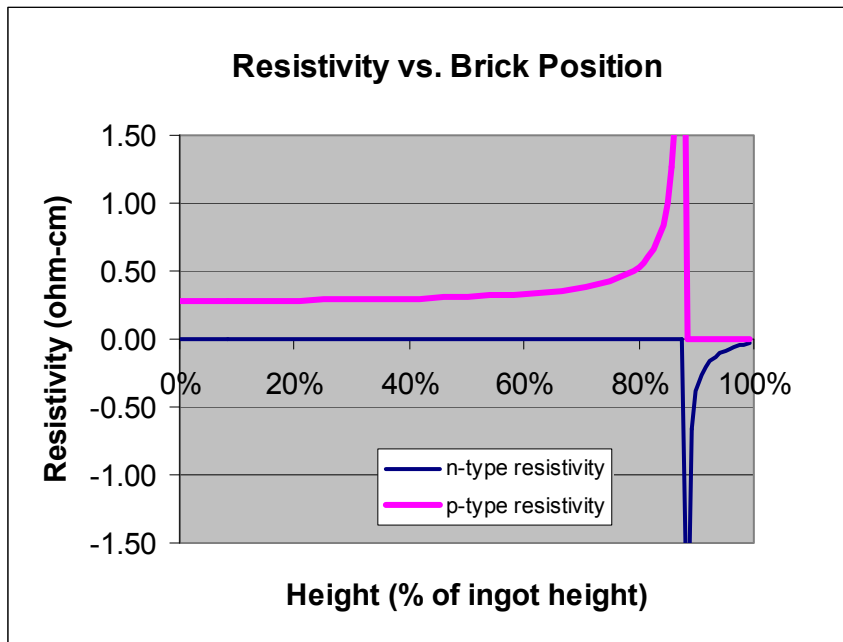
Fig. 1: The resistivity of a brick cast with compensated solar grade silicon varies dramatically along the height (x-axis), with a crossover from p-type to n-type near the top of the brick. Diluting the feedstock with intrinsic silicon can increase the base resistivity, but leaves the crossover point unaffected.

The research interests of BP Solar have overlapped with the larger industry on the topics of ingot size and solar feedstock. However, bulk material improvement efforts have been focused on carbon reduction and realizing and perfecting a cast single crystal ingot.

Experimental

Ingots have been cast in standard production furnaces at BP Solar to the industry standard size of 690x690 mm^2 and a mass of 265 kg. The ingots have been cut into a 5x5 grid of 12.5 cm bricks, which have been wafered to a nominal thickness between 160 and 200 microns. Wafers are

generally etched in a sodium hydroxide bath to remove saw damage, optionally textured with a pyramidal etch or isochemical texturing, and can be phosphorus-diffused either in a belt furnace or in a tube furnace. In some cases, groove diffusion is performed by making laser grooves in a silicon nitride mask and using a relatively heavy tube diffusion. For minority carrier lifetime measurements, bricks are measured as-cut without passivation, while wafers are measured with methanol iodine passivation after having any processing stripped back. Mapping has been performed using SemiLab WS2000 microwave photo-conductance decay equipment.

Results and Discussion

Bricks and Wafers: A broad survey of structural defects reveals a considerable difference between traditional multicrystalline cast silicon and Mono[2] silicon. Examples of selectively etched 12.5cm wafers from cast ingots are shown in Fig. 2, where heavily dislocated grains appear as dark regions. Studies of minority carrier lifetime have shown that the dislocation density controls the grain-to-grain lifetime variations in multi Si even on a sub-millimeter scale.[15] Furthermore, the lifetimes in heavily dislocated grains, with dislocation densities $> 10^6$ cm^{-2}, do not recover to 'good grain' levels as a result of phosphorus diffusion and hydrogen passivation.
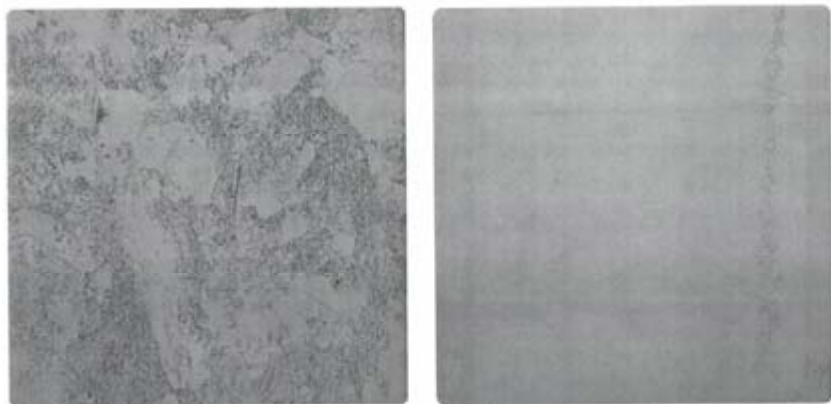
Fig. 2: Multi Si (left) and Mono[2] (right) wafers after selective etching. Darker areas have higher densities of structural defects, mostly dislocations.

The absence of large angle grain boundaries in Mono[2] is not itself taken to be the chief benefit. In fact, due to the relatively large average grain size, the lifetime of multicrystalline wafers is determined primarily by grain-to-grain variations in dislocation density and not by the electrical activities of the boundaries themselves. In Fig. 3, minority carrier lifetime maps and histograms are shown for as-grown multi and Mono[2] wafers from similar positions in an ingot. While the average lifetimes for the two wafers are similar, the two maps could hardly be more different. The distribution of the multicrystalline wafer is typical for a wafer coming from one of the centrally positioned bricks. While some grains have extremely high lifetimes, the majority of grains fall below 30 microseconds. According to simulations, variations in lifetime cause a decrease in open circuit voltage from the V_{oc} that would be predicted for a wafer with a given average lifetime value.[16] According to this work, a ratio of good to bad lifetime in the 20:1 range can pull down Voc on a cell by up to 60 mV relative to a uniform wafer with the same average. By contrast, the lifetime of Mono[2] wafers is more tightly distributed, with a typical lifetime variation closer to the 2:1 range, resulting in minimal loss (<10 mV) from the ideal case.

In examining a series of wafers ranging from the bottom to the top of a brick, as-grown wafer lifetimes start low for a couple centimeters, generally less than 10 microseconds, then through the bulk of the brick remain quite high (40-80 microseconds average), while the top 10% of a brick will see a decrease back down to the 10-20 microsecond range. After a typical phosphorus

diffusion and etch-back, the low-lifetime wafers at the bottom of the brick will recover to normal Mono[2] lifetime values, while those wafers from the top do not significantly improve. Hydrogenation has been shown to further improve bulk lifetime by up to a factor of 3.

The wafers discussed thus far have been cut from the center of the ingot (e.g. the middle nine bricks of a 25 brick ingot). Next, consider the comparison of wafers cut from the edge of the ingot, see Fig. 4. While the Mono[2] wafer has a lower lifetime region of structural defects, the variability in lifetime is still better than the multi case. The very interesting effect is that the typical low-lifetime region found in wafers cut from edge bricks is almost non-existent on the Mono[2] wafer. Surprisingly, this is the case from the top to the bottom of the brick. This fact presents extra benefit for Mono[2] wafers over multi, and closer competition with CZ.
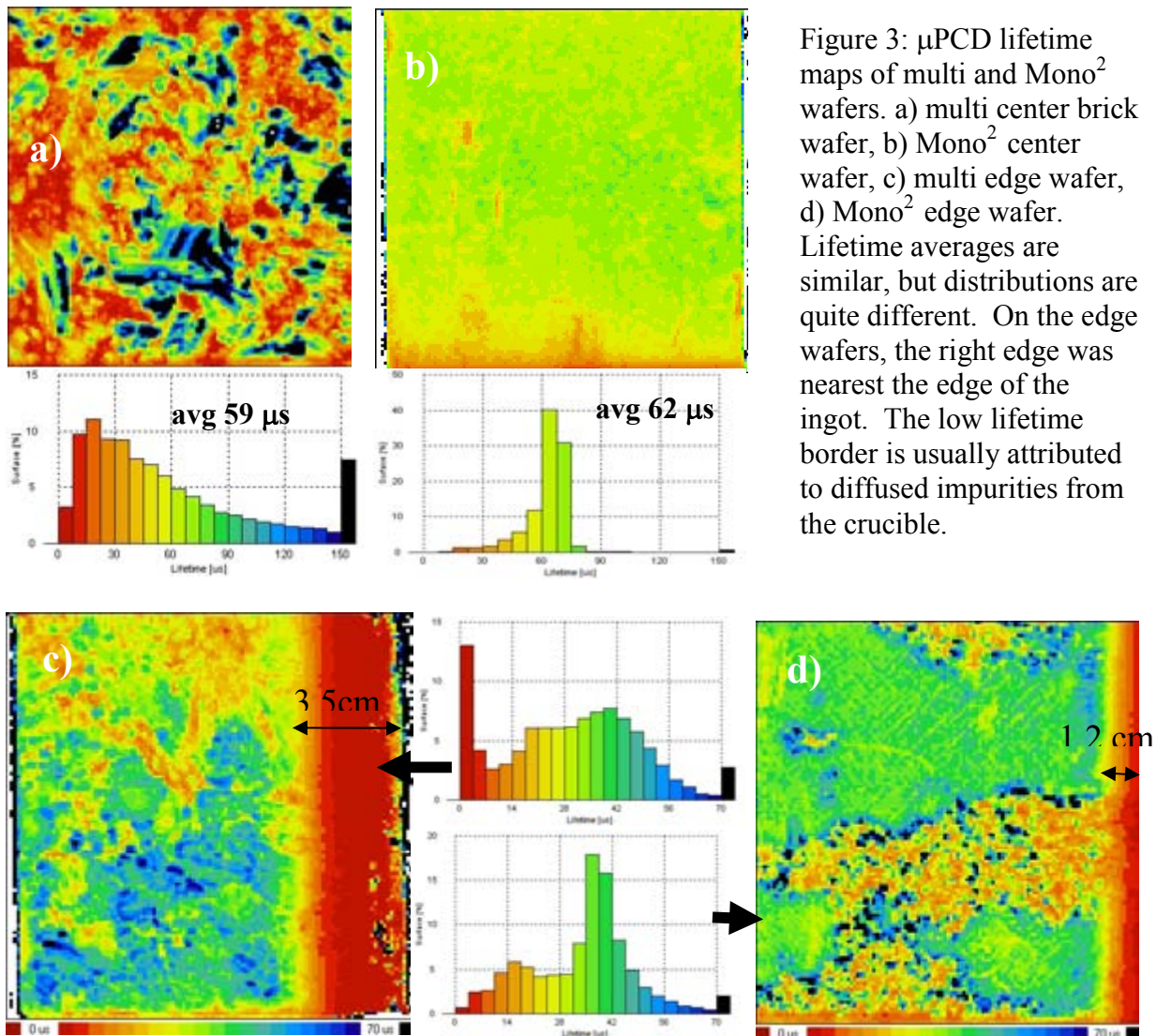
Figure 3: μPCD lifetime maps of multi and Mono[2] wafers. a) multi center brick wafer, b) Mono[2] center wafer, c) multi edge wafer, d) Mono[2] edge wafer. Lifetime averages are similar, but distributions are quite different. On the edge wafers, the right edge was nearest the edge of the ingot. The low lifetime border is usually attributed to diffused impurities from the crucible.

Having considered wafer quality, now consider the material from a crystalline yield point of view at the brick level. It is not entirely difficult to cast an ingot such that the center bricks end up nominally monocrystalline. Unfortunately, it is considerably more difficult to maintain monocrystallinity throughout the edge bricks. Early tests routinely produced edge bricks that

appeared similar to those in Fig. 4a. With an intention to produce a (100) ingot in order to take advantage of pyramidal texturing, the entire ingot starts as (100) oriented. However, when growing next to randomly nucleated crystals, the (100) orientation competes poorly for surface area, tending to twin along a diagonal at roughly 55° to the bottom. The twinned crystal is generally of poor quality, and can degrade further into more random crystals. Wafers cut from bricks like those in Fig. 4 would appear to have one very large crystal covering 30-90% of the wafer, with the remaining area appearing as typical multicrystalline material. This material has been termed 'Mono/poly' and is typical of sub-optimal seeded casting. After a significant amount of process development and optimization, we have developed techniques to control (100) crystals such that they grow vertically and produce Mono^2 edge bricks. An example of vertical (100) growth is shown in Fig. 4.
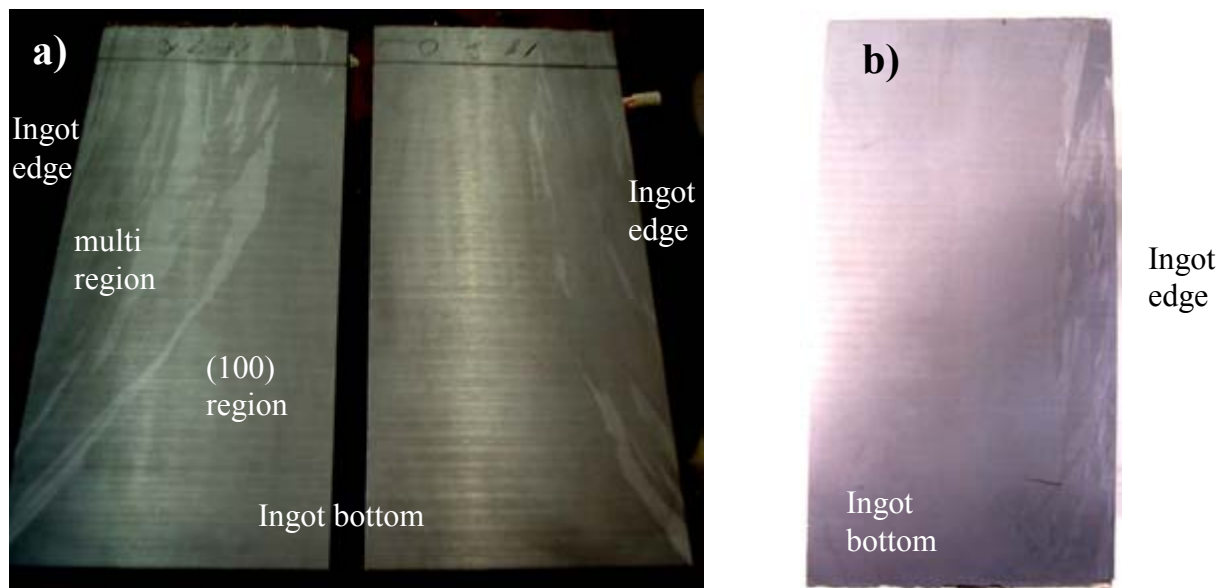
Fig. 4: Edge bricks showing in-growth of multi (left two), and optimized vertical growth of (100) against the multicrystalline region (right).

Cell Results

Mono^2 solar cells made at BP Solar have been produced using a variety of surface texturing options in conjunction with standard industrial screen print processing. The (100) wafers can easily be textured with a pyramidal sodium+IPA etch to produce black solar cells. Large batches of wafers have averaged 16.2% electrical efficiency for 12.5cm cells, with some cells ranging as high as 17.0% under AM1.5 illumination. This represents a 1% absolute efficiency gain (6% power gain) over multi wafers made with the same process, and equivalent performance to CZ wafers manufactured with the same process. Wafers made with a sodium hydroxide polish etch and no surface texture have averaged 0.5% higher than multi, while iso-chemically textured wafers have been intermediate between the NaOH etch and the pyramidal performance. Diffusion length has averaged from 500 to 650 microns on screen printed cells as measured using multiple wavelengths on finished cells.

While these results are promising, the real promise of Mono^2 lies in more advanced cell structures. A project has been undertaken to systematically test wafers with various production-

ready advanced techniques. These have been broken down into two categories here: an advanced front with a standard screen print back, and an advanced back with a normal screen print front. The results of the testing on p-type wafers are shown below in Table 1. It is expected that putting the advanced front and back structures together will result in even higher efficiencies. Work is ongoing to produce cells on n-type Mono^2 wafers, with significant promise. Simulations for a novel BP Solar back contact structure on a Mono^2 substrate have estimated in excess of 22% conversion efficiency. On the whole, Mono^2 wafers have had equivalent lifetimes and cell efficiencies to commercially available CZ wafers.

Process	Type	Voc	Isc	FF	Average Eff	Number of Cells
		mV	A	%	%	
Screen Print Texture	p-type	610	5.4	76.4	16.2	>2000
Advanced Rear	p-type	635	5.4	77.6	17.2	5
Advanced Front+back	p-type	612	5.5	77.0	17.1	4
Simulated Back Contact	p-type or n-type	675	6.2	82.5	22.2	0

Module Results

In the 4th quarter of 2007, BP Solar produced, sold and installed roughly 200kW of Mono^2 modules in a pilot run. For simplicity's sake, these modules were made using an identical cell process to the standard multi-crystalline product. These modules were installed with power tracking capability, and we now have several months of performance data. On the whole, the Mono^2 modules are averaging 6% more power than their multicrystalline counterparts, even though they have no wafer texturing. Because the wafers come from cast ingots, they have low oxygen concentrations and have lost no more than 0.5% of power to light induced degradation, making their field performance better than traditional mono modules. This year, BP Solar will increase Mono^2 casting capacity to 25% of the total, with plans to significantly increase this proportion in 2009 and 2010.

Conclusions

The Mono^2 process has been demonstrated to produce single crystal ingots suitable to make solar cells averaging 17.2% using production-ready processes. As an absolute base case, untextured screen print Mono^2 modules have been shown to produce 6% more power in the field than multi Si modules. Historically, the dynamics of market competition for different technologies in the photovoltaic sector have typically been framed in terms of a trade-off: one can have high energy efficiency or low cost of manufacture. Different players have chosen to operate at different ends of the spectrum, from back-contact 20+% silicon to <10% thin film, but all result in a surprisingly similar installed $/Watt cost. Mono^2 technology can offer the best of both worlds. Single crystal casting is still in its infancy, and there is reason to believe that significant improvements will be attainable in defect management over what can be manufactured today. But even with demonstrated lifetimes, electrical efficiencies in excess of 22% are attainable. With today's single crystal cast ingot, BP Solar believes that the Mono^2 substrate together with new technology in cell processing will break out of the historical trade-off dynamics and move to a place where low cost together with high electrical efficiency achieve widespread grid parity.

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Time dependent and/or 3D investigation of carbon, nitrogen and dislocation distributions in a silicon crystal during solidification process

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ABSTRACT

The unidirectional-solidification process is a key method for large-scale production of multi-crystalline silicon for use in highly efficient solar cells in the photovoltaic industry. Since the efficiency of solar cells depends on the crystal quality of the multi-crystalline silicon, it is necessary to optimize the unidirectional-solidification process to control temperature and impurity distributions in a silicon ingot. We developed a transient global model for the unidirectional-solidification process. We carried out calculations to investigate the temperature and impurity distributions such as carbon and nitrogen, and dislocation density in a silicon ingot during solidification process by taking into account phase diagram. Solid-liquid interface in rectangular crystals is also investigated by using 3D global model.

1. Introduction

The unidirectional-solidification method is a key method to produce multi-crystalline silicon for use in highly efficient solar cells [1]. Since the efficiency of solar cells depends on the quality of the multi-crystalline silicon, which is determined by the crystallization process such as cooling rate and rotation rate of a crucible, it is important to investigate and optimize the unidirectional-solidification process to control the distributions of temperature and impurity in a silicon ingot during the solidification process.

Numerical calculation has become a powerful tool for investigation and optimization of a unidirectional-solidification process and crystal growth process with development of computer technology and new algorithms [2-12]. Since a unidirectional-solidification furnace has a highly nonlinear thermal system, transient simulation with global modeling is an essential tool for investigation and improvement of a unidirectional-solidification process from melting to cooling through the solidification process. We developed a transient code with a global model for the unidirectional-solidification process, and we carried out

calculations to investigate distributions of temperature and impurity in a silicon ingot during the unidirectional-solidification process [13, 14].

2. Model Description and Computation Method

Figure 1 shows the configuration and dimensions of a small unidirectional-solidification furnace for producing multi-crystalline silicon. The melt, a crystal, a crucible and a pedestal are denoted as 1, 2, 3, 4, 5 and 6, respectively. Thermal shields are labeled as 7 to 11. The two heaters marked by 12 and 13 were set to the furnace. The following points are assumed in the present calculation: (1) the geometry of the furnace configuration is axisymmetric, (2) radiative heat transfer is modeled as diffuse-gray surface radiation, (3) the melt flow in the crucible is laminar and incompressible, and (4) the effect of gas flow in the furnace is neglected.
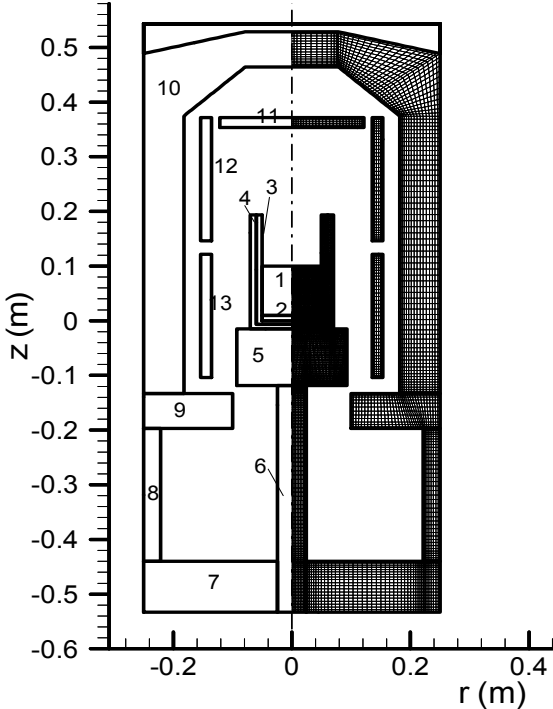
Fig. 1 Configuration and computation grid of a casting furnace. The melt, a crystal, a crucible and a pedestal are denoted as 1, 2, 3, 4, 5 and 6, respectively. Thermal shields are labeled as 7 to 11. The number of 12 and 13 show multi heater.
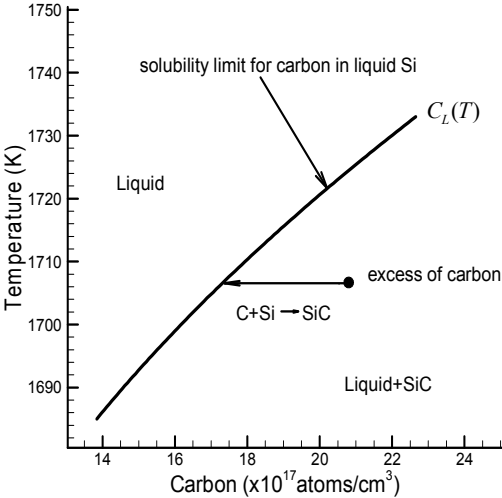
Fig. 2 Schematic of SiC particle precipitation with the Si-C phase diagram in the Si-rich domain.

The domains of all components in a unidirectional-solidification furnace are subdivided into a number of block regions, as shown in the left part of Fig. 1 in order to establish a discrete system for numerical simulation. Each block is then discretized by structured grids, which is shown in the right part of Fig. 1. Conductive heat transfer in all solid components, radiative heat exchange between all diffusive surfaces in the unidirectional-solidification furnace, and the Navier-Stokes equations for the melt flow in the crucible are coupled and solved iteratively by a finite volume method in a transient condition.

Figure 2 shows a schematic of SiC particle precipitation in Si-melt with the Si-C phase diagram in the Si-rich domain [15], in which the solubility limit of carbon in Si-melt $C_L(T)$ is approximated by a polynomial function:

$$C_L(T) = 8.6250 \times 10^{-4} T^2 - 2.7643T + 2222.9 . \tag{1}$$

The units for carbon concentration and temperature in eq. (1) are $10^{17} atoms/cm^3$ and K, respectively. With solidification of the molten silicon and upward movement of the solidification interface in the crucible during the solidification process, the carbon concentration in the melt increases due to the small segregation coefficient of carbon in silicon. If the carbon concentration exceeds the local solubility limit, excessive carbon precipitates and the following chemical reaction occurs:

$$Si + C \rightarrow SiC . \tag{2}$$

The substitutional carbon is thus reduced and the same amount of SiC particles is generated in the Si-melt. The formation rate of SiC particles and the destruction rate of substitutional carbon are equal and proportional to the super-saturation degree of substitutional carbon and the speed of the chemical reaction (2):

$$G_{SiC} = -G_C = \alpha(C_C - C_L(T)), \qquad \text{when } C_C > C_L(T) , \tag{3}$$
$$G_{SiC} = -G_C = 0, \qquad \qquad \text{when } C_C \leq C_L(T), \tag{4}$$

where G_{SiC} and G_C are the formation rates of SiC particles and substitutional carbon, respectively. Minus values denote the destruction rate. The coefficient α is a factor correlating the particle formation rate and the chemical reaction rate in (2). For convenience, we name it the reaction rate coefficient. It is assumed that the chemical reaction (2) occurs rapidly when carbon is super-saturated in the melt. The value of α will be determined in our modeling.

With these assumptions, the governing equations for the concentrations of substitutional carbon and SiC particles in Si-melt can be expressed as follows:

$$\frac{\partial C_C}{\partial t} + \mathbf{V} \cdot \nabla C_C = \nabla \cdot (D_C \nabla C_C) + G_C \quad \text{for substitutional carbon,} \tag{5}$$

$$\frac{\partial C_{SiC}}{\partial t} + \mathbf{V} \cdot \nabla C_{SiC} = G_{SiC} \qquad \text{for SiC particles.} \tag{6}$$

The initial conditions for both impurities in the melt are defined as follows:

$$C_C = C_0 \qquad \text{for substitutional carbon,} \tag{7}$$

$$C_{SiC} = 0 \qquad \text{for SiC particles,} \tag{8}$$

where C_0 is the carbon concentration in the silicon feedstock. The zero mass flux condition is applied at crucible walls and the top surface for both impurities. At the melt-solidified ingot interface, the segregation effect is taken into account for substitutional carbon and the continuity condition is applied for SiC particles. The effective segregation coefficient of carbon in silicon was set to 0.07. Nitrogen concentration in the process was also carried out by imposing the segregation coefficient of 0.0007.
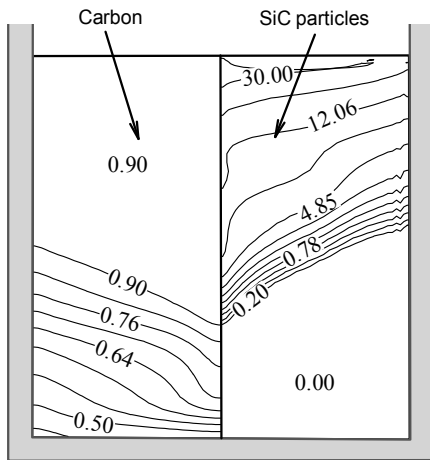
Fig. 3   Distributions of substitutional carbon (left) and SiC particles (right) in a cross-plane of the ingot solidified in a fast-cooling process. Unit of concentration is $10^{17} \, atoms/cm^3$.
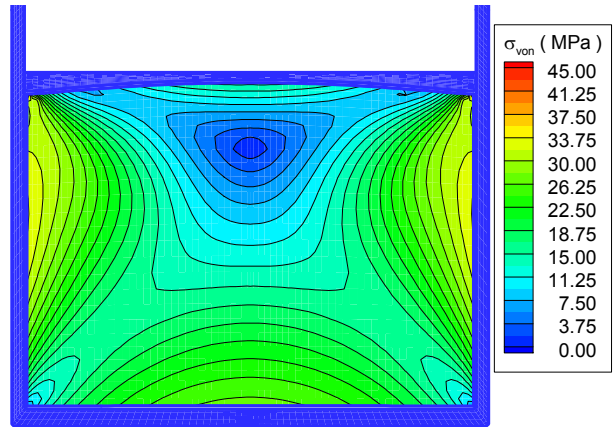
Fig. 4   Von Misess stress distribution for the rigid boundary condition on the ingot and crucible wall interface.

For axisymmetric thermoelastic stress, analysis is performed in the silicon ingot using a displacement-based thermo-elastic stress model, which has been widely used for SiC and AlN crystal growth processes [16–18].   Since the gravity is negligible compared with the thermal stress, it is not considered in the equilibrium equations.

Results and discussion

Figure 3 shows the distributions of substitutional carbon (left) and SiC particles (right) in a cross-plane of the solidified ingot.   It can be seen that particle precipitation begins in the central area when the fraction solidified reaches about 30%.   The SiC particles are clustered at the center-top region of the ingot, where the concentration of substitutional carbon is almost constant.   This distribution pattern is due to the melt-solidified ingot interface shape, which is concave to the solid side throughout the solidification process.

The impurity level in silicon feedstock has significant impact on the conversion efficiency of a multicrystalline silicon solar cell.   We carried out a series of computations for the same fast-cooling solidification process but with different carbon concentrations in silicon feedstock (C_0).   The obtained concentration distributions of substitutional carbon and SiC particles along the center axis of the solidified ingot are compared in Fig. 4 with the carbon concentration in silicon feedstock ranging from $1.26 \times 10^{16} \, atoms/cm^3$ (equivalent to 0.1 ppmw) to $6.30 \times 10^{17} \, atoms/cm^3$ (equivalent to 5.0 ppmw).   When C_0 is $1.26 \times 10^{16} \, atoms/cm^3$, no SiC particles are precipitated in the ingot and there is only a very thin layer rich in substitutional carbon at the top.   When C_0 increases to more than $1.26 \times 10^{17} \, atoms/cm^3$, the content of SiC particles increases significantly in magnitude as well as in space in the solidified ingot.   It is thus necessary to control the carbon concentration in silicon feedstock to less than $1.26 \times 10^{17} \, atoms/cm^3$, which is equal to 1.0 ppmw.

Figure 4 shows the von Mises stress distribution in the silicon ingot.   The results show that the maximum value of the stress distributes at the periphery of the crystals.   In this case, we imposed elastic deformation.   When we consider inelastic effects including dislocation distribution, the stress reduced about 15times smaller than that with an assumption of elastic deformation shown in Fig. 4.

4. Summary

A transient global model and code were developed for analyzing a casting process. We predicted the distribution of temperature and iron distributions as a function of time. The results showed that iron diffused even after the end of solidification, which is due to the rather small activation energy of iron in silicon. A U-shaped distribution of iron in the z-direction could be predicted by using the newly developed code, which can calculate transient phenomena of a casting process of silicon for photovoltaic devices.

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Innovative Crystallization of Multi-Crystalline Silicon Ingots using Compensated Metallurgical Grade Silicon

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Abstract

The presented work is a part of the French Photosil project which deals with the plasma purification and crystallization of metallurgical grade silicon. In this paper we present results obtained from a multi crystalline silicon ingot made from 100% purified metallurgical silicon (SoG). Despite a relatively high concentration of remaining impurities in the feedstock after purification, especially boron and phosphorous ($2.5 10^{17}$ and $3.5 10^{17}$ cm^{-3} respectively), solar cells obtained from the crystallized ingot exhibit an average efficiency of 14%. More surprising, analysis of these solar cells shows an increase of the minority carrier diffusion length with the ingot height, i.e with the degree of compensation. Indeed, due to the more efficient segregation of phosphorous during crystallization the upper part of the ingot presents regions of strong compensation and even an inversion of polarity type from p-type to n-type at 70% of its height. However, this reduced material yield is counterbalanced by lowering silicon losses due to ingot cropping. The innovative crystallization process used is based on a new furnace configuration and on a high purity quartz crucible allowing a lower contamination of the ingot during crystallization. This innovative crystallization process is also described.

1. Introduction

As the demand for high-quality solar grade Si feedstock exceeds supply and drives prices upwards, new solar grade silicon production techniques are being developed [1]. Currently, among the different projects to overcome this shortage by establishing a dedicated solar silicon production, two major routes can be distinguished. The first, called the chemical route, is related to the purification of silicon by means of a simplified Siemens process, consisting of decomposing trichlorosilane by CVD [2]. The alternative route, known as the metallurgical route, involves obtaining solar-grade silicon directly from metallurgical silicon [3]. This route for production can be five times more energy efficient than the conventional Siemens process that uses more than 200 kWh/kg [4]. However, metallurgical route production techniques are generally less efficient in removing dopants and an important point related to the use of purified

metallurgical Silicon is the presence of both, n-type and p-type dopant atoms (Phosphorous and Boron).

Moreover, due to their relatively high segregation coefficients with an important difference in their absolute value (k_b=0.8, k_p=0.35), boron and phosphorous are not easily removable by segregation and have different segregation behavior. As a result, during the crystallization of a multi crystalline Si ingot from such a feedstock, there are 2 major consequences: firstly, similar presence of p-type and n-type dopant atoms changes the free carrier concentration and consequently the resistivity through the ingot height. Secondly, the upper part of the ingot often turns to n type, which drastically reduces the material yield i.e. furnace productivity.

However, the most important question related to this material is the compensation effect. Up to now only few studies have been devoted to the effect of dopant compensation on electrical properties. If on one hand, some studies are suggesting that compensated dopants could have a significant impact on the carrier lifetime [5], others studies are proposing that electrical compensation of boron with donors, like P could be a solution [6]. Based on this variety of results, one can imagine that there is a frontier between beneficial/detrimental effects which is still an unknown, and further investigations are required.

2. Innovative Crystallization Process

Considering the characteristics of the purified metallurgical silicon i.e. a relatively high concentration of residual impurities and a poor material yield of the ingot grown due to the n-type region a crystallization process adapted for that kind of feedstock was developed.

This innovative process is based on two important key features:

The first one is a new thermal furnace topology consisting of two independently controlled inductive heating elements below and above the crucible in combination with a lateral thermal insulation. This new thermal configuration (fig.1) is well adapted for establishing high temperature gradients (>10K/cm) and a planar solid/liquid interface, which are especially beneficial for the segregation of remaining impurities in lower quality silicon at high solidification velocities.

Figure 1: Schematic view of the principal elements of the new crystallisation furnace

The second element is a thermally anisotropic quartz crucible. Contrary to the configuration presently employed by the industry whereas the crucible bottom is characterized by an important thermal resistance (due to the low thermal conductivity of fused silica), our crucible presents an optically transparent bottom and opaque side walls. By this way, during crystallization the heat flux is easily extracted through its transparent bottom via IR radiation, whereas the opaque crucible walls support lateral thermal insulation, thus allowing application of a larger thermal gradient so higher crystallization rate. In a second aspect, the use of quartz instead

Figure 2: Photo of a 200x200x100mm^3 anisotropic quartz crucible with transparent bottom and opaque side walls.

of fused silica as crucible material drastically reduces the contamination of the ingot by solid state diffusion. Indeed, as shown in table 1 the total amount of impurities presents in quartz is much lower than in standard crucible material i.e. fused silica. This allows for improving the material yield by reducing cropping losses, since the ingot regions in contact with the crucible wall get less contaminated during crystallization.

Element	Standard Crucible	Quartz Crucible
Mg	10	0.8
Al	950	17
Ti	60	2.5
Mn	2	0.1
Fe	120	0.8
Ni	1	0.1

Table 1: Impurity concentrations in standard grade silica crucible [7], and quartz crucible (ppmw).

3. Experimental Results and Discussion

Crystallization experiments were carried out in a lab-scale furnace using the innovative crystallization process. Two ingots with different types of silicon were grown: (i) Electronic grade (EG) silicon, boron doped with a resistivity of 0.5Ωcm; (ii) Purified metallurgical Silicon (SoG) from PHOTOSIL with remaining impurities concentrations as shown in Table 2. It has to be noted that the purification results reflect an earlier status of the project. In the meantime Boron concentrations of 1 ppmw are regularly obtained.

Element	Al	B	Ca	Cr	Cu	Fe	Ni	P	Ti	V
Ppmw	<5	~2-3	8.8	2	<2	26	<2	~6-8	<1	<2

Table 2: Impurity concentrations in Photosil purified metallurgical silicon.

After crystallization, the two resulting 6 kg ingots were cut into wafers including the bottom part of the ingot, which is usually removed on standard ingots, in order to assess the level of contamination from the quartz crucible.

Fig. 3 shows the obtained efficiencies of both ingots as a function of their height. In case of the EG ingot the efficiency distribution is very uniform at a high level of 15% from the bottom to the top of the ingot. In case of the ingot from PHOTOSIL Silicon, numerous observations can be made: (i) As expected, due to the high residual concentration of phosphorous and its more efficient segregation compared to boron, the ingot turns n-

Figure 3: Solar cell efficiencies as a function of ingot position for ingots from EG Silicon and PHOTOSIL silicon.

type at around 70% of its height, from which point the solar cells efficiencies drastically drop. (ii) As with EG ingot, no significant degradation of the efficiency for solar cells from the bottom part of the ingot was observed, which confirms the interest of quartz as crucible material. Moreover, the same result can be expected from the periphery of the ingot, so a higher material yield can be

reached for ingots grown using this technique, limiting the loss due to n-type inversion; (iii) Relatively high solar cell efficiencies were obtained (14%) in the p-type region in regards to the residual impurities concentration of the feedstock, especially boron and phosphorous concentrations. More surprisingly, but not perceptible on the graph, is the fact that best solar cells (14.3%) were obtained just before the change of polarity type i.e. in the strongest compensated region.
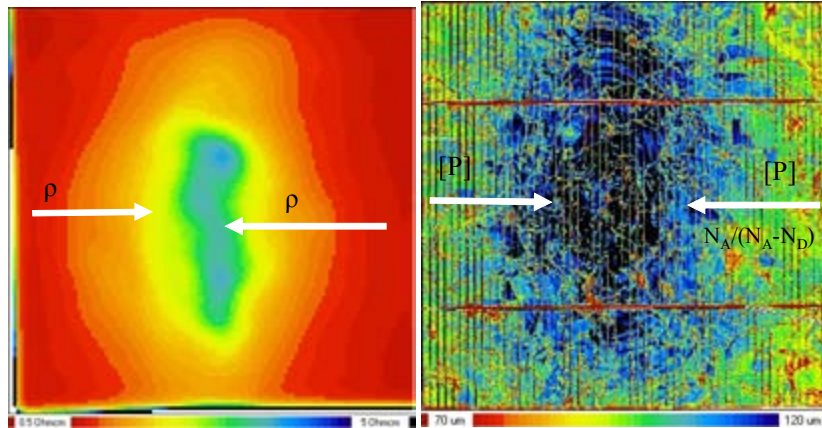
Figure 4: Resistivity (left) and Ln (right) mappings of a compensated SoG multicrystalline silicon cell.

Characterizations of wafers and solar cells were then conducted. LBIC and resistivity mappings show a perfect match between the minority carrier diffusion length Ln and resistivity (fig.4). Indeed, the higher Ln value (120μm) is located in the wafer center i.e. in the highest resistive region while the lower Ln value (75μm) is situated in the wafer edges. This observation clearly suggests that Ln increases with the degree of compensation. Chemical analyses (GDMS) realized on different regions of the wafer surface confirm this results, indicating a higher phosphorous concentration in the center than edges. (Actually this variation of concentration is due to the transport conditions of dopants in the liquid ahead of the crystallization front, which provokes phosphorous to segregate towards the center of the ingot, leading to an increase in the compensation level from the edges to the centre of the wafers.) These results show clearly the beneficial effect of compensation and allow understanding why the best solar cells are located near the inversion of polarity type.

Combining these results and numerical simulation, S. Dubois proposed a theoretical model suggesting that when carrier lifetime is limited by doping species, dopant compensation could be a convenient issue to increase solar cells performances [8].

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Dependency of Power Conversion Efficiency on Donor, Acceptor, and Blocking layer thickness for small-molecular Organic Solar Cell

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It has been reported that OPV device sandwiched with donor (CuPc), acceptor (C_{60}), and hole/exciton blocking (BCP) layer between cathode and anode has been proposed a good device to obtain maximum power conversion efficiency [1-7]. However, they did not show how the power conversion efficiency is one another influenced by the thickness of organic donor (CuPc), acceptor (C_{60}), and hole/exciton blocking (BCP) layer. In our study, thus, we investigated the impact of organic donor, acceptor, and hole/exciton blocking layer thickness on power conversion efficiency for small-molecular solar cell.
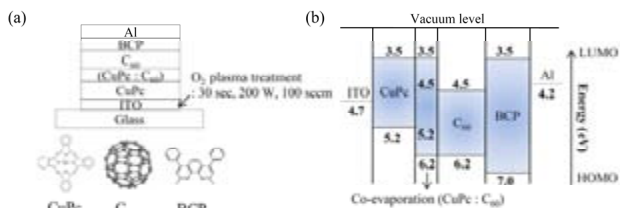
Fig. 1. Schematic structure and energy band diagram for the OPV device fabricated with a double small-molecular layer: (a) cross-sectional device structure and chemical structures, and (b) energy band diagram.

The OPV devices were fabricated with the following configuration by using a vacuum thermal evaporation: ITO glass substrate / CuPc (4.5, 8.2, 11.5, 12.7, 16.9, 17.6, 19.8, 30.1, 35, and 37.3 nm) / CuPc : C_{60} co-evaporation (interface layer; CuPc:C_{60}=2.5:1, 11 nm) / C_{60} (5.8, 8.2, 10.5, 12.8, 15.2, 17.5, 19.8, and 23 nm) / BCP (4, 8, and 12 nm) / Al (100 nm). Figure 1 shows the schematic vertical structure, chemical structures of small-molecular materials, and the energy band diagram of the OPV device.

In order to investigate the power conversion efficiency depending on the donor (CuPc) layer thickness, the OPV device was fabricated with the sandwiched structure of variable thick donor layer, fixed thick interface layer (e.q., ~11.0 nm), C_{60} layer (e.q., ~17.5 nm), and BCP layer (e.q., ~8.0 nm).

Fig. 2. Photovoltaic performance of the OPV device as a function of the CuPc layer thickness: (a) photocurrent density, and (b) power conversion efficiency.

Figure 2 shows the characteristics of OPV device fabricated with double small-molecular layer as a function of CuPc layer thickness. Figure 2(a) shows the photocurrent density versus voltage (J-V) curves for the OPV device with a various CuPc layer thickness. The J_{sc} was varied with the CuPc layer thickness while V_{oc} did not. The variation of V_{oc} was about 3.8% (from 0.515V to 0.535V). V_{oc} is determined by the energy gap between CuPc layer's highest occupied molecular orbital (HOMO) level and C_{60} layer's lowest unoccupied molecular orbital (LUMO) level, Fig. 1(b). Although, the CuPc layer thickness is varied, the energy level between CuPc layer's HOMO level and C_{60} layer's LUMO level is fixed. For this reason, the variation of V_{oc} is uniform. However, J_{sc} sharply increased with the CuPc layer thickness up to ~12.7 nm and then suddenly decreased with increasing the CuPc layer thickness. Figure 2(b) shows the dependence of power conversion efficiency on the CuPc layer thickness. The power conversion efficiency was obtained under the illumination of 100 mW/cm². The power conversion efficiency sharply increased with the CuPc layer thickness up to ~12.7 nm and then suddenly decreased with increasing the CuPc layer thickness. In comparison of V_{oc}, J_{sc}, and power conversion efficiency, it is evident that the power

conversion efficiency shows similar tendency with J_{sc} rather than V_{oc} as the CuPc layer thickness is varied. Since the J_{sc} dominantly influenced the power conversion efficiency in changing the CuPc layer thickness, the maximum power conversion efficiency (~2.5%) at a specific CuPc layer thickness (~12.7 nm) could be obtained by improving about 330%, see Figs. 2(b). Note that power conversion efficiency is obtained by multiplying J_{sc} with V_{oc}, divided by fill-factor.

This trend is probably associated with light absorption and carrier transport resistance depending on the CuPc layer thickness. Figure 3(a) shows the dependency of the light absorption. In the wavelength range of 450 ~ 550 nm, the light was almost entirely transmitted (~10% light absorption) for all thicknesses. In the wavelength range of 550 ~ 650 nm, however, the light absorption of the CuPc layer increased with the thickness.
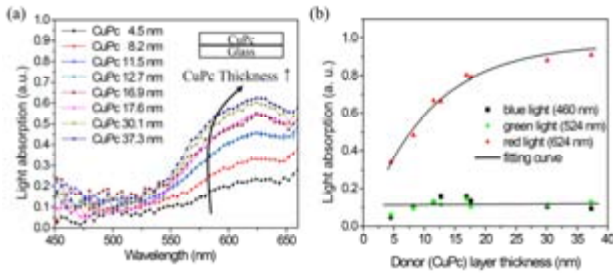
Fig. 3. Relation of the light absorption of the CuPc layer and the wavelength: (a) dependency of the light absorption on the wavelength, and (b) dependency of the light absorption on the CuPc layer thickness for blue (460 nm), green (524 nm), and red (624 nm) wavelengths.

Figure 3(b) shows the variation of the ratio of light absorption as a function of the CuPc layer thickness for red (▲: 624 nm), green (♦ : 524 nm), and blue (

■ : 460 nm) wavelengths. Even as the thickness increased, the green and blue wavelengths did not show sufficient light absorption, with absorption ratios of approximately 10%. In contrast, the light absorption for the red wavelength tended to increase with the square root of the donor layer thickness. Therefore, the light absorption is determined by

longer light wavelengths, rather than shorter wavelengths, and it increases with the CuPc layer thickness. Therefore, the light absorption current ($J_{absorption}$) of the layer can be described by [8]

$$J_{absorption} \propto C_1 \cdot e^{C_2 \cdot a}, \qquad (1)$$

where C_1 and C_2 are constants, and a is the absorption of illuminating light in the CuPc layer.

In general, the carrier transport resistance current ($J_{resistance}$) in the CuPc layer can be described by the mechanism of the space-charge limit current (SCLC). Thus, $J_{resistance}$ can be described as [9-11]

$$J_{resis\,tan\,ce} \propto C_3 \cdot \frac{1}{R^3}, \qquad (2)$$

where C_3 is a constant.

Therefore, the total short-circuit current (J_{sc}) is determined by multiplying $J_{absorption}$ and $J_{resistance}$ in the CuPc layer. Therefore, J_{sc} can be described by

$$J_{sc} = C_4 \cdot \frac{1}{R^3} \cdot e^{C_2 \cdot a}, \qquad (3)$$

where C_4 is a constant. By using equations (1), (2), and (3), $J_{absorption}$, $J_{resistance}$, and the power conversion efficiency were calculated, as shown in Fig 4(a).
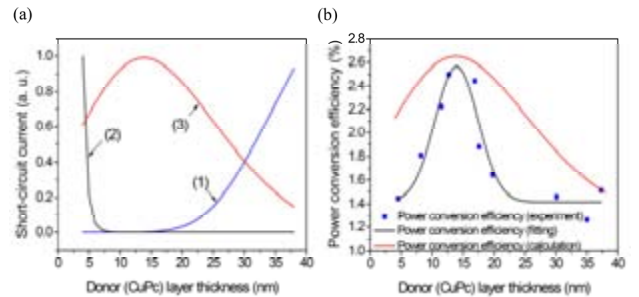
Fig. 4. Correlation of power conversion efficiency between the experimental and calculated results: (a) calculated light absorption current ((1); $J_{absorption}$), carrier transport resistance current ((2); $J_{resistance}$), and power conversion efficiency ((3)), and (b) effect of the donor layer thickness on the power conversion efficiency.

First, $J_{absorption}$, represented by line (1), increased exponentially with the CuPc layer thickness. In contrast, $J_{resistance}$, shown by line (2), abruptly decreased with increasing the thickness. As a result, the power conversion efficiency, represented by line

(3), rapidly increased with the CuPc layer thickness up to ~13 nm and then abruptly decreased beyond that thickness. The calculated and experimental plots both increased with the CuPc layer thickness up to ~13 nm and then decreased as the thickness further increased, although they did not match perfectly for all thicknesses, such as Fig. 4(b). Nevertheless, the similar tendencies of the experimentally measured and calculated values indicate that the actual power conversion efficiency is, in fact, determined by multiplying $J_{absorption}$ and $J_{resistance}$.

In order to investigate the power conversion efficiency depending on the acceptor (C_{60}) layer thickness, the OPV device was fabricated with the sandwiched structure of fixed thick CuPc layer (e.q., ~12.7 nm), interface layer (e.q., ~11 nm), variable thick C_{60} layer, and fixed thick BCP layer (e.q., ~8 nm) between anode (ITO) and cathode (Al). Figure 5(a) shows J-V curves for the OPV device depending on the C_{60} layer thickness. The J_{sc} was drastically varied with the C_{60} layer thickness while V_{oc} was slightly changed with the C_{60} layer thickness.
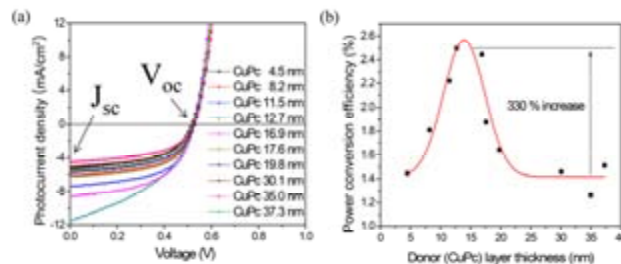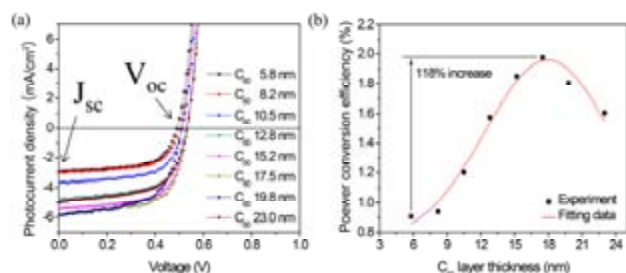

Fig. 5. Photovoltaic performance of the OPV device as a function of the C_{60} layer thickness: (a) photocurrent density, and (b) power conversion efficiency.

The variation of V_{oc} was about 8% (from 0.495 V to 0.535 V). This result indicates that V_{oc} does not significantly changed by the C_{60} layer thickness. However, J_{sc} sharply increased with the C_{60} layer thickness up to ~17.5 nm and then abruptly decreased with increasing the C_{60} layer thickness. Figure 5(b) shows the dependence of power conversion efficiency on the C_{60} layer thickness. The power conversion efficiency sharply increased with the C_{60} layer thickness up to ~17.5 nm and then

suddenly decreased with increasing the C_{60} layer thickness. In comparison of V_{oc}, J_{sc}, and power conversion efficiency, the knowledge of charge transport properties of the individual components is necessary to understand the improvement in device performance. The hole mobility of the CuPc layer has been previously reported to be ~10^{-3} cm^2/Vs while the C_{60} has been demonstrated as a high-mobility material with an electron mobility of 0.5 cm^2/Vs in the single-crystal state [9,12]. The Power conversion efficiency trend on the C_{60} layer thickness is different from the CuPc layer thickness because electron mobility of C_{60} layer is faster 100 times compared with hole mobility of CuPc layer. Therefore, the C_{60} layer needs thicker thickness than the CuPc layer thickness. In other words, unbalanced hole and electron accumulations dominantly influence the power conversion efficiency in changing the C_{60} layer thickness, the maximum power conversion efficiency (~2.0%) at a specific C_{60} layer thickness (~17.5 nm) could be obtained by improving about 118%, see Figs. 5(b).
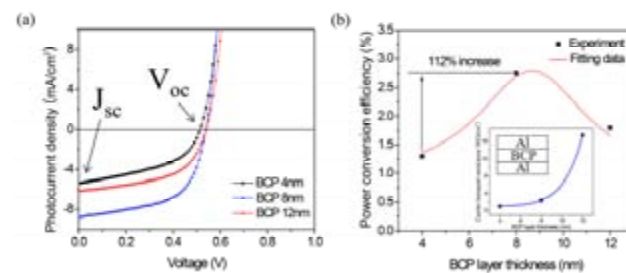
Fig. 6. Photovoltaic performance of the OPV device as a function of the BCP layer thickness: (a) photocurrent density, and (b) power conversion efficiency. Inset is carrier transport resistance on the BCP layer thickness.

In order to investigate the power conversion efficiency depending on the exciton blocking (BCP) layer thickness, the OPV device was fabricated with the sandwiched structure of fixed thickness CuPc (e.q., ~12.7 nm), interface (e.q., ~11.0 nm), C_{60} (e.q., ~18.0 nm), and variable thickness BCP layer between anode (ITO) and cathode (Al). The J_{sc} was varied with the BCP layer thickness while V_{oc} did not change significantly with the BCP layer thickness. However, J_{sc} sharply increased with the

BCP layer thickness up to ~8 nm and then abruptly decreased with increasing the BCP layer thickness. In addition, the variation of J_{sc} was about 64% (from 5.36 to 8.79 mA/cm^2) with varying the BCP layer thickness, as shown in Fig. 6(a). As a result, the maximum power conversion efficiency at a specific BCP layer thickness (~8.0 nm) could be obtained by improving about 112%, see Fig. 6(b). To understand the dependency of power conversion efficiency on the BCP layer thickness, the carrier transport resistance was measured for various BCP layer thickness, as shown inset in Fig. 6(b). The carrier transport resistance exponentially increased with the BCP layer thickness, indicating that the J_{sc} produced by electrons probably decreases with increasing the BCP layer thickness. Otherwise, generally, the blocking efficiency for exciton of the BCP layer increases with the BCP layer thickness, indicating that the J_{sc} produced by both hole and electron increases with the BCP layer thickness [13]. Thus, there is a trade-off between the carrier transport resistance and the blocking efficiency for exciton of the BCP layer as the BCP layer thickness changes. The maximum J_{sc} could be obtained at a specific BCP layer thickness (~8.0 nm), resulting in the maximum power conversion efficiency (~2.8%).

In summary, the OPV devices fabricated with double small-molecular layers, the dependency of the power conversion efficiency on the donor (CuPc) layer, acceptor (C_{60}) layer, and exciton blocking (BCP) layer thickness were investigated. The power conversion efficiency peaks at the CuPc thickness of ~12.7 nm by improving about 330%. In addition, the power conversion efficiency peaks at the C_{60} thickness of ~17.5 nm by improving about 118%. Furthermore, the power conversion efficiency peaks at the BCP layer thickness of ~8.0 nm by improving about 112%. The effect of donor, acceptor, and exciton layer thickness on power conversion efficiency is determined by the change of J_{sc} rather than V_{oc}. All thickness of donor, acceptor, and exciton layer influences J_{sc} while V_{oc} is mainly determined by the energy gap between donor layer's HOMO level and acceptor layer's LUMO level. In addition, the CuPc layer thickness showing the

maximum power conversion efficiency, ~12.7 nm, is thinner than the C_{60} layer thickness, ~17.5 nm. This difference is probably associated with the difference of carrier mobility and the wavelength of absorbed light. Therefore, for the OPV devices fabricated with small-molecular double layer the thickness optimization of donor, acceptor, and exciton layer and choice of donor layer material having higher generation rate of exciton after light absorption would be a key engineering to obtain the maximum power conversion efficiency.

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Crystalline Silicon – Using Experience and Scale to Accelerate Cost Reduction Ahead of Thin Film PV

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(Paper not available)

SiGen's Kerf-free Wafering Equipment

Zuquin Liu
SiGen

(Paper Not Available)

Surface Preparation Chemistry for Solar Cell Manufacturing

Douglas Caskey

JT Baker

Abstract

Due to the use of thinner and larger wafers, in-line belt diffusion becomes more commonly used in new multi crystalline silicon solar cell production lines. In this presentation, an adjustment to the processing sequence with in-line belt diffusion is discussed. A simple surface cleaning before SiN_x:H ARC deposition results in better surface passivation and an additional absolute efficiency gain of 0.3%.

Alagu Thenappan
Honeywell

(Paper not available)

Three-Dimensional Analysis of Defects and Quantitative Analysis of Impurities in Multicrystalline Silicon by Photoluminescence

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Abstract

The photoluminescence (PL) technique has been used to analyze electrically active defects and impurities in multicrystalline silicon (mc-Si) for solar cells. PL imaging during HF etching has the advantage of very rapid detection of defects, which allows us to obtain numerous successive PL images of wafers positioned from the bottom to top of the mc-Si ingots, as well as to synthesize the three-dimensional distribution of the defects from the images. We showed the multiplication of dislocation clusters and their interaction with grain boundaries. The spectroscopic analysis of free and impurity-bound exciton luminescence at liquid He temperature enabled us to determine the impurity concentrations in LSI-grade Si, which has been standardized and used worldwide. We changed the excitation intensity condition to extend the concentration range to 1×10^{13} - 1×10^{17} cm^{-3} for the analysis of solar-grade mc-Si. Satisfactory agreement was obtained among PL, secondary ion mass spectroscopy and inductively coupled plasma mass spectroscopy.

1. Introduction

The production of high efficiency solar cells without using high quality polycrystalline Si is indispensable to solve current environmental and energy issues. Solar-grade Si substrates contain higher concentrations of defects and impurities than LSI-grade Si substrates. The analysis of defects and impurities is essential to improve the conversion efficiency of solar cells, and is also quite effective to reduce their production cost. We have characterized the electrically active defects and impurities in both LSI-grade and solar-grade Si by photoluminescence (PL). In this paper we report on our recent progress of PL characterizaion of defects and impurities in solar-grade Si. We demonstrate the visualization of three-dimensional distribution of electrically active grain boundaries and dislocation clusters in mc-Si ingots. A new quantitative method is proposed for determination of donor and acceptor impurities in the concentration range between 1×10^{13} and 1×10^{17} cm^{-3}.

2. Three-Dimensional Analysis of Defects

2.1 Defects in mc-Si

The intra-grain defects in mc-Si crystals have been successfully detected by the PL technique thanks to its great advantages of high sensitivity, high spatial resolution, high speed, noncontact and nondestructiveness [1-6]. Dark PL patterns were observed in the short lifetime region by PL mapping and imaging, and the defects responsible for these patterns were regarded as a serious obstacle to attaining high conversion efficiency. One-to-one correspondences among the PL, crystallographic-misorientation and etch-pit patterns led us to conclude that the defects are dislocation clusters which form subgrain boundaries [4] and that they act as preferential precipitation sites for not only heavy-metal but also oxygen impurities [6]. We synthesized the 3D distribution of the defects from numerous successive PL images of the wafers positioned from the bottom to top of the mc-Si ingots.

2.2 PL imaging during HF etching

The PL imaging apparatus is shown schematically in Fig. 1 [5]. We used high power light-emitting-diode arrays with a wavelength of 500 nm as an excitation source and a cooled charge-coupled device camera as a PL detector. The band-edge PL emission was extracted by band-pass filters, and the PL imaging was performed while the sample was immersed in 5 % HF solution. The native oxide film of the samples was removed by the HF etching, through which the surface recombination velocity was reduced from about 10,000 to less than 10 cm·s^{-1} [7]. The measurement time and spatial resolution of the present technique is about ten thousand times faster and ten times higher than the conventional microwave photoconductivity decay measurement (μPCD), as shown in Fig. 2.
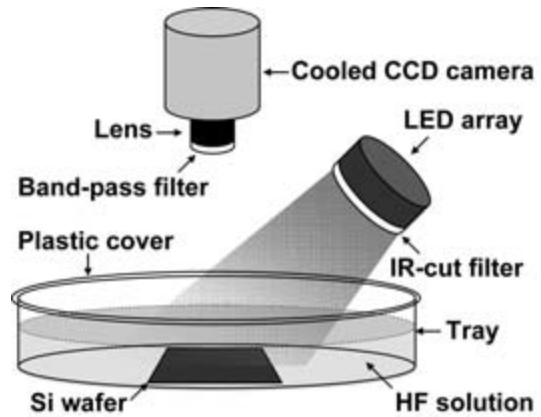
Fig. 1. Schematic illustration of PL imaging apparatus. PL imaging was performed during wafer etching with HF.

2.3 Three-dimensional distribution of defects

We measured succesive PL images of the wafers sliced perpendicular to the growth direction from the n-type mc-Si ingot which had an area of 180 x 180 mm^2 and a height of 120 mm and had a resistivity ranging from about 1 to 10 Ω·cm. Part of the successive PL images of the wafers with a size of 40 x 40 mm^2 and a thickness of 350 μm are shown in Fig. 3, where the height position of the wafer is (a) 40.5, (b) 55.5, (c) 60.5, and (d) 70.5 mm from the bottom. Dark tangled lines marked A, B and C in Fig. 3(a) are due to a high density of dislocation clusters, while distinctive dark lines are due to electrically active grain boundaries. It should be noted that the dislocation clusters B were taken into the grain boundaries, and that the clusters A and C were multiplied with solidification.
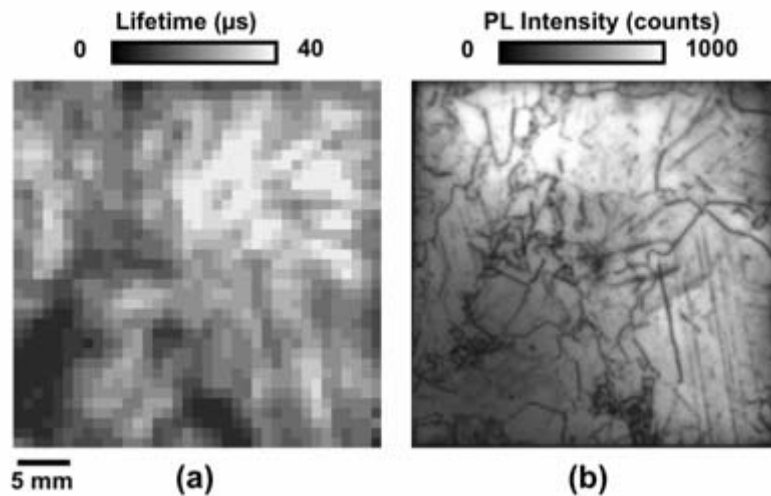
Fig. 2. Comparison of defect detection capabilities in mc-Si between (a) μPCD and (b) PL. Measurement time and spatial resolution are (a) 20 min and 1 mm, and (b) 0.1 s and 100 μm, respectively. Whiter regions indicate higher PL intensity and longer lifetime regions.

(d)

(c)

(b)

A

B

(a)

C

10 mm
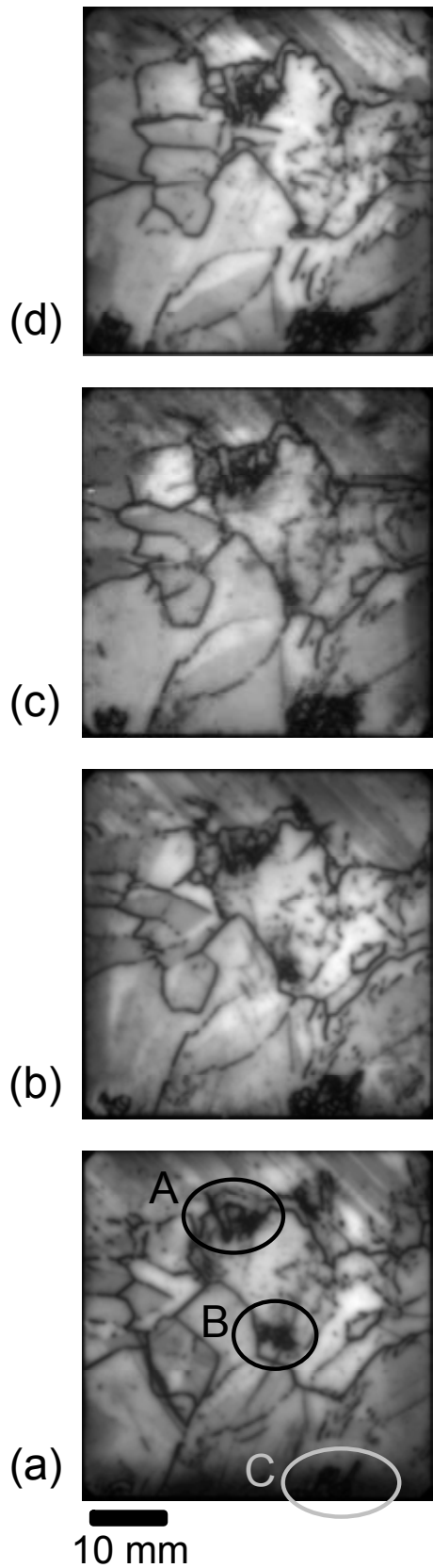
Fig. 3. Successive PL images of wafers sliced
from n-type mc-Si ingot at a height of (a)
40.5, (b) 55.5, (c) 60.5, and (d) 70.5 mm
from the bottom. The total height of the
ingot was 120 mm.

0   25000
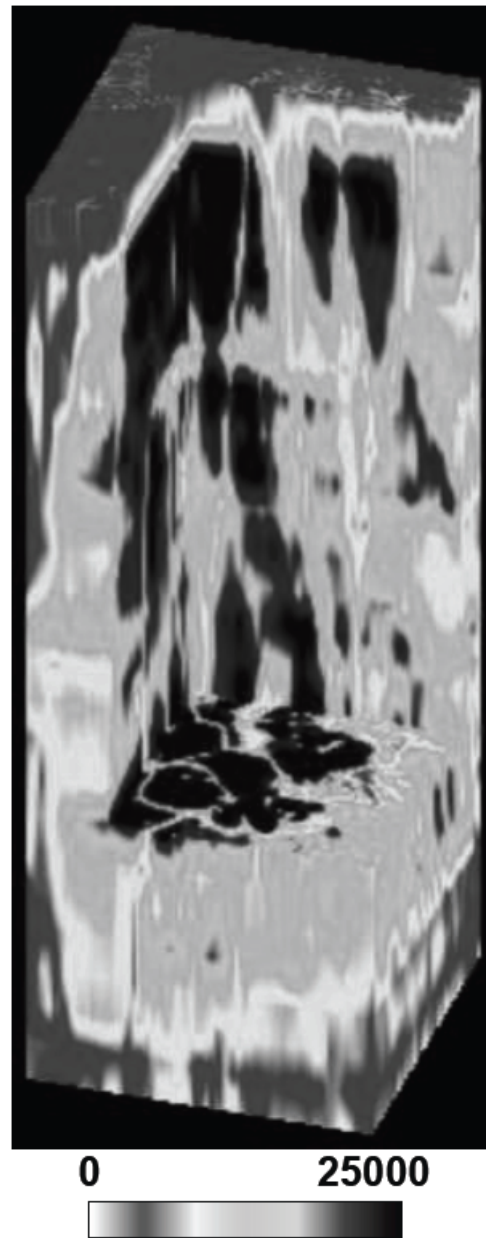
Fig. 4. 3D distribution of electrically active
defects in mc-Si ingot synthesized from
successive PL images partly shown in Fig. 3.
The size of the block is $40 \times 40 \times 120$ mm^3.
This image is originally diplayed with a
color scale.

35

We synthesized the 3D distribution of electrically active defects from the succesive images, as shown in Fig. 4. The rapid generation of dislocation clusters and their interaction with grain boundaries are clearly depicted. We believe the information obtained from the present technique should be quite helpful in controlling electrically active defects in mc-Si.

3. Quantitative Impurity Analysis

3.1 Impurity analysis for solar-grade Si

The concentrations of the residual donor and acceptor impurities in the low-cost solar-grade polycrystalline Si are on the order of 10^{15} to 10^{17} cm^{-3}. It has been reported that PL spectroscopy enables us to identify the species of donor and acceptor impurities and determine their respective concentrations in the range from 5×10^{10} to 1×10^{15} cm^{-3} in LSI-grade Si. This method was standardized by the Japanese Industrial Standard (JIS) and Semiconductor Equipment and Materials International (SEMI) and is still widely used [8,9]. In this technique, the ratio between impurity-bound exciton (BE) and free exciton (FE) luminescence intensities is used as a measure of the impurity concentration [10,11]. However, the method was rarely applicable to the donor and acceptor impurities in a concentration range higher than 1×10^{15} cm^{-3}, because the FE line was almost undetectable.

We focused on the phenomenon that the FE line increases with the excitation intensity with a higher rate than the BE line. The appropriate excitation power was adjusted for observations of the BE line and the FE line in the higher impurity concentration range. Thus, we could make calibration curves for the determination of the B and P concentrations in the range from 1×10^{13} to 1×10^{17} cm^{-3} from the intensity ratio of the BE to FE line.
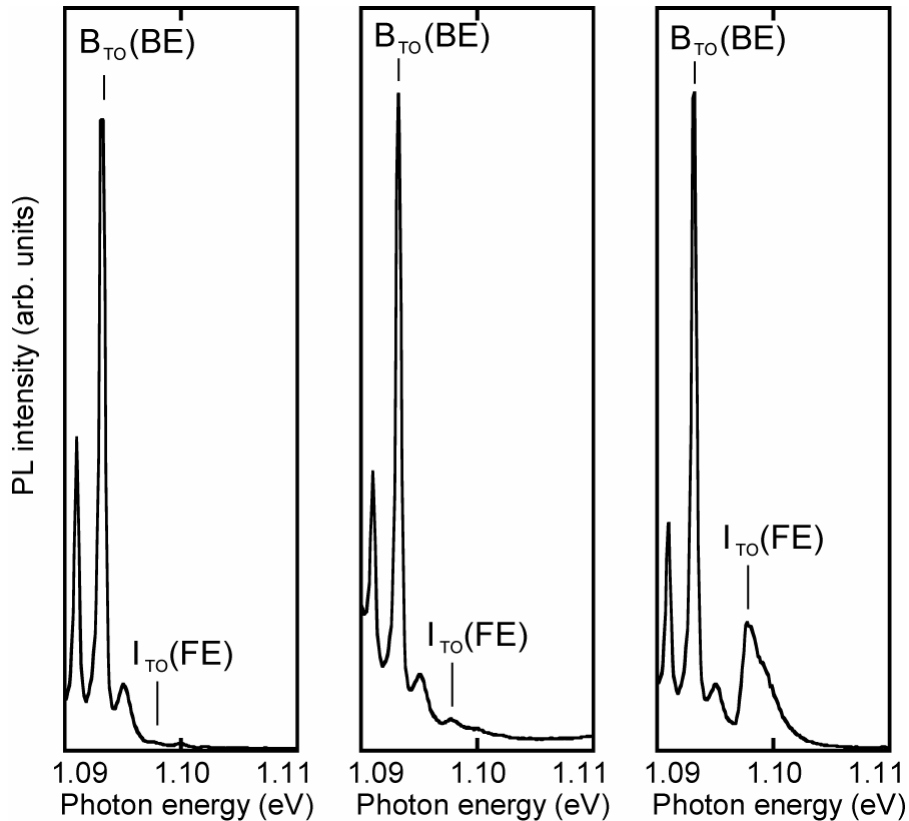
Fig. 5. Variation of PL spectra of B-doped Si with a concentration of 8×10^{15} cm^{-3} by change in excitation power of 3 mm diam laser spot: (a) 50 mW, (b) 500 mW, and (c) 1000 mW.

3.2 Samples and experimental technique

The samples used for the experiment were B-doped p-type and P-doped n-type single crystalline Si wafers commercially grown by the float-zone and Czochralski methods. The residual compensating impurities were expected to be low, which was confirmed by the present PL technique as discussed later. The net carrier concentrations in the samples, $|N_D - N_A|$, (N_D: donor concentration, N_A: acceptor concentration), were determined from the conventional resistivity measurement with the aid of the Irvin curve [12]. We assumed that $|N_D - N_A|$ of p-type Si was equal to the B concentration and that of n-type Si was equal to the P concentration.

PL measurements were performed on the etched surface of the samples which were immersed in liquid He. The luminescence excited by the 532 nm line of Nd: YVO_4 laser was analyzed with a monochromator (Photon design PDP320: $f = 0.32$ m) with a 600 groove/mm grating blazed at 1.0 μm and detected by a cooled InGaAs photodiode array. The excitation power was varied from 50 to 1000 mW with the laser beam diameter of about 3 mm, where the 50 mW power with 3 mm beam diameter was the standard condition settled by JIS. Other details of the experimental method are described in JIS and SEMI [8,9].

Fig. 6. Excitation power dependence of BE and FE luminescence intensities in the same B-doped Si as Fig. 5 at 4.2 K.

3.3 Calibration curves for B and P in 1×10^{13} - 1×10^{17} cm^{-3} range

The PL spectra of a B-doped sample with a concentration of 8×10^{15} cm^{-3} at liquid He temperature under various excitation-power conditions are shown Fig. 5, where the condition of (a) is the standard condition of 50 mW settled by JIS, and that of (b) and (c) are higher excitation conditions of 500 and 1000 mW, respectively. The notations of I_{TO}(FE) and B_{TO}(BE) are TO-phonon sideband of the FE luminescence and that of the BE luminescence due to B, respectively [10]. The I_{TO}(FE) line is almost buried in the background emission in Fig. 5(a), while the line can be clearly observed in Figs. 5(b) and 5(c). Figure 6 shows the relationship between the excitation power and the PL intensities of the BE line and the FE line. We determined the excitation power to be 500 mW for the quantitative analysis.

We analyzed the B-doped and P-doped samples by the PL method under 500 mW excitations and plotted the ratios of B_{TO}(BE)/I_{TO}(FE) and P_{TO}(BE)/I_{TO}(FE) against the B and P concentrations on a log-log scale, as shown in Fig. 7. The data points lie nearly on a straight line; therefore, we can use the lines as calibration curves for determining the B and P concentrations from the PL intensity ratio. The discrepancies of the data points from the straight lines were larger under the excitation power of 1000 mW (not shown in this paper). However, the 1000 mW excitation enhanced the FE line, which enabled us to determine higher concentrations of B and P. The large discrepancies under the 1000 mW excitation condition were caused primarily by heating of the samples, as suggested from the broadening of the FE line in Fig. 5(c)

We measured the BE/FE ratios of these samples three times in order to estimate the

measurement error.   The errors under the 500 and 1000 mW excitations were estimated to be about ±50 and ±90 %, respectively.   We also examined the degree of compensation in the B-doped and P-doped samples by determining the compensating P and B impurities, respectively, using our calibration curves.   The compensation ratios of the samples were less than 1/100. Therefore, we are confident that the $|N_D - N_A|$ value is essentially equal to N_A or N_D, namely, the B or P concentration, respectively.   We have already made preliminary calibration curves for Al and As impurities, which will be reported in a separate paper

3.4 Comparison of PL with SIMS and ICP-MS

We applied practically the PL method to the quantitative analysis of residual donor and acceptor impurities in mc-Si wafers for solar cells.   In order to check the validity of the present PL method we performed secondary ion mass spectroscopy (SIMS) and inductively coupled plasma mass spectroscopy (ICP-MS) for comparison purposes.   The B concentration in the
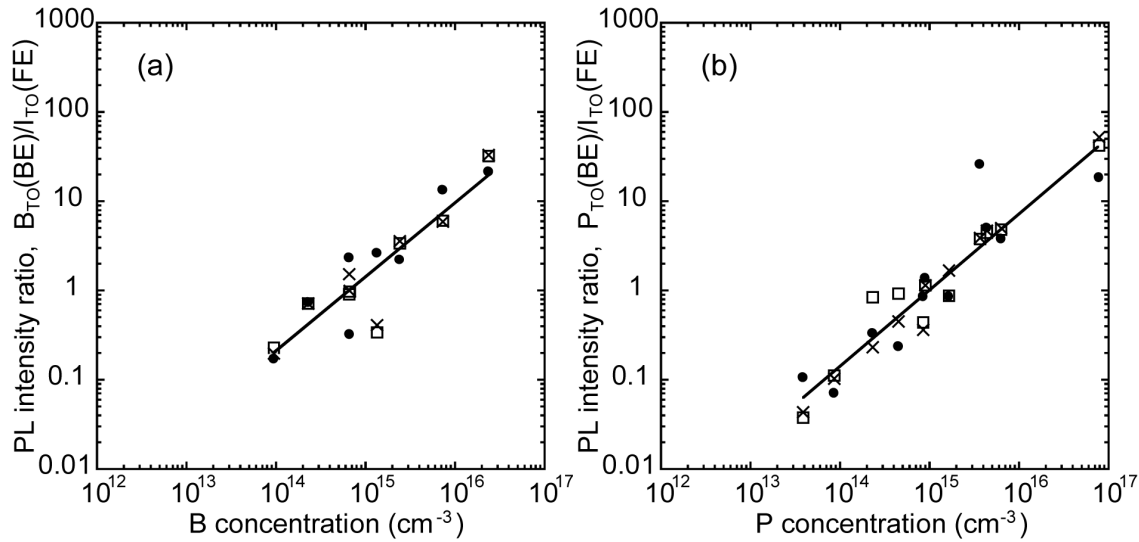
Fig. 7.   Calibration curves for (a) B and (b) P in Si for the PL method under 500 mW excitation power at 3 mm diam laser spot.
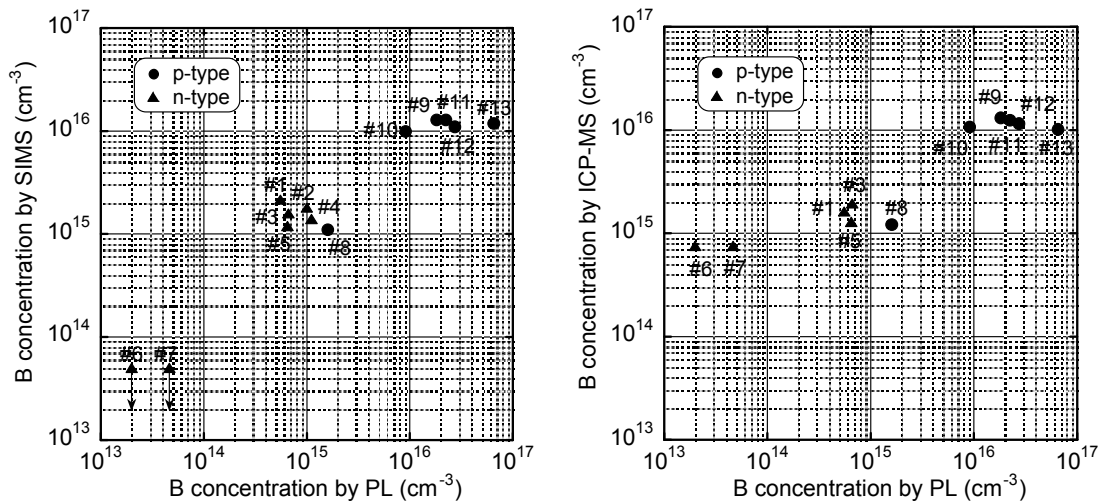
Fig. 8.   Comparison of B concentration in mc-Si wafers between (a) PL and SIMS measurements and (b) PL and ICP-MS measurements.

mc-Si wafers was compared between the PL and SIMS measurements and between PL and ICP-MS measurements, as shown in Fig. 8(a) and (b), respectively.   Satisfactory agreement was obtained among the PL, SIMS and ICP-MS data in the concentration range between 1×10^{14} and 2×10^{16} cm^{-3}; the correlation between PL and SIMS was superior to that between PL and ICP-MS. Although the deviation of the PL data in the higher concentration range is due to the error in measuring the weak FE line, we believe that the PL data is most accurate in the lower concentration range.

4. Conclusions

We used PL imaging during HF etching to analyze the 3D distribution of electrically active grain boundaries and dislocation clusters in mc-Si ingots.   The dislocation clusters were multiplied with solidification as expected, while some of them were taken into the grain boundaries during the growth.   To the best of our knowledge this is the first clear observation of the 3D movement of dislocations in mc-Si crystals.   The standardized PL method for the determination of donor and acceptor impurity concentrations was extended to the concentration range of 1×10^{13} - 1×10^{17} cm^{-3} to analyze the residual impurities in solar-grade Si.   Satisfactory agreement was obtained among the PL, SIMS and ICP-MS data in the concentration range between 1×10^{14} and 2×10^{16} cm^{-3}.

Acknowledgements

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Correlation of Defects with Cell Performance using PVSCAN

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ABSTRACT

Crystalline silicon solar cells have been the main stay of the photovoltaic industry. Both monocrystalline and multicrystalline silicon technologies are being used in production. It is important that further improvements in device performance be pursued and this is possible using an areal review of defects/impurities in silicon wafers and correlating the data with cell performance parameters. This work utilizes the PVSCAN data to show good correlation of average dislocation density with average cell efficiency and compares the areal distribution of dislocation density with LBIC scans of adjoining wafers from a multicrystalline silicon brick.

INTRODUCTION

Crystalline silicon solar cells comprised more than 87% of commercially produced photovoltaic (PV) modules during 2007[1]. Multi-crystalline silicon (mc-Si) has been an increasingly important material for the manufacture of cells due to ease of production and lower costs. Solar conversion efficiencies of mc-Si cells are typically lower than monocrystalline silicon due to larger minority carrier recombination at the grain boundaries and presence of dislocation defects [2]. Dislocations can also be precipitation sites for metal impurities and cannot be easily passivated and thereby limit cell efficiency. The effect of dislocations on cell efficiency has been discussed for a long time but very limited direct measurements of this correlation has been performed until recently when areal mapping of adjacent wafers has become possible using the PVSCAN.

BACKROUND

The concept of the PVSCAN was developed at the National Renewable Energy Laboratory(NREL) [3]. GT Solar Incorporated further developed technology and manufactured this equipment into an industrial unit. As the name implies, the PVSCAN is a photovoltaic metrology tool capable of measuring multiple material properties including reflectivity and dislocation density. The PVSCAN utilizes an XY Stage to raster a cell beneath a stationary optics assembly. Laser emission at either 632nm or 980nm can be utilized to examine surface or bulk material properties respectively [4].

For dislocation density measurements, the silicon wafer must be prepared by mechanically polishing the surface of the silicon and then etching to expose the dislocations [5]. An optical integrating sphere collects laser emissions that are scattered by dislocations. The ratio of scattered light to specular reflected light varies linearly with the density of dislocations at the surface and this is captured quantitatively by the PVSCAN.

EXPERIMENTAL RESULTS

A typical mc-silicon ingot 69-cm square cross section, 240-kg, manufactured at the REC ScanWafer facility using an ALD furnace, was used for characterization in this project. The ingot was sawn into sixteen 156cmx156cm bricks using production processing. One brick was selected from the center of the ingot and sawn into approximately 600 wafers 200 um thick. Some of the wafers were processed into solar cells and the position of the wafers within the brick was retained. Cell efficiency was monitored along the height of the brick. Seven wafers were selected from various positions in the brick. These wafers were mechanically polished and subsequently etched using Sopori etchant [5]. The 7 wafers were scanned for dislocation density using the PVSCAN. Data was collected in 200um step sizes and the average dislocation density for the entire cell was recorded.

Figure 1 shows the data that resulted from this experimentation. Plotted are average dislocation densities for the seven selected wafers as a function of cell position in the brick where cell position zero is the cell closest to the bottom of the crucible. Solar cell efficiencies of wafers adjacent to the seven wafers characterized for dislocation density are also shown in Figure 1. In this particular brick, the central region exhibits greater dislocation density compared to wafers on the ends. A corresponding efficiency loss is seen from those cells manufactured from the central region of the brick. As seen by the data, an inverse correlation is evident between dislocation density and cell efficiency; generally wafers with higher dislocation density exhibit lower cell efficiencies.

Figures 2,3 and 4 show three sets of LBIC and dislocation density maps performed on cells on wafers adjacent in position to the cells. In figure 2, the dislocation density map of wafer #185 shows regions of higher dislocation densities. Sections labeled A and B correspond to higher dislocations and correlate well in shape and location to regions of reduced LBIC response observed for adjacent wafer # 186 in the LBIC map; these areas will exhibit lower cell efficiency. Similar patterns are evident in figures 3 and 4 in which areas possessing high dislocations correlate to low cell efficiency. The parallel vertical stripes seen in the LBIC maps represent the bus bars on the manufactured cells and respond appropriately with essentially no measured cell efficiency in those areas.

Figure 5 exhibits metal contamination as a function of position within the brick. These values were gathered by MURR Nuclear Analysis [6]. As is evident from this plot, metal contamination concentrations are low and do not explain the variation of cell efficiency across the brick. In addition, most contamination densities fall below $1x10^{14}cm^{-3}$ validating that this material possesses relatively low levels of contaminants. Contamination levels were also

measured for Au, Co, Ir, La, Sb, and Zn, but their values were typically less than $1\times10^{10}cm^3$ and were not shown in the plot to maintain clarity.

CONCLUSIONS

The PVSCAN instrument, conceived by the National Renewable Energy Laboratory and developed into an industrial unit by GT Solar, is a strong characterization tool which gives areal mapping of dislocation density of silicon wafers. This data has shown very good correlation of dislocation density measurements with cell efficiency. Adjacent wafers were examined with the same brick, one for dislocation density, and the other manufactured into a cell and measured for efficiency and mapped using LBIC technique. Both quantitative average measurement across the entire wafer or cell and qualitative wafer and cell map examination exhibit an inversely proportional relationship between dislocation density and cell efficiency. MURR Nuclear Analysis measurements were conducted on samples to confirm that metal contamination did not degrade solar cell efficiencies. Such PVSCAN data can be used to optimize performance of solar cells as well as target high defect density areas of wafers for passivation/gettering treatments and thereby produce higher efficiency solar cells.
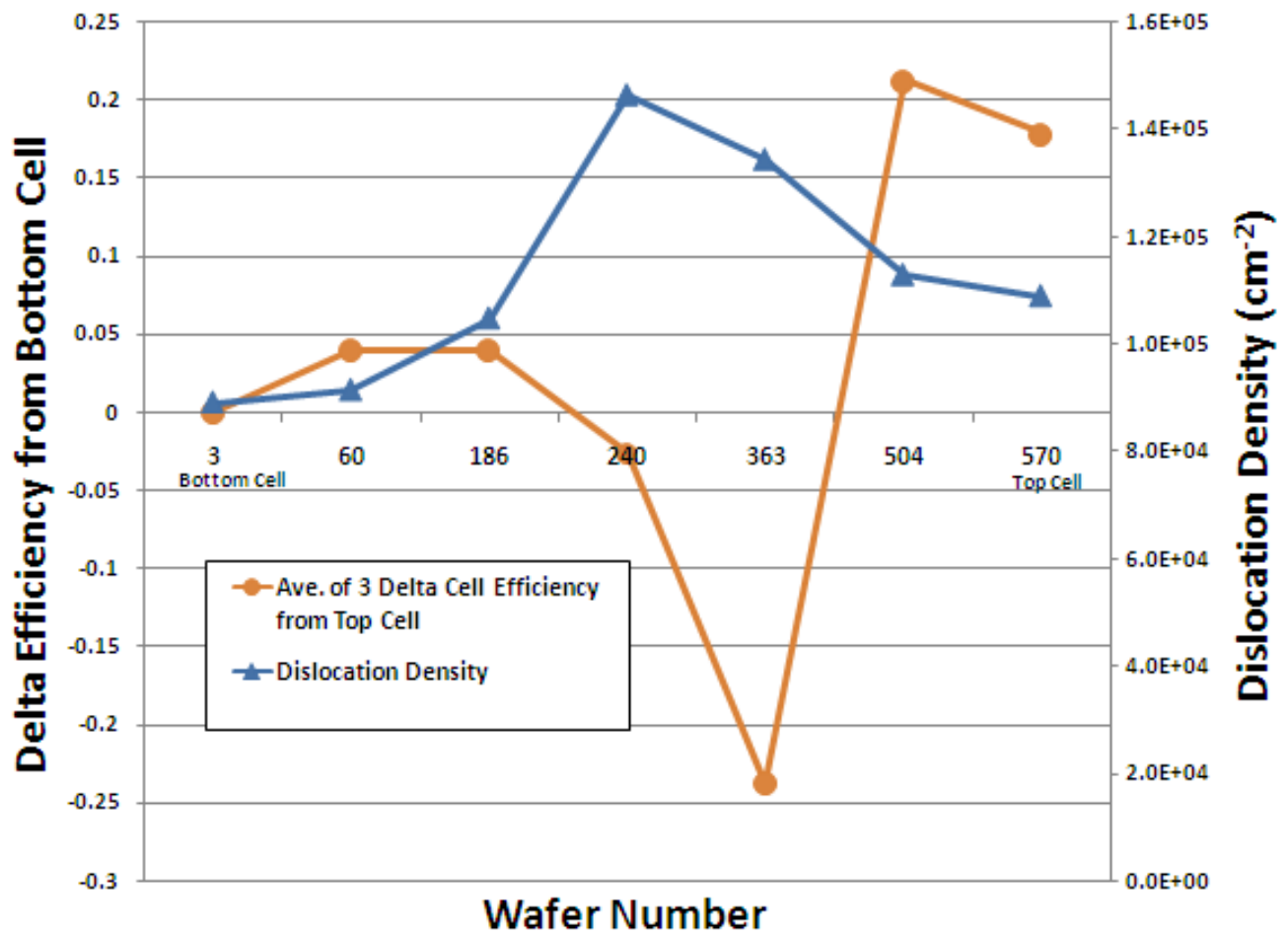
Figure 1. Solar cell variation and average dislocation density, as measured by PVSCAN, as a function of height for a brick from a 69-cm square cross section multicrystalline silicon ingot.
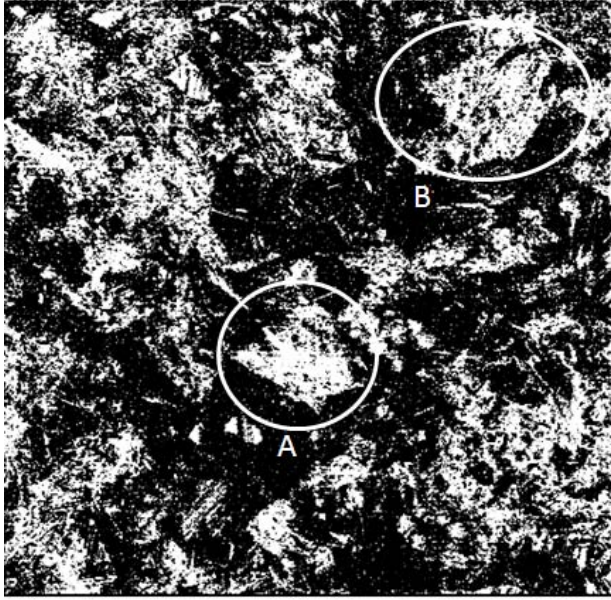
Wafer #185 Dislocation Map   Wafer #186 LBIC Map
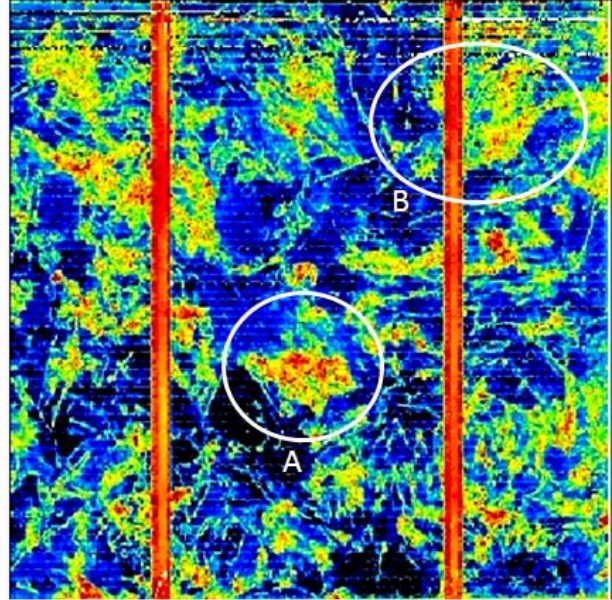
Figure 2. Areal mapping of two adjacent wafers for dislocation density and LBIC output after processing into solar cell.   Areas A and B corresponding to high dislocation density and shown to have a corresponding LBIC response.
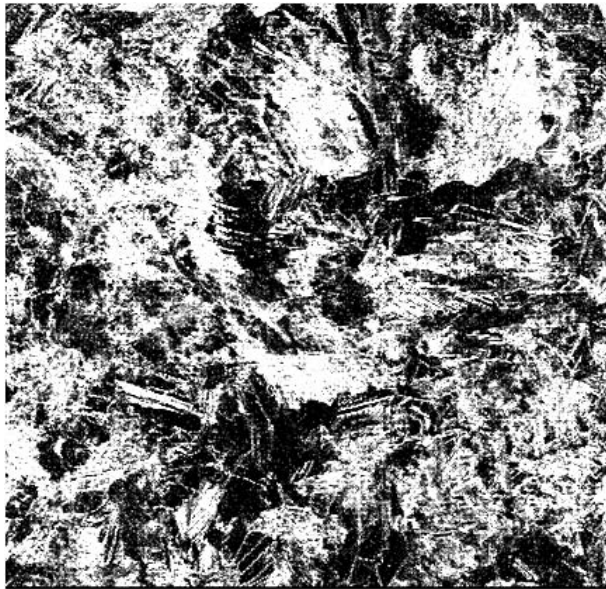
Wafer #240 Dislocation Map   Wafer #239 LBIC Map
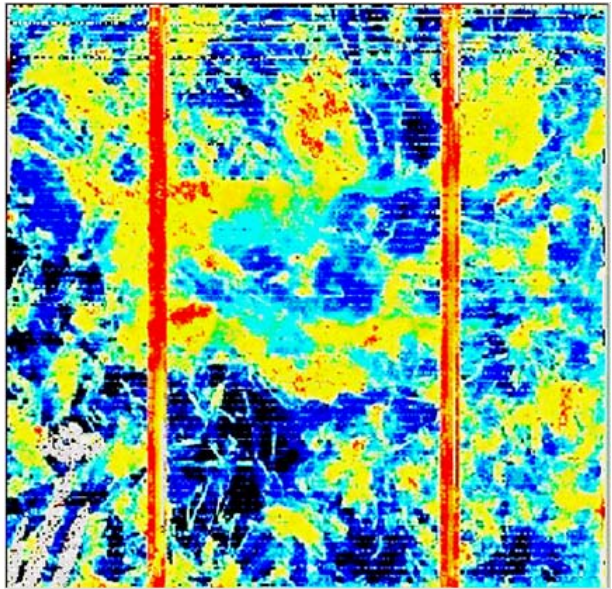
Figure 3. Correlation of two adjacent wafers for dislocation density and LBIC response showing similar correspondence.

Wafer #363 Dislocation Map

Wafer #362 LBIC Map
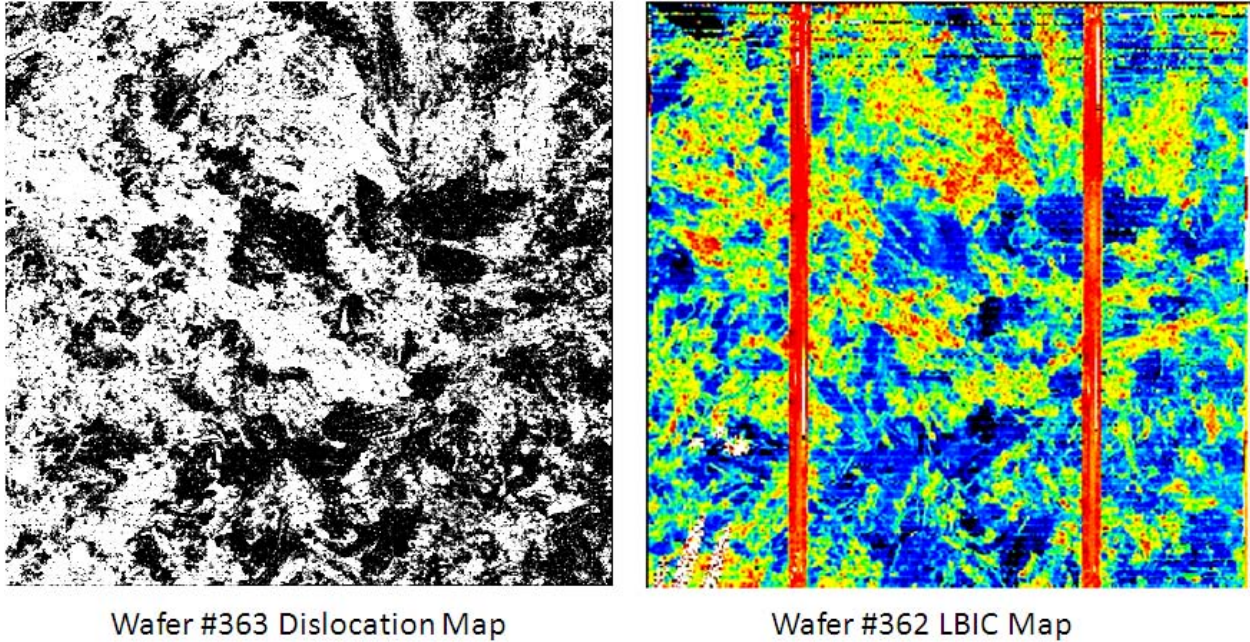
Figure 4. Comparison of two adjacent wafers showing correlation of dislocation density and LBIC response.
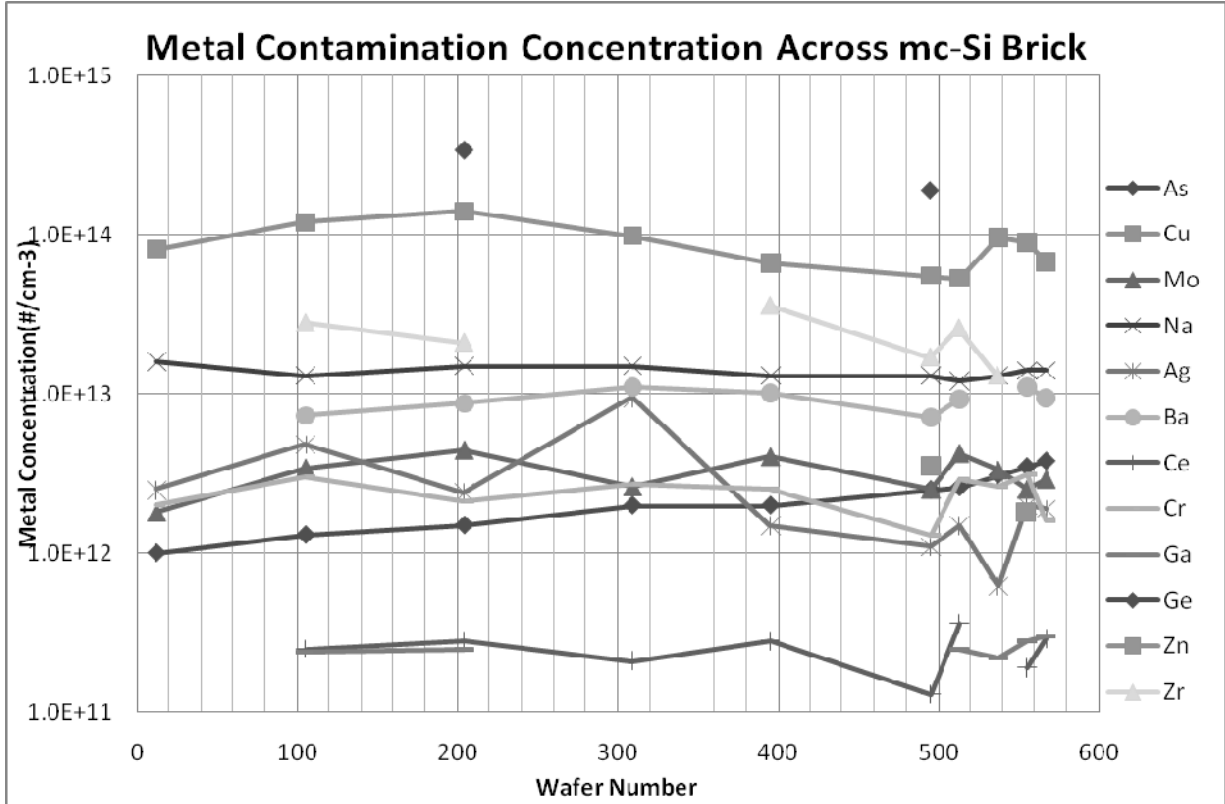
Figure 5. MURR Nuclear Analysis for metal contamination as a function of height within the brick showing that the contamination level is low and almost uniform as a function of position.

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Iron in Si: the visible, the hidden, and the (partially) passivated

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Interstitial Fe (Fe_i) and the iron-boron pair ($\{Fe_iB_s\}$) are undesirable recombination centers. Numerous attempts at gettering and passivation have produced mixed results. For the past couple of years, we have been performing systematic first-principles calculations of Fe-related defects in Si. We have considered a wide range of interactions involving Fe and impurities (H, B, C, O, etc.) or native defects (vacancy, divacancy, self-interstitial). The goal is to identify and characterize the most stable complexes containing Fe, and predict their electrical activity. Over 30 Fe-related defects have been considered so far, and this work is being extended to other transition metals.

In this talk, I will discuss the interactions between H and Fe_i and $\{Fe_iB_s\}$, and show that hydrogen not only fails to passivate these centers, but makes things worse. Then, I will show that vacancies react much more energetically with Fe than H does, and that injecting vacancies does partially passivate these centers. These predictions suggest that some surface treatments and/or high-temperature anneals (SiN_x process, metallization, etc.) could increase minority carrier lifetimes via the unavoidable (but often ignored) injection of vacancies, thus removing the deep donor levels associated with Fe_i and $\{Fe_iB_s\}$. I will conclude with preliminary results of similar studies with Ni and Ti.

PV Silicon Cell Warpage Measurement and Analysis

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Overview: Two core areas of expected application need are warpage/flatness measurement of thick film silicon substrates and measurement and analysis of surface features known as saw marks. Silicon represents the basis upon which PV materials are deposited and structures are created to complete a solar cell. Cells are then attached to glass panels and linked together (electrically) to produce a solar/PV panel. A flat silicon substrate is of value to the PV producers from both a handling and material-printing process perspective. Non-flat silicon substrates indicate higher residual stresses in the mono or poly crystalline grain structures. When these non-flat substrates are handled in production, they are far more likely to fail due to crack propagation. When non-flat substrates are processed, mechanical forces (i.e. screen printing) can cause any micro cracks to propagate to the point of failure during the processing.

Moiré image- 140,000 data points on 156mm cell

Even a flat wafer can have surface features that reduce its strength and impede the ability of an automated process to correctly deposit films/materials at the appropriate thicknesses as well as achieve desired adhesion levels. Saw marks occur during wire saw cutting of silicon wafers. When the high speed wire saw rotates during cutting, it can leave a 'peak' or 'valley' in the surface of the wafer. The magnitude of such displacements is often on the order of 5-25 microns.

Akrometrix' shadow moiré technique has been shown to be able to measure both wafer warp and saw mark surface features with a single, full-field data acquisition. Speeds of up to 1 wafer per second are obtainable. Software algorithms are able to analyze and sort wafers on varying degrees of magnitude for optimal pre-process decision making by a PV cell processor.
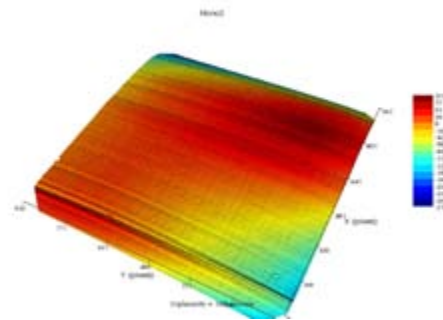
3D plotting of 156mm poly crystalline cell

Shadow moiré technique can be combined with dynamic temperature profiling (-55 C to 300 C +) to evaluate in-situ (thermal processing, operating environments, temp cycling) mechanical behaviors for process optimization and reliability assessment.

It is expected that thinner and larger silicon substrate drivers will create heightened mechanical characterization needs for the industry.
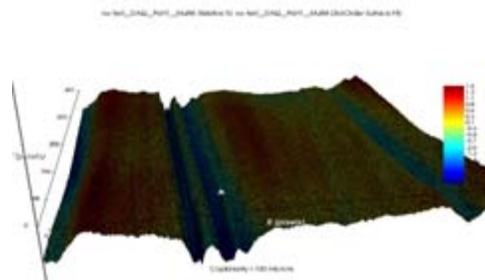
Surface analysis of 25um saw mark on poly cell

Analytical Techniques for PV Si Feedstock Evaluation

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Introduction, background, caveats, and cautions

This paper is an overview of analytical techniques for evaluating silicon solid material that is used to manufacture crystalline or micro-crystalline silicon solar cells. In any overview of a technical field, the author's experience and expertise leads to emphasis on some topics, less on others and benign neglect on some. I claim nothing less. I worked for some years as a senior research group leader for analytics in a silicon substrate company (the predecessor to MEMC), and for many years in managing instrumental analytics as a commercial service business at the Evans Analytical Group (previously known as Charles Evans & Associates). As such I do not have expertise on the use of wet chemistry or optical/electrical characterization techniques for silicon. I also have been active for many years in the development of ASTM and SEMI test methods in the area of silicon, but again related to instrumental analytics, and I am presently Chair of the EU PV Analytical Task Force and Co-Chair of the North American PV Analytical Task Force, both under SEMI Standards. This experience emphasizes test methods and techniques that can be used in the commercial world of industry, and de-emphasizes innovative analytics that may not have reach commercialization (for example, in universities or research institutes.)

Before delving into specific analytical techniques, it is important to understand that an analytical technique that is used in the commercial materials world is only part of the problem of evaluating silicon feedstock. *Representative* sampling (cf. ASTM Practice E 122, ANSI/ASQC Z1.4-1993) and process stability of the silicon feedstock are also part of the problem, and a procedure to validate the measurement capability (SEMI E89), statistical process control of the total measurement, and the effects on costs (SEMI M56-0307) are also critical. None of these issues are simple.

One last caveat – there is no clear definition in the PV industry on what defines PV Si Feedstock (or Solar Grade Silicon), and various analytics may or may not be appropriate depending up how one makes that definition. There are even loosely termed "grades" of solar grade silicon. The PV industry, as it stands today, is a very new industry, and as such there is much unknown, some would call chaos. But it is producing product which is being used worldwide. This is what we, as analysts, have to work with today.

What needs to be evaluated in Feedstock Evaluation?

The answer to this is universally (to my knowledge) – impurities, and "elemental" impurities, not impurities in compounds or various chemical states. The reason for this is that PV Si feedstock is converted into crystalline or multi-crystalline material through a high temperature process (solid silicon melts at 1420 $^{\circ}$C) whereby chemical bonding in the original feedstock is lost.

The specific elemental impurities that need to be evaluated in feedstock depends, to some extent, upon the process to make the solar wafer and the solar cell design and processing. However, the list of impurities always includes the following: dopants (mainly B and P), atmospherics (mainly O and C) and transition metals (especially Fe). But beyond the usual suspects, the list can be expanded to almost the entire periodic table of elements (conversion of metallurgical grade silicon into "upgraded" metallurgical grade silicon for PV Si feedstock may result in many different impurities beyond the usual suspects.)

Review of analytical techniques

The definition of an analytical technique for feedstock evaluation includes the sample preparation, not just the direct analysis. The reason is that the sample preparation may change the concentrations of the impurities of interest, or the sample preparation may create a chemical state of an impurity that is useful, or not, in the analysis. An example would be to take the feedstock and grow a multi-crystalline block that could be analyzed using resistivity, lifetime techniques, or FTIR. The process of growing the block may introduce impurities, such as O, C, N, and Fe, or even dopants such as Al. Or, the process may result in a mix of chemical states for O which can affect the FTIR measurement, or thermal donors related to O which will affect resistivity. The "analysis" which includes the sample preparation would have to be controlled and monitored in such a way that these artifacts do not result in misleading data. For these kinds of reasons, we will comment on the sample preparation as part of the analytical technique.

At first thought the simplest approach to feedstock evaluation is to convert the silicon feedstock into a form whereby resistivity, lifetime and FTIR can be measured. If the new form is a single-crystal of Si grown by the Float-Zone process (SEMI MF1723-1104, SEMI MF1708-1104) followed by a thermal donor annihilation process and a 2 mm slug is cut from the ingot, then resistivity measurement provides the net carrier concentration, lifetime gives an indirect measure of the impurities, and FTIR provides interstitial O concentration and subsitutional C concentration. Low temperature FTIR or PL can provide B, P and Al concentrations. One must take into account the segregation coefficients of impurities through the FZ ingot (SEMI MF 1723-1104). This kind of collective analysis was common for Siemens polysilicon evaluation in the 1980's and may still be today. The sample preparation process could be done cleanly, and the O and C tended to form chemical states accessible to FTIR. For very high purity Siemens polysilicon this works well. It should be noted that the very high purity Siemens polysilicon had extremely low concentrations of dopants and metals. The test method (SEMI MF1630) for low temperature FTIR is limited to 5 ppba of electrically active impurity and the test method (SEMI MF1398) for PL also has some upper limits. These upper limits in concentrations restrict these techniques from being useful for a range of higher impurity PV Si Feedstock. Resistivity by itself cannot provide dopant concentration if there is compensation from different dopants.

One can go through a similar sample preparation as above via a Cz crystal growth process, but O is introduced from the crucible and the low temperature FTIR and PL have the same constraints as described above.

One can follow a similar sample preparation but using a multi-crystalline growth process like direct solidification.   In this case O, C, N and Fe may be introduced, and the O and C may form precipitates that are not measured by the FTIR. If there is more than one dominant dopant, resistivity will not give the correct dopant concentration. If one knows the impurity segregation coefficients and measures the resistivity as a function of position along the growth axis of the multi-crystalline ingot, in principle the dopant concentrations can be determined. One needs to truly know the segregation coefficients which are a function of the growth rate, and all contributions from thermal donors need to be eliminated. Artifacts from the multi-crystalline nature of the material that can affect the resistivity need to be eliminated.

Lifetime measurements provide an indirect measure of contamination, at least for those which are strong scatters of minority carriers, but identification of specific metals or their concentrations are not possible except for Fe in B-doped silicon using SPV. Although lifetime is an indirect measure of contamination, for many solar cell designs this parameter is key even if the specific elements are not known. The downside is that a low lifetime does not identity how to improve the feedstock quality.

The next series of analytical techniques do not require a conversion of the feedstock into ingot or block form.

Neutron Activation Analysis (NAA) is the most sensitive instrumental analysis technique for bulk analysis of moderate to high-Z impurities, and can make measurements on any form of the feedstock. The technique requires access to a neutron source which makes it restricted in location, and the nuclear decay times for analysis are quite long, so that analysis results can take one or more months to achieve. Thus, this technique though the most sensitive has limited use commercially. NAA is used for IC-grade polysilicon analysis for metals because of its very high sensitivity and the ability to quantify individual elements.

Another analytical technique that was developed for the IC-grade polysilicon is acid extraction followed by atomic absorption spectroscopy (SEMI MF1724) or ICPMS. This method was developed to test for metals on the surface of the polysilicon and was not intended as a bulk analysis. It could be applied to any polysilicon form, such as chunks, granules, or powders. The test method describes the use of blanks and controls that are critical to identifying interferences, and this method requires a high skill in avoiding contamination. The downside of this test method is that it does not measure the bulk impurity levels. However, it is possible to do a variant of this method by digesting the entire sample (a small sample) and then analyzing the solution by ICPMS.

Inert Gas Analysis or Gas Fusion requires the feedstock to be shaped into a cylinder for insertion into the instrument which heats the sample such that gases (O, C, N, H) from

the sample are emitted and analyzed. One must note that the gaseous species can derive from the sample surface or its bulk, but emission from the bulk does not depend upon chemical state. Detection limit for O is 1 ppmwt which is useful.

The last two techniques are Glow Discharge Mass Spectrometry (GDMS) and Secondary Ion Mass Spectrometry (SIMS), both of which are direct sampling techniques, require no conversion of the feedstock form, and samples of all forms can be analyzed – chunks, granules, powders, or wafers. Samples may require no "preparation", or simple mechanical shaping. Both techniques can be used to analyze all elements in the periodic table (but detection limits or precisions may not be useful for all elements or "grades" of feedstock), and the analysis is independent of the chemical or electronic state of the impurity. Standard test methods have been developed for each technique as applied to different materials in the commercial world. GDMS has been used for over 15 years in the high purity metals and alloys industry (for example, ASTM test methods F 1593, F 1845, F 1710). SIMS has been used in the IC silicon industry for over 20 years (for example, ASTM test methods F 1528, F 2139, F 1366, and F 1617). A standard test method for GDMS as applied to PV Si feedstock is under development in the SEMI PV Committee. SIMS can in principle achieve better precisions than GDMS.

The GDMS survey method is most cost effective (compared to SIMS) when many impurity elements (up to 73) are of interest, while SIMS is the test method of choice when best accuracy and detection limits of dopant elements- such as B and P – are needed. SIMS also provides the best detection limits and analysis precision for atmospheric species, such as C, O, N and H.

GDMS analysis of PV Si

Cathodic sputtering is used for GDMS analysis. The cathode/sample is bombarded by positive ions formed in the glow-discharge. Argon is typically used as the discharge gas. Argon positive ions are accelerated towards the cathode (sample) surface with energies from hundreds to thousands of eV resulting in erosion and atomization of the upper atom layers of the sample. This bombardment produces surface erosion, layer by layer. Atoms, electrons and ions are removed from the surface of the cathode/sample. This sputtered material then participates in ionization caused by collisions in the discharge. Analyte ions generated from the sputtered area are measured after being mass separated in a mass spectrometer. The ions are converted into concentrations, typically in unit of parts per million in weight (ppm wt), based on element dependent calibration factors.

Traditional GDMS calibrations for silicon are traced back to NIST SRMs of metallurgical grade silicon or steels. To improve the accuracy for the dopants B and P, EAG has developed protocols that trace the B and P calibration to NIST SRMs of B and P in silicon.

GDMS techniques can be used to quantitatively measure the elemental impurity concentrations in 6N or 99.9999% pure materials and cleaner. The GDMS survey

methods are the most cost effective especially when many impurity elements (up to 73) are of interest.

The table below shows GDMS results of ultra-high purity "IC grade" boron-doped Si ingot. Only B was detected in this BLANK sample. The B detection limit in Si is 0.001 ppm wt.

Element	ppm wt	Element	ppm wt	Element	ppm wt	Element	ppm wt
Li	< 0.001	Cu	< 0.01	Te	< 0.01	Lu	< 0.005
Be	< 0.001	Zn	< 0.05	I	< 0.01	Hf	< 0.01
B	36	Ga	< 0.05	Cs	< 0.001	Ta	< 100
F	< 1	Ge	<0.05	Ba	< 0.01	W	< 0.05
Na	< 0.01	As	< 0.05	La	< 0.01	Re	< 0.01
Mg	< 0.005	Se	< 0.01	Ce	< 0.005	Os	< 0.01
Al	<0.01	Br	< 0.01	Pr	< 0.005	Ir	< 0.01
Si	Matrix	Rb	< 0.01	Nd	< 0.005	Pt	< 0.01
P	<0.01	Sr	< 0.01	Sm	< 0.005	Au	< 0.1
S	< 0.1	Y	< 0.01	Eu	< 0.005	Hg	< 0.01
Cl	< 0.05	Zr	< 0.01	Gd	< 0.005	Tl	< 0.01
K	< 0.05	Nb	< 0.01	Tb	< 0.005	Pb	< 0.01
Ca	< 0.05	Mo	< 0.05	Sm	< 0.005	Bi	< 0.01
Sc	< 0.001	Ru	< 0.01	Eu	< 0.005	Th	< 0.005
Ti	< 0.005	Rh	< 0.01	Gd	< 0.005	U	< 0.005
V	< 0.005	Pd	< 0.01	Tb	< 0.005		
Cr	< 0.01	Ag	< 0.01	Dy	< 0.005		
Mn	< 0.005	Cd	< 0.05	Ho	< 0.005		
Fe	< 0.05	In	< 0.01	Er	< 0.005		
Co	< 0.005	Sn	< 0.01	Tm	< 0.005		
Ni	< 0.01	Sb	< 0.01	Yb	< 0.005		

SIMS analysis of PV Si

Secondary Ion Mass Spectrometry (SIMS) analysis provides a more accurate quantitative measurement for impurities in PhotoVoltaic grade silicon (PV Si) at the sub-6N level (sometimes needing high mass resolution). Unlike Instrumental Neutron Activation Analysis (INAA) which takes a few months to complete the analysis, SIMS can be accomplished within a few hours. SIMS can measure all elements of the periodic table, but is especially good for dopants (B, P, As, Sb, Al, In) independent of electrical activity and for atmospherics (H, O, C, N) independent of their chemical state. The cost of SIMS for a few elements is low, but because it is an element specific technique the cost can become prohibitive for a large number of elements. GDMS is recommended when the number of elements of interest is more than a few.

During a SIMS analysis, the samples are sputtered by a focused energetic primary ion beam, either oxygen (O_2^+) or cesium (Cs^+). Secondary ions formed during the sputtering process are accelerated away from the sample surface. Secondary ions are energy separated by an electrostatic analyzer and mass separated based on their mass/charge ratio by a magnetic mass analyzer. Oxygen (O_2^+) beam sputtering is used to enhance ion yield of electropositive species (boron and metal elements); cesium (Cs^+) beam sputtering is used to enhance ion yield of electronegative species (P, As, Sb and atmospherics species).

By choosing the proper primary beam and using optimized instrument conditions, SIMS can provide excellent detection limits at sub-ppm to ppt level. The table below shows SIMS detection limits at bulk mode in Si for selected elements. Please note that units used in the table are atosm/cm3 and parts per **billion** in weight (ppb wt).

SIMS detection limits in Si

Atoms/cm^3 (ppb wt)

O$_2^+$ primary beam				Cs$^+$ primary beam	
He	1E17 (286)	Cr	3E11 (0.01)	H	5E16 (36)
Li	5E11 (0.003)	Mn	2E12(0.1)	C	2E15 (30)
B	1E12 (0.008)	Fe	1E13 (0.4)	N	5E13 (0.5)
Na	5E11 (0.001)	Ni	1E14 (4)	O	5E15 (60)
Mg	1E12(0.02)	Cu	1E14 (4)	F	1E14 (1)
Al	5E12 (0.1)	Zn	1E14 (6)	P	1E13 (0.2)
K	5E11(0.001)	Mo	1E14 (7)	S	2E14 (10)
Ca	2E12 (0.08)	In	1E13 (0.8)	Cl	5E14 (23)
Ti	1E12 (0.03)	W	5E13 (7)	As	1E13 (0.5)
				Ge	5E13 (2.6)
				Sb	1E13 (0.8)
				Au	1E13 (1.4)

SIMS is both accurate by using traceable reference materials and precise using highly developed protocols and instrumentation. For the dopants B, As, and P in silicon there are even NIST certified reference materials. Long term precisions for bulk analysis of B and P in Si are shown in the following figure. Even at very low 10^{14}/cm^3 concentration level of B (0.001 ppm wt), SIMS analysis can achieve long term reproducibility of 7.5 % (1 σ).

EAG Boron bulk measurement control

EAG P in Si control
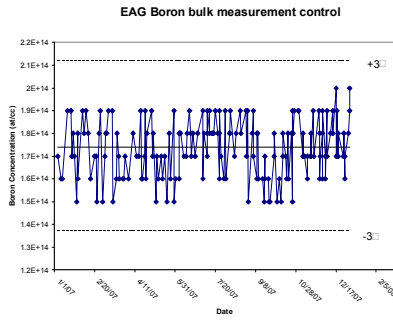
Stdev (1s) =7.5%

Stdev (1s) =4%

23
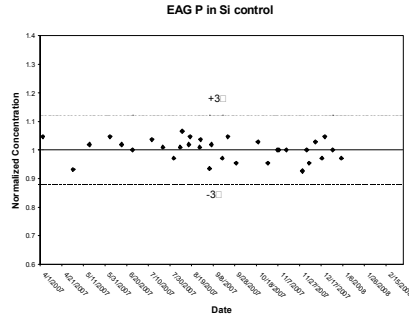
PV Si can come in many forms, including powders. SIMS can be used to measure wafers, chunks, granules, flakes or even powders if the size of the powder is greater than 300 um. Results below were obtained from powder Si sample (see figure below) with the impurities in individual powder pieces, as shown in the following table. The analyses were performed using five analytical conditions.

Element	Ppm wt	Element	ppm wt
B	1.1	Cr	<7E-5
C	9	Fe	<0.001
O	30	Ni	<0.008
Al	0.3	As	0.07
P	8.1		

In conclusion, GDMS can provide high sensitivity survey and total elemental impurity mass concentrations analysis. SIMS can be used for accurate, precise, and localized measurement of selected impurities in PV Si.

<u>Uniformity Study of B, Al, P, C, O, Ca and Fe in Upgraded Metallurgical Silicon (UMG-Si) by SIMS</u>

In the beginning of this paper we mentioned that the analysis is only one part of the problem for evaluating feedstock. *Representative* sampling and process stability of the silicon feedstock are also part of the problem, and a procedure to validate the statistical process control of the analytics is also critical.

The worldwide shortage of polysilicon for mono-crystalline and multi-crystalline Si PV has resulted in R&D and now commercialization of upgraded metallurgical silicon (UMG-Si) which has higher levels of impurities than traditional Siemens-based polysilicon but which can be used successfully in some PV solar cell designs. In the early days of Siemens-based polysilicon (over 30 years ago) companies had to determine the uniformity of impurities in the large polysilicon rods in order to know how to characterize the impurities for an individual polysilicon rod. In other words, where and how many samples must be taken from the polysilicon rod and analyzed in order to provide a *representative* level of impurities for the polysilicon rod and eventually for the *process*? The following preliminary experiment was completed in support of one UMG-Si manufacturer in order to determine if this kind of study will be necessary for UMG-Si. The conclusion was this kind of study will be very important.

Experimental Design
This particular UMG-Si process results in a large, rectangular block of silicon. Samples were taken from three UMG-Si bricks in locations as illustrated in the following figure.
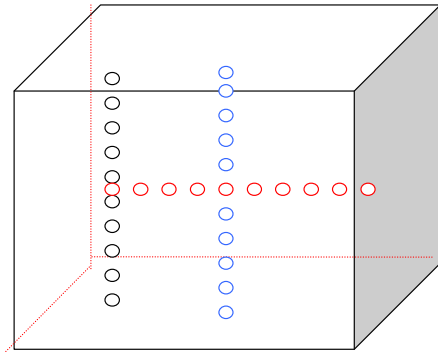
Black circles represent samples from the Edge Vertical, numbered #1 to #10 from top to bottom. The location is close to left hand side of the sample

Blue circles represent samples from the Center Vertical, numbered #1 to #10 from left to right. The location is in the middle between top and bottom

Red circles represent samples from Center Horizontal, numbered #1 to #10 from top to bottom. The location is in the middle between left and right.

All 30 sample pieces (~ 5 mm x 7 mm) were polished on one side as illustrated in the following figure.

SIMS analyses were performed at two or more locations, ~ 150 microns apart, on each sample (polished face). Average concentrations of impurities from two or more locations were averaged and reported for each sample.

B, Al, Ca and Fe: These elements were analyzed using oxygen beam sputtering and positive ion detection (O-SIMS). B was analyzed using maximum transmission. Al was analyzed using Medium Mass Resolution. Ca and Fe were analyzed using High Mass Resolution.

C, O and P: These elements were analyzed using Cs beam sputtering and negative ion detection (Cs-SIMS). C and O was analyzed using best detection sensitivity (low background). P was analyzed using High Mass Resolution.

All quantifications are based on EAG reference materials (standards). The B and P standards are calibrated to NIST standard reference materials, and are accurate to within 1-3%. The Al, C, O, Ca and Fe standards are Ion implanted reference materials which are accurate to within 10-15%.

Analysis precision was as follows. B control (2.9E16/cc) samples were measured together with all samples in B measurements. The analysis precision (1σ) was 3.5%. For all other elements, multiple pieces of standards were measured. The analysis precisions (1σ) were 3-8%.

Results
The following table shows the data for B measurements in the 30 samples taken from three UMG-Si blocks. Concentration units are atoms/cc. The left hand column lists data for samples taken on the edge of a block. This material is normally cut from the UMG-Si block and excluded from use. The sample number sequence (1 through 10) is the sequence of samples taken from the top to bottom of the edge. The average of the 10 samples taken from the edge is 5.06E17/cc and the relative standard deviation (RSD) of the 10 samples is 18.7%. However, the standard deviation is misleading because the B values of the 10 samples in sequence are not random. There is a B trend from top to bottom of the edge as shown the by the % deviation from average for each of the 10

samples. The range (maximum/ minimum) of B is about 1.8x. As stated earlier the analysis precision for B is small (3.5 %) compared to the trend.

B Data (units of atoms/cc)

Edge Vertical Sample Sequence			Center Vertical Sample Sequence			Center Horizontal Sample Sequence		
Sample	Average	Deviation from Ave	Sample	Average	Deviation from Ave	Sample	Average	Deviation from Ave
1	4.40E+17	-13.1%	1	3.59E+17	-3.4%	1	2.30E+17	-12.7%
2	4.24E+17	-16.3%	2	3.37E+17	-9.2%	2	2.90E+17	10.3%
3	4.42E+17	-12.6%	3	3.58E+17	-3.6%	3	2.76E+17	4.9%
4	4.08E+17	-19.4%	4	3.48E+17	-6.3%	4	2.25E+17	-14.6%
5	5.17E+17	2.1%	5	3.85E+17	3.8%	5	2.69E+17	2.3%
6	5.34E+17	5.5%	6	3.72E+17	0.4%	6	2.86E+17	8.6%
7	4.64E+17	-8.3%	7	3.90E+17	5.0%	7	2.26E+17	-14.1%
8	5.26E+17	3.9%	8	4.14E+17	11.5%	8	3.00E+17	14.1%
9	5.95E+17	17.6%	9	3.79E+17	2.0%	9	2.84E+17	8.0%
10	7.17E+17	41.7%	10	3.67E+17	-1.1%	10	2.43E+17	-7.6%
Average	5.06E+17		Average	3.71E+17		Average	2.63E+17	
RSD	18.7%		RSD	6.0%		RSD	11.1%	
Range	1.8x		Range	1.2x		Range	1.3x	
Trend?	yes		Trend?	yes		Trend?	no	

The middle set of data (Center Vertical Sequence) are taken from the sequence of 10 samples taken vertically down the center part of a UMG-Si block. The average is 3.7E17/cc, about 27% lower than the average of the 10 samples taken from the edge, but more importantly the RSD of 6.0% is one third of the RSD of the edge sequence. The B down the center is more uniform than on the edge. The range is 1.2x. There appears to also be a trend.

The far right set of data (Center Horizontal Sequence) are taken from the sequence of 10 samples taken horizontally across the center part of a UMG-Si block. The average is 2.6E17/cc, about 29% lower than the average of the 10 samples taken vertically from the center, and the RSD of 11.1% is about twice that of the RSD of the vertical sequence. The B across the center does not show a clear trend, unlike the other two sequences. The range is 1.3x.

In summary, there are real distributions of B in the UMG-Si block, but as we will see next, on a relative basis the B is more uniform than the P.

The P data are shown in the following table. The averages of the P sequences are closer together than the B, but the RSDs are higher. Two of the sequences have trends.

P Data (units of atoms/cc)

Edge Vertical Sample Sequence			Center Vertical Sample Sequence			Center Horizontal Sample Sequence		
Sample	Average	Deviation from Ave	Sample	Average	Deviation from Ave	Sample	Average	Deviation from Ave
1	1.58E+17	-46.8%	1	2.30E+17	-25.3%	1	1.43E+17	-27.5%
2	1.65E+17	-44.4%	2	2.90E+17	-6.0%	2	2.00E+17	1.3%
3	1.83E+17	-38.2%	3	1.95E+17	-36.7%	3	2.05E+17	3.8%
4	1.72E+17	-41.8%	4	1.98E+17	-35.9%	4	1.36E+17	-31.0%
5	1.99E+17	-32.8%	5	4.07E+17	32.0%	5	2.05E+17	3.9%
6	2.47E+17	-16.4%	6	3.45E+17	12.0%	6	2.03E+17	3.0%
7	3.68E+17	24.4%	7	3.20E+17	3.9%	7	1.36E+17	-31.1%
8	2.52E+17	-14.9%	8	4.00E+17	29.9%	8	3.37E+17	70.9%
9	5.04E+17	70.3%	9	3.55E+17	15.3%	9	2.49E+17	26.4%
10	7.15E+17	141.6%	10	3.45E+17	12.0%	10	1.55E+17	-21.4%

	Edge Vertical			Center Vertical			Center Horizontal	
Average	2.96E+17		Average	3.08E+17		Average	1.97E+17	
RSD	61.9%		RSD	25.3%		RSD	31.5%	
Range	4.5x		Range	2.1x		Range	2.5x	
Trend?	yes		Trend?	yes		Trend?	no	

A summary table for the impurity elements is shown below.

Summary of Results

Sample Sequence	**B**	**P**	**Al**	**C**	**O**	**Ca**	**Fe**
Edge Vertical							
Ave (atoms/cc)	5.06E+17	2.96E+17	3.04E+17	9.42E+17	1.62E+18	<2E 12	< mid E 13
RSD	18.7%	61.9%	119.0%	26.5%	37.0%		
Range	1.8x	4.5x	12.2x	1.9x	4.2x		
Trend?	yes	yes	yes	no	yes		
Center Vertical							
Ave (atoms/cc)	3.71E+17	3.08E+17	7.30E+16	8.68E+17	1.93E+18	<3E 12	< mid E 13
RSD	6.0%	25.3%	16.5%	29.4%	14.9%		
Range	1.2x	2.1x	1.7x	2.3x	1.5x		
Trend?	yes	yes	yes	no	no		
Center Horizontal							
Ave (atoms/cc)	2.63E+17	1.97E+17	2.48E+16	8.90E+17	1.81E+18	<3E 12	< mid E 13
RSD	11.1%	31.5%	40.7%	32.9%	22.1%		
Range	1.3x	2.5x	3.8x	2.5x	1.9x		
Trend?	no	no	no	no	no		

Conclusions from the Summary Table:

- Impurity distributions in UMG-Silicon samples are generally not uniform.
- The range of non-uniformity is element specific
- Boron in this study is the most uniformly distributed element in UMG-Silicon
- Some impurities in some sections show trends (not random distribution) – most likely process dependent

- Sensitive analytical measurements can help manufacturers to improve their processes
- Analytical results can be used to determine, for instance, what material to exclude (e.g., edge)
- Analytical results can be used to select where representative samples should be taken.
- Sampling volume for techniques such as SIMS, GDMS or ICPMS is not relevant

In summary, SIMS can be used to study the uniformity of impurities in UMG-Si, and thereby provide a metric to improve uniformity. In addition, SIMS can help determine where and how many samples need to be analyzed to give a *representative* level of impurities. Lastly, this study reveals that the analytical volume in an analysis (which varies between SIMS, GDMS, ICPMS) does not determine whether one technique can give a *more representative* level of impurities.

Effect of Metal Impurities in Silicon Feedstock on Multicrystalline Silicon Solar Cells

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ABSTRACT

The effect of metal impurities in multicrystalline silicon ingots for solar cells has been investigated by adding impurities to clean polycrystalline feedstock, followed by directionally solidified casting of *p*- and *n*-type multicrystalline silicon ingots and comparing the material to non-contaminated reference material from the same feedstock.

The effect of iron contamination on solar cells is a decrease of the diffusion length in the top half of the ingots, with a trend in agreement with Scheil's model for segregation and an increased crystal defect concentration in the top and bottom of the Fe contaminated ingots. Both effects contribute considerably to the degradation of the solar cell performance. Furthermore, a low lifetime of about 1-2 µs for *p*-type and 6-20 µs for *n*-type, is improved up to 50 times in the *p*-type ingot, and about 5 times in the *n*-type ingot after (boron/)phosphorus (co-)diffusion and hydrogenation due to gettering of iron, pointing out the (reduced) gettering effectiveness of (co-)diffusion.

INTRODUCTION

Due to a shortage in silicon feedstock, the PV industry is considering the option of using less pure silicon, called Solar Grade silicon (SoG-Si) for the production of solar cells. In the 1980's the effect of impurities on the solar cell performance, was studied for single crystalline wafers by Westinghouse Corp. Since then, solar cell processes were modified and the use of multicrystalline wafers, instead of single crystalline, has increased, raising the need for a detailed update before SoG-Si can go to market.

In this work, the focus lies on the impact of Fe on *n*- and *p*-type wafers and solar cells from directionally solidified microcrystalline ingots. Fe is a dominant metal impurity in silicon[1,2.] A typical concentration[3,4] of total Fe in commercial multicrystalline silicon ingots has been reported[2,3] to be in the range of 10^{13}-10^{15} cm^{-3}. Fortunately, for the cell performance, Fe is a relatively fast diffusing impurity (D = 2.6×10^{-6} cm^2/s @ 1000 °C)[5], which can be (partly) removed by gettering during the solar cell process. At the moment, beside the effects of Fe, also those of Ni and Cr under investigation within the 'Crystal Clear' project as possibly dangerous contaminants, being present in stainless steel infrastructure in a silicon manufacturing plant.

It is important that the silicon, containing the examined impurities, is subject to a similar thermal history and process as would be the case when the impurities were naturally present in the feedstock. The thermal history of the material determines, among other aspects, the fraction of impurities that are electrically active in the Si, the properties of precipitates, etc., and thus the final impact of impurities on the solar cell performance. Therefore, in this study, the impurities were added at a feedstock level in contrast to other, earlier approaches[6,7] where contaminants were added on a wafer level by either ion implantation or annealing of a contaminated surface.

The most reliable input parameter to model and predict the impact of an impurity in different cell architectures (e.g., different thickness, different surface passivation, etc.) is the diffusion length (L_D) as a function of impurity concentration. Fe influences the diffusion length through interstitial point defects (Fe_i). Here, an effective diffusion length was determined directly from spatially resolved and averaged internal quantum efficiencies (IQE) of the solar cells. Moreover, besides a reduction of L_D due to interstitial point defects, Fe also seems to affect the formation of a good crystal structure, leading to an even further reduction of the performance of the solar cells.

EXPERIMENTAL
Four pilot scale ingots of 12 kg with a diameter of 250 mm and a height of 110 mm have been grown using a Crystalox DS 250 furnace and a Bridgman-type directional solidification method. All known sources of contamination (e.g. feedstock, crucible, and coating) were minimized by using virgin polysilicon, high purity (HP) crucibles[8] and purified Si_3N_4[9]. Some additional dopants, 0.116 ppm wt of B for *p*-type and 0.318 ppm wt of P for *n*-type, and the intended amount of impurities (here 53 ppm wt of Fe) were introduced in the feedstock charge, resulting in bulk resistivities of ~1.0 $\Omega \times$cm for *p*-type and 0.4-0.8 $\Omega \times$cm for *n*-type ingots. A full description of the crystallisation process and characterisation of the material can be found in Ref.[10]. In the following, the Fe contaminated ingots will be referred to as *p*-type *Fe* and n-type *Fe*, respectively.
The *n*-type reference ingot has a substitutional carbon concentration of about 7×10^{17} cm^{-3} in the top of the ingot, while the others had values below 10 ppma, because it was grown under slightly different furnace conditions. In both n-type ingots the interstitial oxygen concentration $[O_i]$ is about 3×10^{17} cm^{-3}, the Fe contaminated p-type ingot had an $[O_i]$ of 1.5×10^{17} cm^{-3} and the p-type reference had an $[O_i]$ of 3×10^{17} cm^{-3} due to sticking problems.
From each ingot centre a block of 125×125 mm^2 was cut and sliced into 240 μm thick wafers, of which 10 representative wafers were processed into solar cells. The *p*-type solar cell process is the state of the art industrial P diffusion Al-Back Surface Field (BSF) SiN$_x$:H firing through[11]. The *n*-type cell process consists of a boron front emitter and phosphorous BSF in a co-diffusion step (B/P co-diffusion), both passivated by SiN$_x$:H, and firing through metallization with open rear side grid[12].
Neighbouring wafers for minority carrier lifetime characterization were co-processed and taken out of the batch after some processing steps, one group directly after P diffusion and another after hydrogenation, where the last group was taken out after SiN$_x$:H anti-reflection coating (ARC) deposition and then fired, with an extra layer of SiN$_x$:H on the rear side and without metallization to imitate the hydrogenation effect of the cell process. For the lifetime measurements, the SiN$_x$:H layers and/or emitter were removed by chemical polishing, followed by deposition of a SiN surface passivating layer[13] on both sides. Similarly, for the *n*-type cells the first group was taken after and the second after B/P co-diffusion and hydrogenation.

RESULTS

Solar cells
In Figure 1 the short circuit current (J_{sc}) times open circuit voltage (V_{oc}) product is reported as a function of vertical position in the ingot. $J_{sc} \times V_{oc}$ represents the recombination in the solar cells, excluding variations due to process-induced or material-related series resistance and shunts that influence the fill factor (FF). At about 70% ingot height the $J_{sc} \times V_{oc}$ values of the two p-type ingots are comparable, while in the bottom half and the top, those of the the Fe doped ingot are relatively

reduced. In the *n*-type Fe doped ingots, $J_{sc} \times V_{oc}$ is reduced in the bottom and the middle. In the top, the performance of the *n*-type reference decreases, approaching the value of *n*-type *Fe*. From spectral response and reflectivity measurements the internal quantum efficiency (IQE) and the effective average minority carrier diffusion length (L_{eff}) were calculated.[14] The main differences between the references and Fe doped ingots are in the long wavelength response.
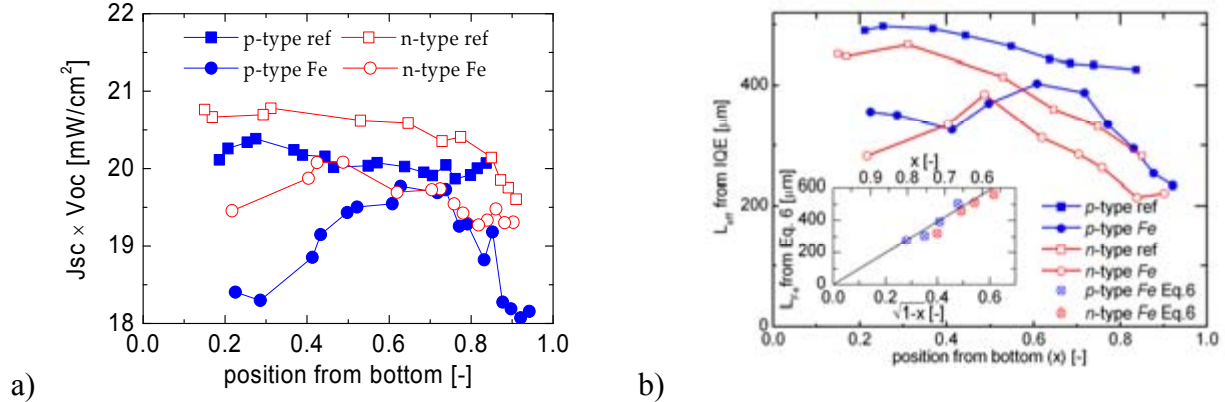
Figure 1. *(a): $J_{sc} \times V_{oc}$ versus vertical position in ingot. (b): Diffusion length versus position in ingot. In the inset, the diffusion length, corrected for the contributions of crystal defects (calculated from the reference), is plotted versus square root of the position from the ingot top.*

Crystal structure

By combining Light Beam Induced Current (LBIC) and reflectance measurements at three different wavelengths in a scan over the whole area of a solar cell, maps of the local effective diffusion length were obtained and converted into maps of internal quantum efficiency and local effective diffusion length[15] (Figure 2).The L_{eff} maps qualitatively represent the grain structure, because grains with high defect density show a relatively low LBIC signal and a low L_{eff}[16].Clearly, there is a difference in the crystal structure development for the Fe-ingots compared to the reference ingots. At the bottom and top of the Fe-ingots the density of the crystal defects is enhanced, both in comparison to the about 70% ingot height in the same ingots, and in comparison to the reference ingots.

Minority carrier lifetime

The minority carrier lifetime has been measured by Quasi-Steady-State PhotoConductance (QSS-PC) at an injection level of 10^{15} cm^{-3} before and after FeB pairs dissociation[17,23]. In Figure 3 the FeB lifetime (before dissociation) is given. Some *n*-type wafers were processed together with the *p*-type wafers in the *p*-type process and some *p*-type wafers were processed together with the *n*-type in the *n*-type cell process. The as-grown lifetime in *p*- and *n*-type Fe doped wafers is about 1-2 μs and 6-20 μs, respectively. This difference in lifetime between *p*- and *n*-type can be explained by a Shockley-Read-Hall (SRH) model applied to interstitial Fe defects.

For the *p*-type reference ingot just a minor improvement on a good as-grown lifetime is observed after gettering and hydrogenation (*p*-type process), while the lifetime of *p*-type *Fe* wafers improves up to 50 times and that of the *n*-type *Fe* wafers 5-10 times and the values for *n*- and *p*-type are similar (~2 times higher for *n*-type). Also, the gettered values of the *n*-type *Fe* ingot are similar to the as-grown lifetime values for the *n*-type reference. After B/P co-diffusion (*n*-type process) and hydrogenation the lifetime improves up to 10 times for the *p*-type *Fe* and 3-10 times for the *n*-type

Fe wafers, resulting in a value up to 8 times higher in the *n*-type *Fe* wafers than in the *p*-type *Fe* wafers.
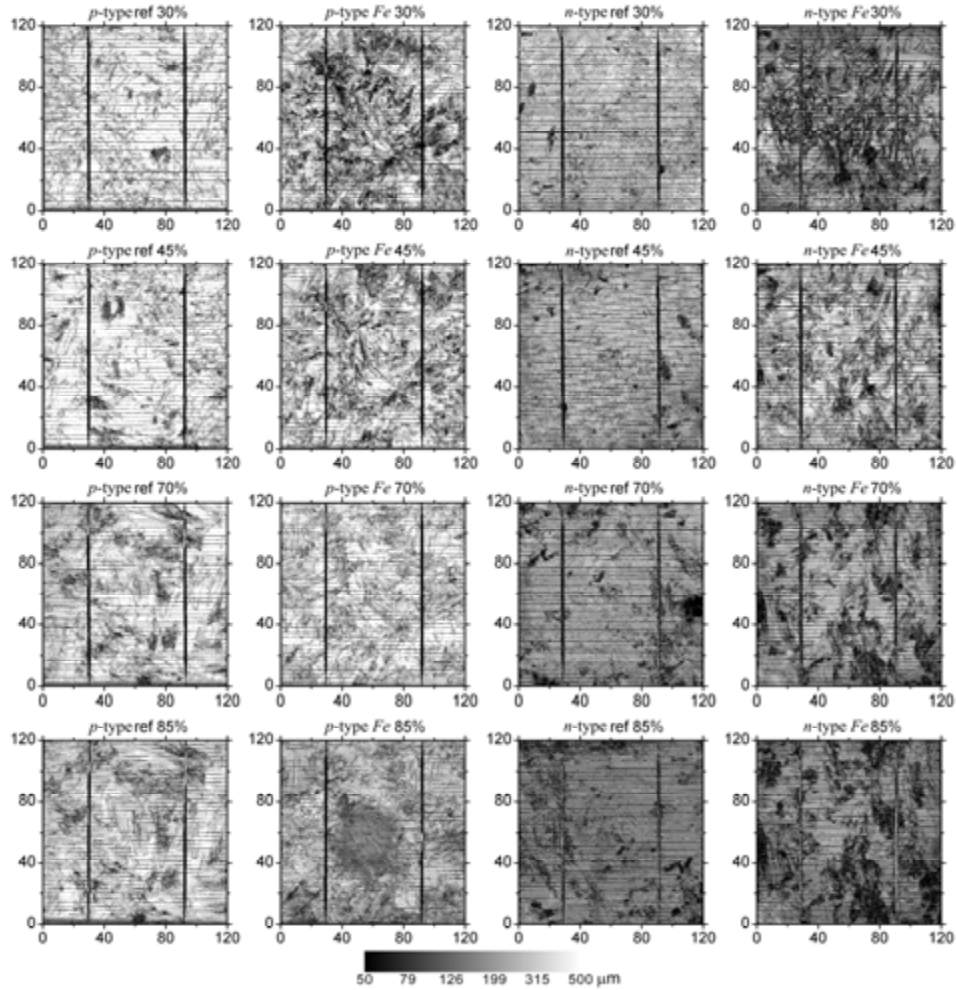
Figure 2: *L_d maps at 30% (upper pictures), 45%, 70% and 85% (lower pictures) of the ingot height respectively. Most left: p-type reference ingot, Centre left: p-type Fe ingot, Centre right: n-type reference ingot, Most right: n-type Fe ingot. The x-y axis values are given in mm.*

Lifetime maps

The lifetime spatial distribution has been investigated by the Modulated Free Carrier Absorption[18] (MFCA) measurements (Figure 4). The as-grown lifetime map shows several GBs rimmed, along their length, by higher lifetime boundaries. Clearly, the average lifetime increases after phosphorous diffusion. After hydrogenation the darker areas improve, showing the passivation of defect areas (GBs and areas with high dislocation density)[19,20,21], but in the higher lifetime areas, which correspond to intragrain areas, the lifetimes slightly decrease. The $1/\tau$ averaged[22] lifetime increases from 47 μs to 58 μs after hydrogenation, confirming the beneficial effect of the hydrogenation (the as-grown $1/\tau$ averaged lifetime is 2.4 μs).After B/P co-diffusion and hydrogenation the averaged lifetime is lower. Here also, several crystal defects, hardly visible in the phosphorous diffusion wafer, are still active.
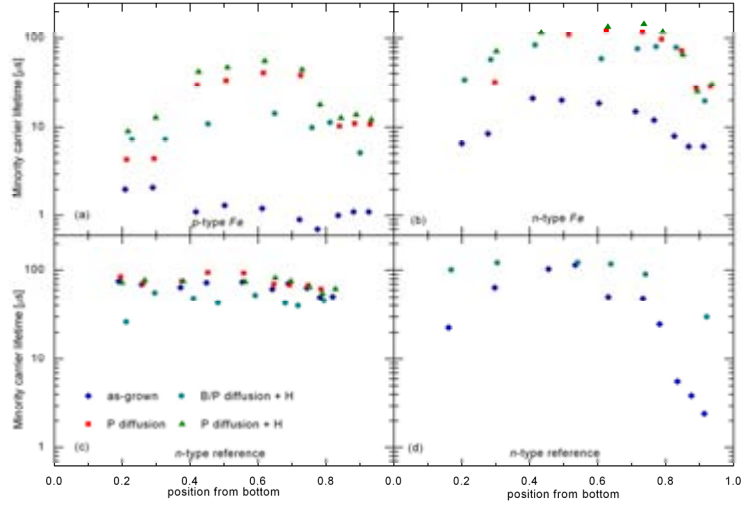
Figure 3: *Minority carrier lifetime versus vertical position in the ingots after different solar cell process steps. P diffusion: emitter formation in p-type solar cell process. P diffusion + H: emitter formation, SiN$_x$:H deposition and firing as in the p-type solar cell process. B/P co-diffusion + H: emitter and BSF formation, SiN$_x$:H deposition and firing as in the n-type solar cell process. (a): p-type Fe doped. (b): n-type Fe doped. (c): p-type reference. (d): n-type reference.*
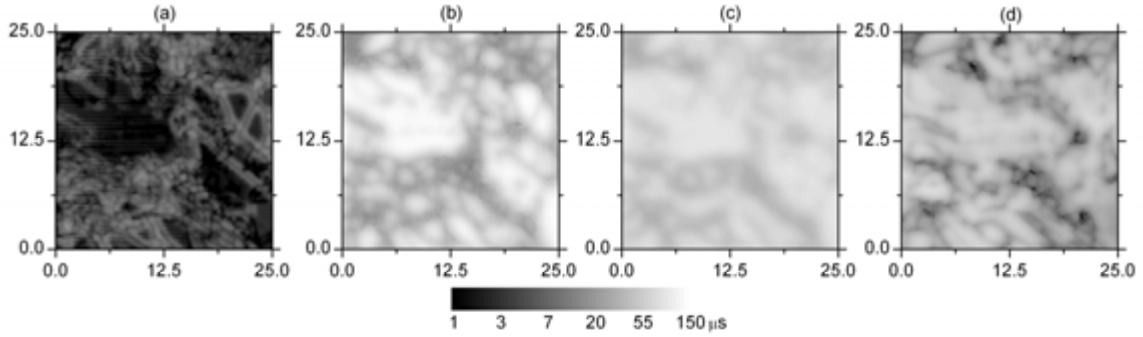
Figure 4: *Lifetime map as measured by Modulated Free Carrier Absorption[18] on neighbouring wafers at ~75% height of the p-type Fe ingot. The resolution used is 250 μm. The as-grown sample (a) has been illuminated with a bias light of 25 suns. Most of the traps are filled at this corresponding injection level as determined by QSS-PC measurements. The samples after P diffusion (b), P diffusion + hydrogenation (c) and B/P co-diffusion + hydrogenation (d), have been illuminated with a bias light of 2.5 suns.*
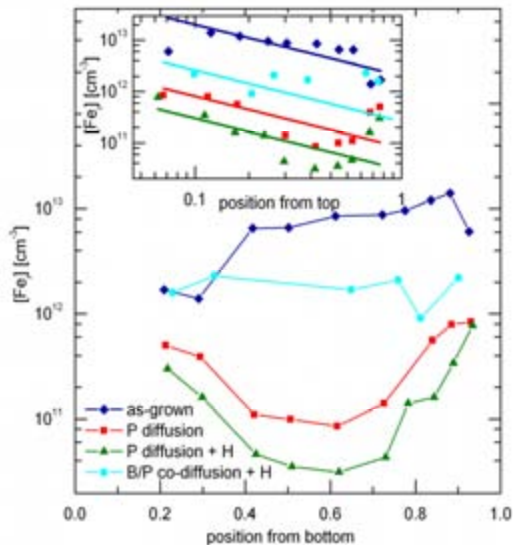
Figure 5: *Interstitial Fe concentration versus vertical position in p-type Fe doped ingot derived from lifetime measurements before and after FeB dissociation. The data are reported after different solar cell process steps. The [Fe$_i$] of as-grown wafers are indicative since the lifetime of these wafers is very low (1-2 μs), which reduces the measurement accuracy.*

Inset: [Fe$_i$] versus vertical position from the top with Scheil equation fit (k<0.01 to rule out k-effects).

Interstitial iron concentration
For the *p*-type ingots, the interstitial Fe concentration [Fe$_i$] was derived from lifetime measurements before and after FeB pair dissociation[23] (Fig. 5). The as-grown [Fe$_i$] is about 10^{13} cm^{-3} in the middle of the ingot and decreases to about 10^{11} cm^{-3} after phosphorous diffusion. After subsequent hydrogenation, the active interstitial Fe is further reduced by a factor two. The concentration of Fe$_i$ after B/P co-diffusion and hydrogenation is about 10^{12} cm^{-3}.

DISCUSSION
p-type and *n*-type solar cell processes were applied to a representative selection of wafers from Fe contaminated and reference ingots produced with clean silicon feedstock. For these cells effective diffusion length values were calculated from IQE measurements, which, comparing the J$_{sc}$×V$_{oc}$ and L$_{eff}$ values in Figure 1, seem to be limiting the solar cell performance, reflecting a similar trend as a function of ingot height. For wafers from the top of the ingot, as is demonstrated in the inset of Figure 1b, this trend, after subtraction for recombination effects that are also present in the reference ingot, can be related to a Scheil-like distribution of interstitial Fe defects according to $L_{Fe} \propto \sqrt{1-x}$. Here, x is the fractional ingot height and L_{Fe} is the impurity affected diffusion length. L_{Fe} was determined using the following relationship between L_{Fe}, the effective diffusion length in the reference L_{Ref} and the effective diffusion length (L_{eff}) in the Fe contaminated ingot:

$$\frac{1}{L_{Fe}^2} = \frac{1}{L_{eff}^2} - \frac{1}{L_{Ref}^2}, \text{ with } \frac{1}{L_x^2} \text{ the recombination due to } x.$$

In the diffusion length maps (Figure 2), a difference in the crystal structure development for both the Fe doped ingots compared to the reference ingots was observed. The Fe doped ingots display an increased crystal defect density in the bottom and top and a comparable level of defects at ~70% ingot height. This is reflected in the solar cell efficiencies, which are reduced in the bottom and top, but are comparable to the reference at around 70% height. The increasing defect concentration in the top of the Fe doped ingots may be related to the increasing iron concentration in the melt. In the bottom, the initial high concentration of Fe in the silicon melt may have initiated or enhanced a transient nucleation and growth disturbance during the early solidification phase, but verification of this hypothesis would require additional dedicated experiments and modeling.

The differences in the as-grown lifetime between *p*- (1-2 μs) and *n*-type (6-20 μs) Fe doped Si ingots can be explained by SRH theory for interstitial Fe defects, taking in consideration the injection level at which the lifetime has been measured and the Fe concentration (at 10^{15} cm^{-3} the SRH curves for p-type already significantly bend upwards). The reduced gettering effectiveness of the p-type process for n-type wafers, i.e. only 5 times improvement of lifetime compared to 50 times lifetime improvement for p-type wafers, might be explained by the presence of a 'ceiling' due to non-getterable defects, because the most harmful impurities in n-type are substitutional. The gettering effect of boron/phosphorus co-diffusion is less effective than phosphorous diffusion and because B/P co-diffusion takes place at higher, for gettering non- optimal, temperature, it causes a larger amount of impurities to dissolve from precipitates and diffuse.

The higher lifetime rims of the GBs, visible in the as-grown MFCA maps, cannot be explained by trapping, because from the QSS-PC measurements it is known that most of the traps are filled at 25 suns illumination. However, the GBs can act as sink for impurities (also known as internal gettering[24,25]), which causes an impurity depletion region, with higher lifetime, beside the GBs. After gettering and hydrogenation, improved passivation of GBs and a degradation of intragrain

areas is observed. The passivation of GBs, and crystal defects in general, depends on both the GBs character[26] and impurity level. In neighbouring samples, the GBs character and as-grown impurity distribution and precipitates are similar, so the activity of the crystal defects after the B/P co-diffusion, compared to phosphorous diffusion is due to a higher remaining impurity level. The degradation of intragrain areas after hydrogenation was observed in earlier work[27] but not discussed, it might also be limited (>100 μs) by surface recombination.

The as-grown [Fe_i] in the *p*-type Fe doped ingot, in the order of 10^{13} cm^{-3}, represents about 10% of the total iron concentration, which is estimated from a Scheil distribution fit that is presented in the inset of Figure 5. After phosphorous diffusion, the concentration of interstitial Fe is not constant, but shows, in the top of the ingot, a trend roughly referable to the Scheil equation (inset Fig. 5). The [Fe_i] after phosphorous diffusion is expected to be equal to the solubility of Fe at the gettering temperature, so independent of the wafer position. However, the gettering effectiveness is known to depend on the crystal structure, which might explain the observed trend for [Fe_i]. Possibly for similar reasons, the [Fe_i] remains high in the bottom after gettering.

The impact of Fe on multicrystalline solar cells, as described above, is confirmed by recent tests within Crystal Clear on a similar ingot with 200 ppm wt of Fe, for which the effects were very similar, but enhanced. Also Ni and Cr contaminated ingots show a decrease of efficiency in both bottom and top, but on a more detailed level their influences differs from that of Fe.

CONCLUSIONS

The solar cell performance of Fe contaminated wafers follows a trend resembling that of the diffusion length as a function of vertical position in the ingot. In the top, this trend can be related to a Scheil like distribution of interstitial Fe defects through the ingot. Both in the top and the bottom an enhanced crystal defect density is observed.

A low average lifetime of about 1-2 μs for *p*-type and 6-20 μs for *n*-type, is improved up to 50 times in the *p*-type ingot, and about 5 times in the *n*-type ingot after (boron/)phosphorus (co-)diffusion and hydrogenation due to gettering. Clearly, the gettering effect of co-diffusion is less effective. Some grain boundaries seem to act as a sink for impurity defects in as-cut samples. Passivation of GBs and areas with high dislocation density by means of hydrogenation is observed.

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Toward a 21% Commercial Silicon Module

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ABSTRACT: In January of 2008, SunPower began ramping the production of its Gen 2 solar cell technology platform, from a pilot capacity of 28 MW to a present capacity of 225 MW, to an entitled capacity of more than 400 MW by the end of the year. Sunpower's Gen 2 solar cell achieves low cost in high-volume production at conversion efficiencies of 22.4% and produces modules with power up to 315 watts. The increase in solar cell performance over its Gen 1 technology has resulted from improved patterning techniques and optimized cell/process design, leading to lower series resistance, lower carrier recombination and higher carrier collection. A 20.1% Gen 2 module was constructed using 165 mm diameter semi-square wafers for better packing density, a 96-cell module format for reduced perimeter loss, and an antireflection coated glass in the module. Sunpower recently announced plans for a 1 GW plant in Malaysia, and announced initial results of the Gen 3 solar cell technology platform reaching conversion efficiencies as high as 23.4%. These recent developments make the prospect of a 21% commercial silicon module seem very promising.

Introduction

SunPower Corporation designs and manufactures high-efficiency silicon solar cells, modules and systems for residential, commercial and utility-scale power plant generation markets. High cell efficiency is a key driver in the economics of photovoltaic energy because it leverages savings across the entire PV value chain, from the cost of raw silicon, to the per-watt cost of cells and modules, to the per-area costs of modules and systems.

In 2003, Sunpower introduced its Gen 1 "A300" technology platform based on a cost competitive

Figure 1. Gen 2 solar modules on single axis trackers at Nellis Airforce Base, Nevada USA.

manufacturing technology and back-side contact solar cell technology. This technology platform achieved over 21% and 18% cell and module efficiencies, respectively, with an installed capacity of 75 MW presently.

In 2007, Sunpower introduced its Gen 2 technology platform, extending and improving on the A300 platform and reaching 22% and 20% cell and module efficiencies, respectively. At present, the Gen 2 platform has an installed capacity of 250 MW with announced planned total capacity of more than 1.3 GW.

In 2008, Sunpower announced early stage results of its Gen 3 cell technology platform, reaching 23.4% cell efficiency in pre-pilot production.

This presentation reviews the key improvements of the Gen 2 technology platform in addition to several module improvements that led to a 20.1% confirmed Gen 2 module efficiency.

Gen 2 Cell Improvements

One of the key improvements of the Gen 2 platform is a reduction in overall recombination, leading to improved open-circuit voltage. Contact

and diffused region recombination are two of the main recombination loss mechanisms addressed by the Gen 2 platform. Smaller contact features are enabled by enhanced lithography techniques and the diffusion processes are optimized around the contact feature size, leading to minimal total recombination of the contacted and non-contacted regions.

Another key improvement of the Gen 2 platform is a reduction of the finger-finger pitch, which is another improvement enabled by enhanced lithography techniques. Reducing this pitch lowers both resistance losses associated with lateral drift and enhanced recombination associated with lateral diffusion in the base layer. Reducing the diffusion pitch also reduces the device's sensitivity to variations in bulk resistivity and minority carrier lifetime, leading to tighter electrical yield distributions.

These improvements, along with careful attention to design detail at the cell edges and bus bars, enabled the Gen 2 platform to reach over 22% conversion efficiency in production cells, as illustrated in Figure 2.

Module Improvements

Module optics is an important opportunity for improving module efficiency. Front reflection at the air-glass interface accounts for about 4% of optical loss due to reflection. A front anti-reflection coating improves module current by an average of 2.4%, which is equivalent to almost 0.5% absolute efficiency increase in a 20% module. The anti-reflection coating also improves
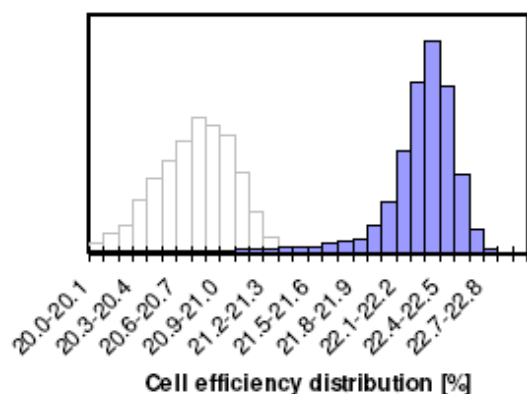
Figure 2. Production efficiency histograms for Gen 1 (left) and Gen 2 (right) technology platforms.

daily energy collection by coupling more light into the module at steep angles.

Module back sheet reflection also contributes to an internal optical enhancement that boosts module performance. Tests on modules made with 92% cell packing density showed a 2.3% increase in performance with a white backsheet compared to a black backsheet.

Packing density is another opportunity to increase module performance. Sunpower manufactures Gen 2 cells on two wafer formats: 125 x 125 mm2 pseudo square cut from 150 mm and from 165 mm diameter ingots. Wafers cut from 165 mm ingots increases the packing density from about 92% to about 96% and produces approximately 4.2% more power density in the module, although this reduces the white backsheet benefit by about half.

Packing density can also be improved by using larger modules, which decreases the perimeter and frame area contributions relative to the active area of the module. Moving from a 72-cell module to a 96-cell module increases the module power density by about 0.5%.

These improvements were incorporated in a champion module constructed using Gen 2 cells, with a verified (NREL) efficiency of 20.1%. These modules will be commercially available in limited quantities starting next year.

Conclusion and Outlook

Continuous improvements on the Gen 2 technology platform are expected to lead to further performance gains over time, and further engineering improvements at the module level will enhance module performance as well. These engineering efforts will enable a 20% commercial Gen 2 module technology that can be manufactured in high volume production. Nonetheless, the Gen 3 technology platform and future process technology and tool improvements will enable further performance gains at the cell level, making the prospect of a 21% commercial silicon module seem very promising.

Progress Towards High Efficiency All-Back-Contact Heterojunction c-Si Solar Cells

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Abstract

All-back-contact heterojunction crystalline silicon solar cells have a potential to reach 26% efficiency based on modeling results due to the short-circuit current density and fill factor advantage of the back contact design, and the high open-circuit voltage of heterojunction structures. The amorphous/crystalline silicon heterojunction solar cell performance is largely governed by the properties of the intrinsic amorphous silicon buffer layer (i-layer) on the emitter side. By optimizing the i-layer, we have achieved excellent silicon surface passivation with minority carrier lifetimes greater than 1 ms and heterojunction solar cell efficiency of 18.4% on textured wafer. The same i-layer applied to the interdigitated back contact structure improves short-circuit current without affecting open-circuit voltage, but results in a poor fill factor with an "S" shape J-V curve. 2D numerical simulation is used to guide optimization of the i-layer properties. Preliminary experimental results show that lowering the band gap of the i-layer dramatically improves the fill factor of back contact heterojunction solar cells.

Introduction

Silicon continues to dominate the photovoltaic market and large scale expansion of mono- and multi-crystalline silicon solar cells over the last decade looks set to continue. Current efforts in the bulk silicon technology to increase efficiencies and lower processing costs are leaning towards thinner wafers, low temperature continuous processing, and superior passivation and metallization schemes. The highest efficiency modules on the market today are manufactured by SunPower, with a confirmed efficiency of 20.1% [1] using Interdigitated Back Contact (IBC) (or all-back-contact) solar cells. While SunPower produces diffused junction solar cells with the highest open circuit voltages (V_{OC}) in production at 680 mV [2], these voltages are considerable lower than the over 730 mV manufactured by Sanyo using silicon heterojunctions (SHJ) [3]. Current efforts at the Institute of Energy Conversion with SunPower, as a part of the Solar America Initiative (SAI), are geared towards combining the advantages of IBC design with SHJ and low temperature processing to yield high-efficiency and low cost silicon solar cells. Initial experiments have independently confirmed an 11.8% efficient cell without any optimization [4] and modeling with Sentaurus package [5] indicates possibilities of 24-26%.

Rear-junction, IBC c-Si solar cells potentially have a number of advantages over conventional front-junction solar cells. The back surface of IBC solar cells can independently be optimized for low series resistance and high fill factors (FF), while the front surface is separately optimized for passivation and anti-reflection (AR) properties to achieve maximum optical coupling and high short circuit currents (J_{SC}). Back contact solar cells are far easier to incorporate into a module with a higher packing factor since all the contacts are on one side of the wafer, and the interconnection strips do not have to pass from the front of one cell to the back of the next. Therefore, the advantages of all-back-contact solar cells include performance (no shading loss and avoiding the trade-off between series resistance and reflectance), manufacturability (for example, ease of series

connection for module and allowing for higher packing factor) and aesthetics (PV modules with more uniform appearance is desirable for architectural applications).

While the advantages of all-back-contact c-Si solar cells are well known, their implementation is hindered by several design and processing constraints. Further improvements in cell efficiency will require new contacts and junctions that have lower recombination than that achieved by diffused devices. Moreover, high temperature processing induces thermal stress and bending of wafers. These limitations can be circumvented using low temperature depositions and fabrication of heterojunctions mainly in three ways. First, since thin wafers are attractive for back contact cells as they require minority carrier diffusion lengths greater than twice the device thickness, low temperature junction and contact formation processes are crucial for such solar cells. Second, heterojunction are able to achieve the low surface recombination velocities required to achieve high V_{OC}'s. Finally, the central challenge in back contact solar cells, patterning in the rear, is easier for deposited heterojunctions since it is easier to mask and etch deposition compared to diffusions. In addition, rear junction devices with deposited amorphous silicon (a-Si) layers also mitigate possible disadvantages of the front junction technology that require front transparent conductive oxides (TCO) and a-Si layers causing absorption losses.

In this paper, we present progress towards realizing high-efficiency IBC-SHJ solar cells using low temperature (200 °C) deposited a-Si:H/c-Si heterostructures. Key results and achievements are classified into four parts: (1) passivation quality of the free crystalline silicon surface by intrinsic a-Si:H and its structural and optical properties, (2) the front junction SHJ cells with high V_{OC} and understanding device operation, (3) fabrication of IBC-SHJ solar cells and comparison with front junction solar cells, and (4) 2-D numerical simulation to understand IBC-SHJ cell operation and guide experiments to improve device performance.

Experimental

Most experiments are carried on n-type Si wafers (~300 μm) with resistivity of 1.0 Ω.cm for (100) and 2.5 Ω.cm for (111) oriented wafers. The samples are cleaned for 5 mins in a mixture of H_2SO_4:H_2O_2 (4:1) followed by 5 mins rinse in de-ionized water and in 10% HF for 60 sec prior to each Si:H deposition. The Si:H i-layers (10 nm) are deposited on both sides by RF and DC plasma processes using a six-chamber large area (30 × 35 cm²) chemical vapor deposition (CVD) system. The substrate temperature, deposition pressure and SiH_4 flow rate are fixed at 200 °C, 1250 mTorr and 20 sccm, respectively. The primary variable in the i-layer process is the H_2 flow rate, which was varied from 0 to 200 sccm, and characterized by the dilution ratio R = H_2/SiH_4. The RF power of 30 W and a DC plasma current of 123 mA are maintained constant. The quality of surface passivation is determined by measuring effective minority carrier lifetime (τ_{eff}) using the photoconductive decay method [6]. Structural and optical characterizations of thin layers are performed using fourier transformed infrared (FTIR) spectroscopy and variable angle spectroscopic ellipsometry (VASE) measurements. Thin layers (10 nm) of p-type a-Si:H emitter followed by 70 nm indium tin oxide (ITO) with metal grids at the front and n-type a-Si:H followed by an evaporated Al contact at the rear are deposited to fabricate front junction SHJ cells. The interdigitated pattern of deposited p- and n-type a-Si:H layers (20 nm) and evaporated Al contacts are created for the IBC structure by two step photolithography processing, where the width of p- and n-fingers are 1.2 mm and 0.5 mm [4], respectively. The front surface of IBC cells are passivated by a 20 nm a-Si:H i-layer followed by AR coatings. This surface passivation/AR structure is not ideal for high J_{SC}, but provided a means of direct comparison with the front junction SHJ cell performances.

Results and Discussions

(1) Passivation of silicon surface with intrinsic a-Si:H.

Figure 1 shows τ_{eff} as a function of R for i-layers deposited on (100) and (111) wafers by DC and RF plasma after annealing the samples at 280°C for 10 mins. Three distinct regions can be identified in the variation of τ_{eff} with R. In region I, R < 2, τ_{eff} depends on the plasma process; namely, DC plasma deposited i-layers at R = 0 show slightly lower lifetime, ~ 500 μsec, than RF plasma deposited i-layers, > 1 msec, irrespective of the wafer surface orientation. τ_{eff}, however, becomes similar for RF and DC plasma deposited i-layers at R > 2, region II and III, implying little or no adverse effect of ion damage in the DC process on Si surface passivation. In region III, R > 4, the measured τ_{eff} exhibits a pronounced Si surface orientation dependence. The values of τ_{eff} sharply decrease to < 10 μsec on (100) wafers, while on (111) wafers they remain > 1 msec even at R = 10.
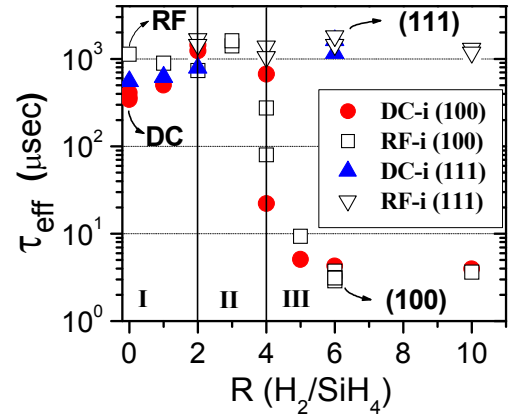
Figure 1. Effective minority carrier lifetime (τ_{eff}) on Si (100) and (111) wafers with 10 nm Si:H i-layer deposited on both sides by RF and DC plasma at variable hydrogen dilution (R).

Structural and optical characterizations are performed on the same thin i-layers on Si (100) and Si (111) wafers to understand the variation of their surface passivation quality. FTIR spectra are recorded after lifetime testing and prior to the SHJ cell fabrication. An increased peak at ~2090 cm^{-1} due to Si-H$_2$ compared to the peak at 2000 cm^{-1} due to Si-H stretching vibration is correlated to poor optoelectronic quality due to microstructural defects. Figure 2 shows that the Si-H fraction decreases while the Si-H$_2$ fraction increases monotonically with the decrease of R. For R ≤ 2, DC plasma deposited i-layer has more SiH$_2$ compared to the RF process. At R = 0, a significant poly-silane formation in the plasma is expected and contributes to the film growth for both DC and RF processes. This poly-silane concentration is comparatively higher in DC due to the presence of a larger amount of reactive ionic species, which produces a-Si:H films with more microvoids and SiH$_2$. Formation of poly-silane decreases with an increase of R in DC plasma [7]. Despite a large variation of SiH$_2$ bonding in films deposited by either RF or DC plasma with different R, the relatively small changes in τ_{eff} (only by a factor of 2) as shown in Figure 1 suggests that the passivation quality of a-Si:H i-layers is only weakly dependent on the amount of SiH$_2$, microstructural defects and deposition process of the i-layer. On the other hand, τ_{eff} decreases more than two orders of magnitude on (100) compared to (111) wafers at R > 4.
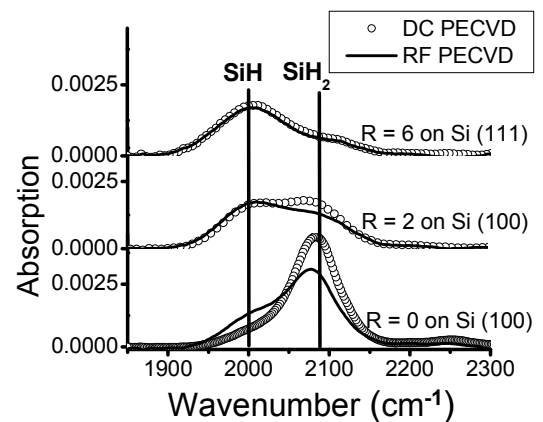
Figure 2. Comparison of FTIR spectra of 10 nm thick a-Si:H i-layers grown by RF and DC plasma with variable hydrogen dilution (R).
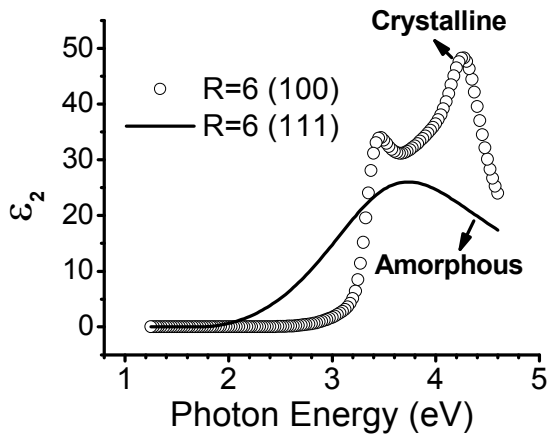
Fig.3: Imaginary part of pseudo-dielectric function (ε_2) as a function of photon energy (E) for the Si:H i-layers deposited with R=6 on (100) and on (111) wafers.
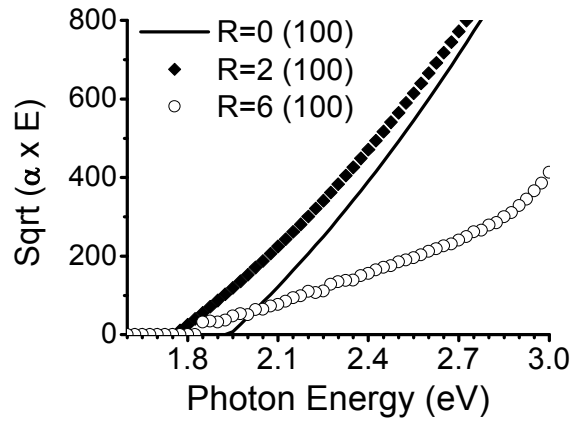
Fig.4: Tauc's plot ($\sqrt{\alpha \times E}$) as a function of photon energy (E) for the Si:H i-layers deposited with different R and on (100) wafers.

To understand the wafer orientation dependence of τ_{eff}, i-layer structure and optical properties are determined from VASE measurements on the same samples used for lifetime testing. Figure 3 shows the imaginary part of the pseudo dielectric constant, ε_2, as a function of photon energy (E) for i-layers deposited on (100) and (111) wafers at R=6. A broad featureless spectrum for the R = 6 i-layer on Si (111) wafer is indicative of amorphous Si:H structure. However, the same Si:H layer deposited on (100) wafer exhibits the identical optical constants as crystalline silicon, which implies that the film is epitaxial; this is confirmed by transmission electron microscopy (TEM). This indicates that any epitaxial growth of i-layers severely deteriorates the surface passivation quality of the deposited layer and τ_{eff} drops to less than 10 μsec (see Figure 1). Figure 4 compares the Tauc's plot ($\sqrt{\alpha \times E}$, α is the absorption coefficient) of 10 nm Si:H layers deposited on (100) wafers with different R. A very low absorption coefficient of the Si:H layer grown at R = 6 is consistent with the crystalline nature of the film. Interestingly, the optical band gap of the i-layer is wider by ~ 0.2 eV at R = 0 compared to the film deposited with R = 2. The poly-silane contribution in Si:H film growth at R = 0 results in wider band gap with higher SiH_2 bonding and microstructural defects for both DC and RF processes with an enhanced effect in the DC discharge.

(2) Front junction SHJ cells with high V_{OC}.

After completion of the i-layer characterizations, the same samples are fabricated into front junction SHJ cells by depositing standard p- and n-type a-Si:H followed by the ITO and metal contacts. The J_{SC} values are similar (~32 mA/cm^2) for all the devices, while the cell efficiencies change with R in i-layers due to changes in V_{OC} and FF. Figure 5 shows the variation of V_{OC} and FF of the cells as a function of R for the i-layers. Interestingly, V_{OC} exhibits pronounced wafer orientation dependence in region III (R = 6), while FF exhibits only plasma process dependence for R = 0. V_{OC} correlates well to the variation of τ_{eff} with R shown in Figure 1, and decreases to ~ 600 mV for the i-layer deposited with R = 6, demonstrating the necessity of high τ_{eff} and good surface passivation quality to achieve high V_{OC}. However, a high value of τ_{eff} alone does not insure a high efficiency device because the FF decreases drastically to < 50% with an "S" shape J-V for the i-layers grown at R = 0, despite exhibiting τ_{eff} > 500 μsec.

Figure 5. (a) Open circuit voltage (V_{OC}), and (b) Fill factor (FF) of SHJ cells on Si (100) and (111) wafers with 10 nm Si:H i-l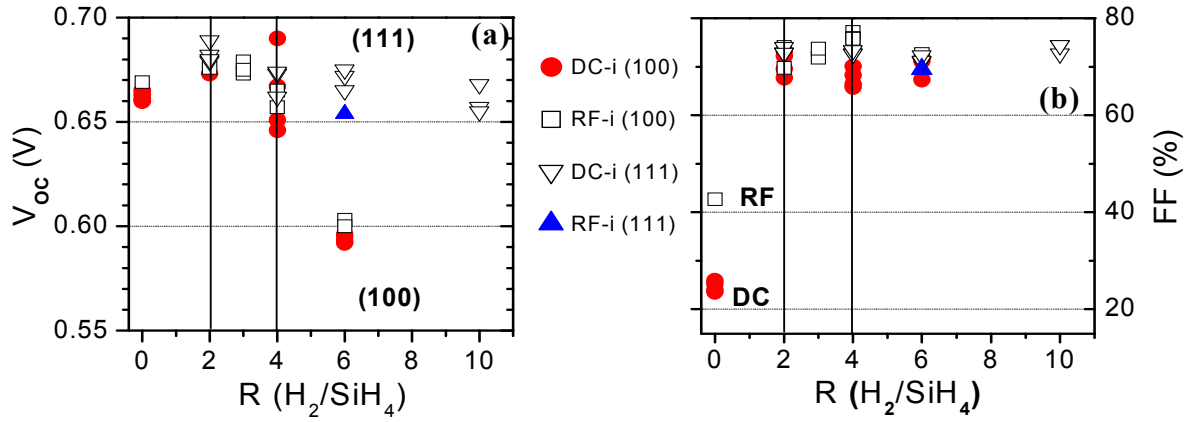ayer deposited on both sides by RF and DC plasma process with varying H_2 to SiH_4 ratio (R). At R > 4, τ_{eff} and V_{OC} show wafer orientation dependence, while at R < 2, τ_{eff} and FF exhibit plasma process dependence.

To understand the source of the "S" shape J-V curve, we fabricate SHJ cells with a 10 nm i-layer either at the front (emitter side) or at the rear (back surface field side) of the heterostructure. Figure 6 (a) compares the J-V characteristics of the cells without any buffer layer (p-n-n$^+$), 10 nm buffer layer in the rear (p-n-i-n$^+$), and 10 nm buffer layer in the front (p-i-n-n$^+$). The figure indicates that the J-V performance of the device with rear buffer layer is essentially identical to that of no buffer layer. A high FF (77%) of the device with rear buffer layer suggests that there is no carrier transport issues due to any band mismatch at the rear end of the device. However, insertion of a front buffer layer exhibits a very low FF and high V_{oc} with an "S" shaped J-V curve. Therefore, the front buffer layer severely affects the carrier transport across the heterojunction and leads to a low FF.

Figure 6 (b) shows the band diagram of SHJ cells with front buffer layer as obtained from AFORS-HET simulation [8]. The valence band offset (ΔE_v) increases with the insertion of a buffer layer between p (a-Si:H) and n (c-Si). Such an increased ΔE_v at the heterojunction imposes a barrier for holes and severely impedes their transport across the junction and appears as a non-ohmic series element in J-V curve. The hole current will thus be determined by the barrier width and height i.e., the thickness and band gap of the buffer layer. Therefore, it was concluded that the SHJ device performance is predominantly determined by the emitter layer properties and carrier recombination in the front of the device.
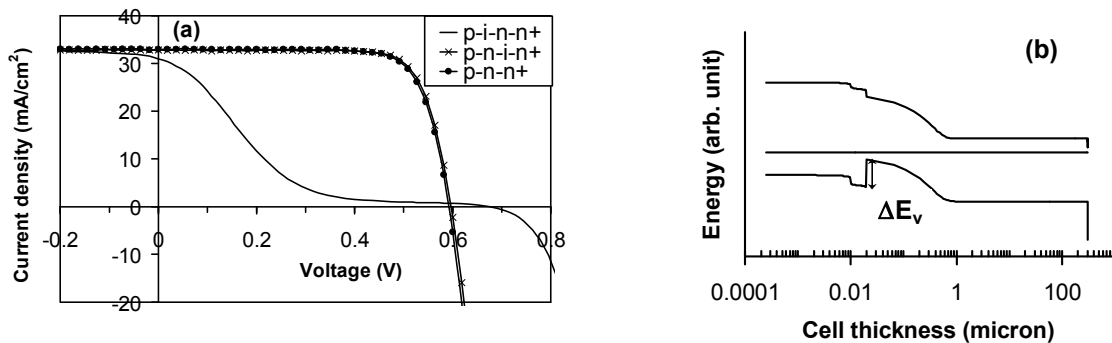
Figure 6. (a) J-V characteristics of heterojunction cells without any buffer layer (p-n-n+), with a rear buffer layer (p-n-i-n+) and with a front buffer layer (p-i-n-n+). (b) Equilibrium band diagram with a front i (a-Si:H) buffer layer between the emitter and c-Si as obtained from AFORS-HET modeling.

74

Wider band gap for the i-layer grown with R = 0 (shown in Figure 4) together with higher microstructural defects (shown in Figure 2) severely inhibits hole transport across the i-layer over a large valence band offset in the emitter side and reduces FF. On the other hand, epitaxial nanocrystalline growth at R = 6 narrows the band gap of the deposited layer and therefore does not affect hole transport and FF, but results in low V_{OC} due to insufficient surface passivation. Consequently, the highest SHJ cell efficiency was obtained for i-layers deposited with R = 2.

Figure 7 shows the J-V curve for SHJ cells fabricated on polished Fz (100) and textured Cz wafers with an R = 2 i-layer [9] confirmed by NREL. J_{SC} increases by ~ 5 mA/cm^2 due to light scattering on textured wafer and results in an efficiency of 18.4%, while V_{OC} and FF remain almost the same for both devices. This implies that the texturing scheme of the n-type Cz wafer does not have any deleterious effect on the surface passivation or on cell performance.

	Textured Cz	Polished FZ
V_{OC} (V)	0.694	0.687
J_{SC} (mA/cm^2)	35.68	31.14
FF (%)	74.17	74.96
Efficiency (%)	18.35	16.05
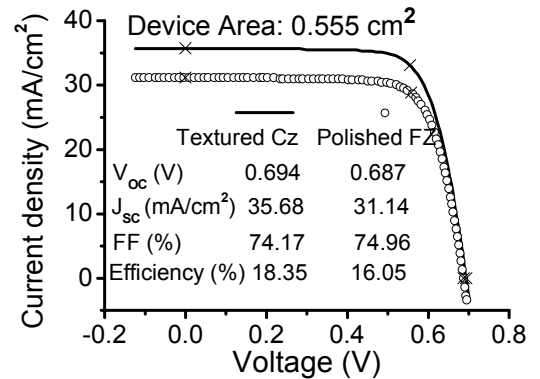
Figure 7. J-V characteristics of silicon heterojunction cells on n-type polished FZ (100) and n-type textured Cz wafers as measured by NREL.

(3) IBC-SHJ solar cells.

Figures 8 (a) and (b) shows the schematic structure of the front junction SHJ and IBC-SHJ cells, respectively. All the a-Si:H layers are deposited using identical plasma conditions in both cell structures. The i-layers are deposited with R = 2, which offers an optimum front junction SHJ cell performance as discussed in the earlier sections. The illuminated J-V curves are compared in Figure 8 (c). The V_{OC} values (~690 mV) are the same in both structures, while J_{SC} is higher (~ 3 mA/cm^2) in the IBC structure due to reduced optical loss at the front illuminating side. However, the FF in this IBC structure is very low due to the "S" shape J-V curve. This result indicates the necessity of further optimization of IBC-SHJ solar cells. There are two major functional differences between the front-junction and IBC device structures: (i) the carrier transport is one dimensional in front-junction SHJ cell, while the IBC-SHJ structure has a two dimensional transport mechanism, and (ii) the front i-layer in front-junction SHJ cell gets illuminated and generates photo carriers, while the i-layer in the IBC structure is in the dark and does not generate carriers.
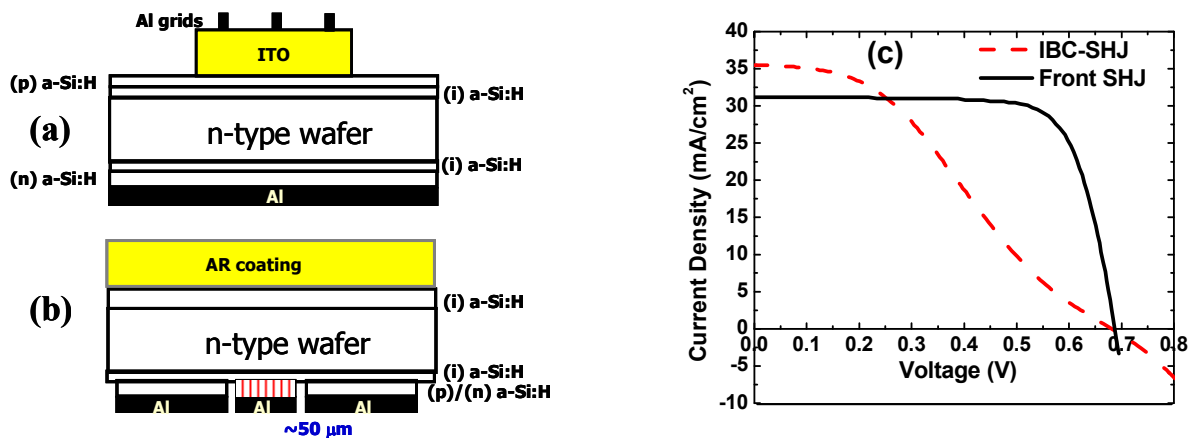
Figure 8. Schematic structures of (a) front junction SHJ cell, (b) IBC-SHJ cell and (c) comparison of the illuminated J-V curves in two cell structures.

(4) 2D numerical simulation of IBC-SHJ solar cell.

We have performed 2D numerical simulation using "Sentaurus Device" simulator (called DESSIS in its old version). The details of modelling have been discussed elsewhere [10]. Both the experimental results and numerical simulation confirm that low FF with an "S" shape J-V appears in IBC-SHJ structure due to the presence of an intrinsic a-Si:H buffer layer only in the p-type emitter strip. This suggests the existence of a hole transport barrier across the intrinsic a-Si:H buffer layer.

The low FF and "S" shape J-V can arise from the hole transport barrier due to the enhanced valence band offset generated by the intrinsic buffer layer.

Figure 9. Simulated J-V curves for IBC-SHJ cells [structure shown in Figure 8 (b)] under illumination with variable band gap of the intrinsic a-Si buffer layer.

Hence the effect of band gap of the intrinsic a-Si buffer layer on IBC-SHJ cell performance is studied. Again, the surface passivation effects of the different buffer layers are assumed to be the same, while electron affinities of the buffer layers are assumed constant. Figure 9 shows the illuminated J-V characteristics obtained from simulation for intrinsic a-Si buffers as a function of band gaps. A substantial effect of the band gap is evident on FF, which increases from 55% to >78% as the band gap of the buffer layer is reduced by 0.07 eV.

To simultaneously maintain high V_{OC} and J_{SC} with narrower band gap buffer layers, high passivation quality of the buffer layer is also required. Intrinsic a-Si:H buffer layers with narrower band gaps are developed by varying plasma process parameters without alloying with other semiconductors like Ge. Figure 10 (a) shows the Tauc's plot for two different a-Si:H layers, where the dashed (black) curve represents the control buffer layer, and the solid (red) curve indicates the newly developed i-layer. It can be seen that the band gap of new i-layer is ~0.04 eV narrower than that of the control layer. The τ_{eff} values shown besides the curves indicate that they have similar passivation quality. Figure 10 (b) compares the illuminated J-V curves for the IBC-SHJ cells with 5 nm narrower band gap i-layer and 10 nm higher band gap i-layer. An IBC-SHJ cell with efficiency of 13.5% and FF of 77% is achieved with the narrower band gap i-layer. However, the V_{OC} and J_{SC} is lower than the standard i-layer, which is due to insufficient surface passivation in the gap between the p- and n- strips.
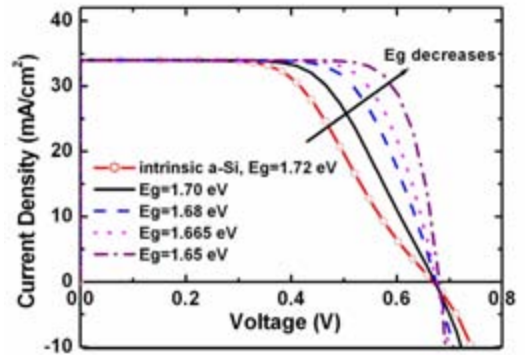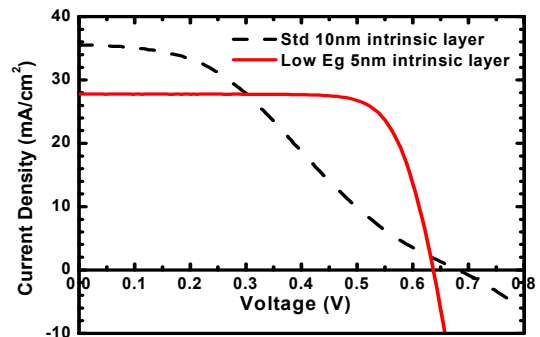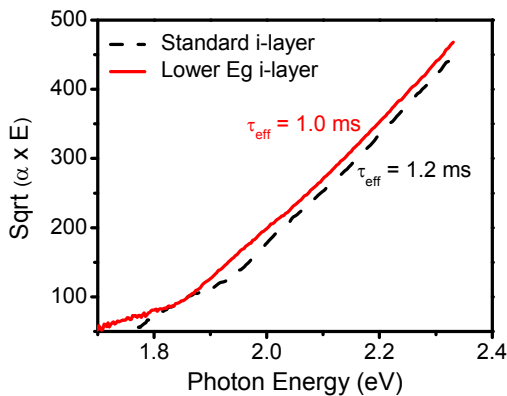

Figure 10. (a) Tauc's plot for control (black curve) and newly developed (red curve) intrinsic a-Si:H layers. (b) illuminated J-V curves of IBC-SHJ cells with a 5 nm lower band gap i-layer and 10 nm standard i-layer.

Conclusions

In conclusion, SHJ-IBC solar cells provide a substantial advantage to fabricating high-efficiency low-cost solar cells. The SHJ solar cell performance is primarily governed by the passivation quality of the intrinsic a-Si:H buffer layer and the hole transport across the emitter side. The front junction SHJ cell efficiency of 18.4% with V_{OC} of 694 mV is achieved on textured Cz wafer using DC plasma deposited i-layer. The IBC-SHJ structures show promise towards improvement of J_{SC}, while maintaining high V_{OC}. Further optimization of the i-layer as guided by 2D numerical simulation is in progress to improve FF for high efficiency all back contact SHJ solar cells.

Acknowledgment

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Challenges With Testing High-Efficiency Si Solar Cells and Modules

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ABSTRACT: High efficiency silicon solar cells present difficulties in IV-curve measurement due to their slow time response to varying light intensity or ramped voltage. Even on-sun measurements can be influenced by the time response of the module if the voltage ramp rate is too high during measurement. For flash testing, the constraints are even tighter since the flash intensity may be changing with time in some methods, or the voltage is ramped during a relatively short period of constant light intensity. This paper discusses the device physics that determine the time response of silicon cells and presents a strategy for obtaining accurate measurements from using a multi-flash technique with short flash pulses. Complemented with use of the Suns-Voc technique, a comprehensive module testing methodology is presented.

1 OVERVIEW

High-efficiency silicon solar cells have very slow time response to changes in voltage or light. This is due to the fact that high efficiency cells operate at high voltages which imply large amounts of stored charge. If this charge is discharged during the measurement, the measured currents are inflated relative to the steady-state measurements. If the stored charge is increased during the measurement, then the measured current is low compared to the steady state.

These trends are well known and have been documented [1,2,3,4]. In recent years, especially with Sanyo and SunPower cells and modules, these errors can be intolerably large, requiring very long pulses and slow voltage ramp rates for accurate module or cell measurement[3]. One solution to this problem is to measure one I-V point per flash, while holding the voltage constant throughout the measurement to limit the effects of the capacitance[2,4]. This is commonly referred to as the "multiflash" technique, which has been used for high-efficiency cell measurements since at least the early 80's. Significant errors still arise even using this constant-terminal-voltage-per-flash technique on the latest high-efficiency modules[4].

As an example of the errors that can result in both steady state and flash-test measurement of solar modules or cells, consider the common case of ramping the voltage linearly from short circuit to open-circuit voltage of a module or solar cell. PC1D simulations of this case are shown for a hypothetical backside-contact solar cell with an open circuit voltage of 720mV in Fig. 1. Simulated data from voltage ramp rates corresponding to short-circuit to open circuit in 2, 5, 10, 20, 50 and 100ms are shown, and compared to the simulated IV curve that would be taken with a very slow steady-state measurement.
Fig. 2 indicates that in order to measure this type of cell accurately within 1% with a linear voltage ramp

rate, the ramp time would need to be greater than 100 ms. This has implications not only for flash testing, but in the maximum voltage ramp rate to be used under steady-state illumination conditions.
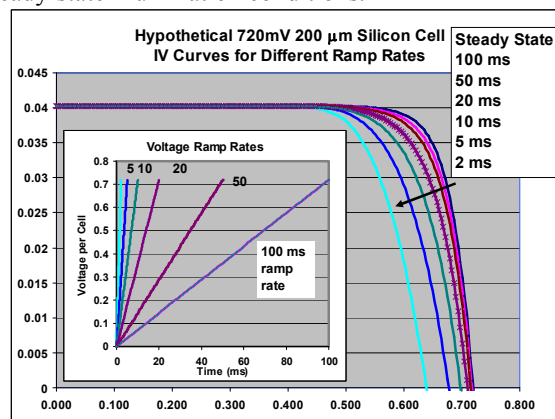
Figure 1: PC1D[3] simulations of the of the IV curves that would result from taking data at different ramp rates from short-circuit to open-circuit voltage.
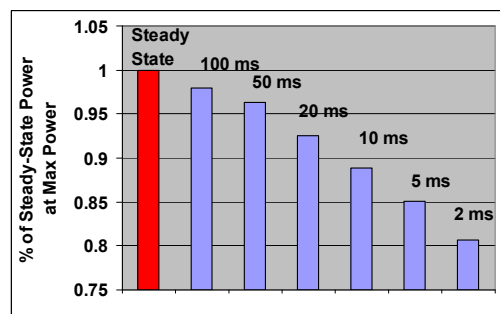
Figure 2: A comparison of the power (or efficiency) that would be reported for each of the curves in Figure 1.

Long-pulse simulators are a viable approach for measuring these cells or modules. However, simulators with 100 ms pulses require very large capacitive energy storage and substantial flash power supplies and therefore can have high cost of ownership.

2. MULTI-FLASH METHODOLOGY:

A different strategy to obtain accurate measurements is to improve upon the constant-voltage multi-flash concepts in order to use short pulses to make accurate measurements of high-efficiency silicon solar cells.

Figure 3: A PC1D[3] simulation of the time response for an idealized 1D backside-contact solar cell. The cell is held at the one-sun maximum power voltage during the light pulse. The current is shown as a function of time, and compared to the steady-state value that would be measured at each light intensity.

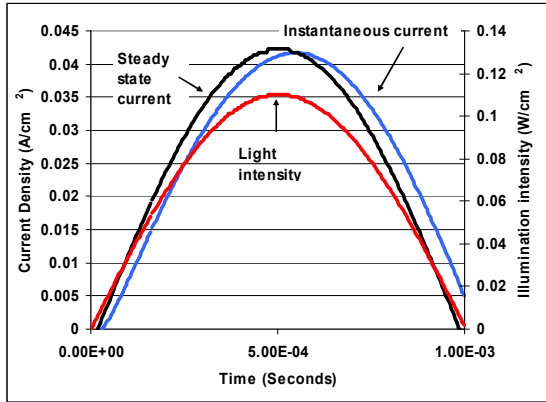An illustration of the time response of a solar cell to a pulse of light at constant terminal voltage is shown in Fig. 3, based on a PC1D simulation of a 1D approximation of a 2004-era SunPower high-efficiency backside contact solar cell. First, the steady state current is shown at each light intensity. This is compared to the instantaneous current that would be measured if the light were swept in 1 ms, as shown in the graph.

Compared to the steady-state response, the instantaneous measured current during a flash pulse is low on the rising side of the light pulse, peaks late, and then is high on the falling side of the pulse. This characteristic leads to errors when using short light pulses to measure high-efficiency solar cells or modules. In contrast to the behavior in Fig. 3, Figure 4 shows the behavior of the solar cell under the same flash pulse shape when the voltage is modulated during the flash pulse to force the current to be in phase with the light.

The appropriate modulation for this modeled cell was
$$V = (0.605 - 0.647 * J) \text{ Volts},$$
where J is the terminal current density.

Further modeling was used to illustrate the mechanism behind this interesting result. Fig. 5 shows the carrier density profile across the cell at various times during
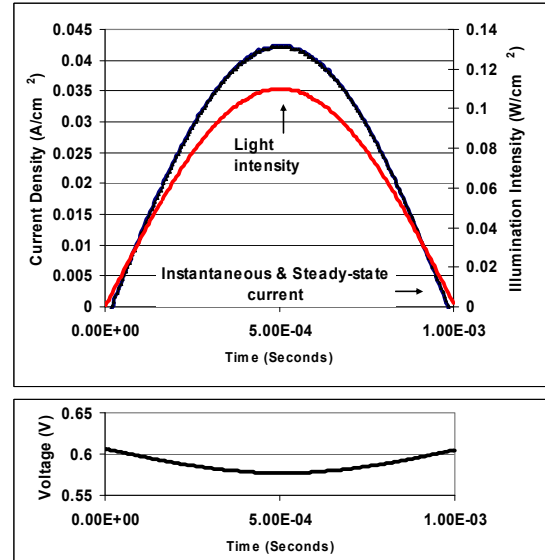
Figure 4: A plot of Current density and intensity vs. time, as in Fig. 3, but for the case when the voltage is modulated during the pulse as shown (bottom). The voltage at one sun is the same maximum power voltage as the constant voltage in Fig. 3. The instantaneous current is the same in this case as would be measured in the steady state at each voltage-intensity point during the pulse.

this light pulse for the constant terminal voltage case shown in Fig. 3. The carrier density profile is relatively flat prior to the pulse, then increases to a peak before flattening out again.

The modulation at the back of the solar cell (the junction in this backside-contact case), is due to voltage modulation at the junction. Even though the terminals of the cell or module are held at constant voltage, inside the solar cell the local junction voltage will modulate due to the product of cell and wiring series resistance and current density. In the front of the cell, the carrier density modulation during the pulse is even more pronounced. This is due to the pileup of carriers that are photogenerated near the front of the cell. This pileup creates the gradient that drives the diffusion current towards the back junction.

Clearly, there is a lot of charging and discharging of the electron-hole charge in the cell during this light pulse. This accounts for the slow time response and the differences in current measured between the instantaneous case and the steady-state case.

Contrast this with the carrier-density profiles in Fig. 6, which correspond to the output characteristic shown in Fig. 4 with terminal voltage modulation during the pulse. The carrier density at the front of the cell still increases during the pulse. The carrier density at the back of the

cell is intentionally pulled down during the pulse by the voltage modulation. The total integrated charge in the cell is constant at each point in time. There is no charging or discharging of the cell charge during the pulse. Therefore the measured current will be the same as in the steady-state case.
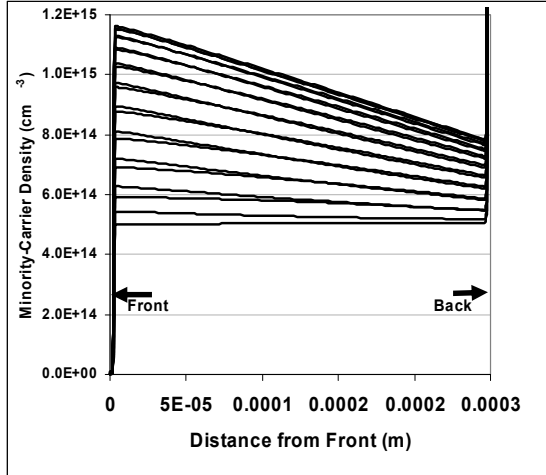
Figure 5: The carrier density modeled for a backside-contact solar cell during the pulse shown in Figs. 3 and 4. The terminal voltage is held constant at the maximum power voltage. The carrier density is initially flat (prior to the pulse), then increases to a maximum shortly after the peak intensity before falling back to the flat profile after the light pulse.
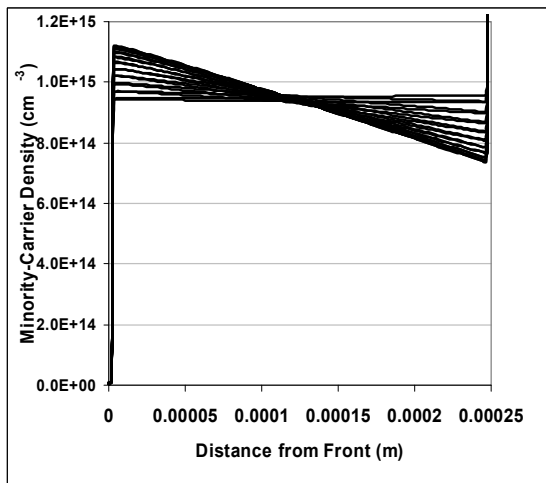
Figure 6: Carrier density profiles during the light pulse shown in Figs. 3 and 4, but with the voltage-time profile shown in Fig. 4. Although the profile changes during the pulse, the total charge in the cell does not.

The voltage modulation compensates for series resistance and is also used to counter-balance the carrier density gradients in the cell. The time response is determined only by the time that it takes to re-distribute this constant charge in the cell. Instead of

constant terminal voltage during the light pulse, the goal is essentially to have constant voltage in the center of the wafer thickness during the pulse.

3 EXPERIMENTAL

We tested the new method by measuring high efficiency modules with a variety of flash-pulse durations.

The flash pulse shapes are shown in Fig. 7, and referred to as "Full", "1/2", and "1/4" pulses, with pulse widths at half maximum of about 6, 3, and 1.5 ms. For this paper, the power output of the module was measured at one sun during decay side of the flash-intensity pulse. We measured the characteristics of a purchased Sanyo HIP-190 module. Of the available modules that we had, this was the one with the slowest time response, about 3X slower than the SunPower modules reported in ref. [4]. We used a "multi-flash" method with one pulse per I-V point on the curve.

The results are shown in Fig. 8. Here, we plot the power vs. voltage (per cell) for the module from testing with each of the pulse types shown in Fig. 7. The data have been normalized to the steady-state results, where the steady state maximum power is given as unity. Fig. 8 (top) shows the case for measurements with constant terminal voltage during the light pulse. With the full pulse, the power is already measured higher than the steady state value. This indicates that even this longest pulse width was not long enough for accurate measurements on this module. The half and quarter pulses have increasing errors with the 1/4 pulse showing a very obvious distortion to the power curve.
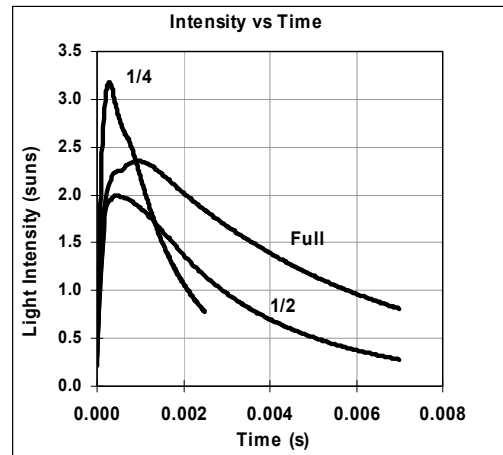
Figure 7: Three flash-lamp pulses used in this study. Data were taken at one sun on the trailing edges of each of these pulses.

The data at the bottom of Fig. 8 show the case with modulated voltage during the light pulse as is proposed in this paper. In this case, all three sets of data lie on the same curve, and the maximum power that is reported is

the same as the steady-state result. This is quite remarkable, especially in the case of the 1.5 ms pulse. By comparing the data from the top curves and the bottom curves, it is clear that with the new technique very short pulses can be used compared to what would be required for accurate measurements using the constant voltage technique. The same voltage modulation as a function of terminal current was used for all three pulse types, indicating that this is a function of the module, not the pulse time profile. This is the result to be expected from the modeling results.
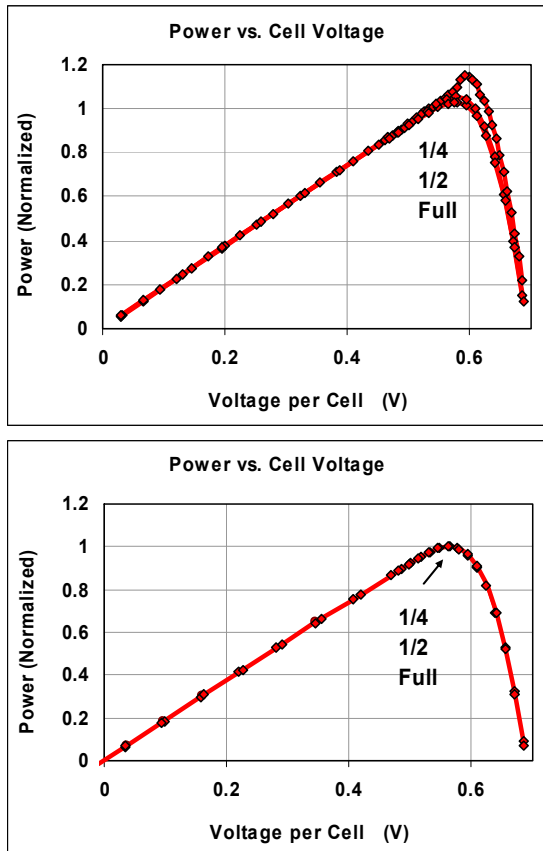
Figure 8: For the case of constant terminal voltage during the pulse (<0.5V/sec/cell), the power curve has a strong dependence on the pulse shape (top). The maximum power is reported higher for shorter pulses. For the case where the voltage was modulated during the light pulse as proposed in this paper (bottom), the power curve is independent of the pulse shape. The data overlays.

A summary of the measurement errors in the power for these tests is given in Fig. 9. The error (compared to the steady-state result) is shown for the 3 pulses from Fig. 7 for both the constant-terminal-voltage and the modulated-terminal-voltage cases. The intensity slew rate at one sun is also shown on the x-axis for each pulse type. For the case of constant voltage during the pulse, the Sanyo module was measured 3%

high even with the longest pulse, indicating that this pulse was not long enough for accurate measurement using this method. The error was 6% with the half pulse, and 15% with the 1/4 pulse.

Using the strategically modulated voltage during the pulse, the errors were insignificant in each case. The measured results were independent of the pulse shape. The same power was measured from the module within 0.2% from the longest to the shortest pulse. The voltage modulation for the maximum power point is shown in Fig. 10. For a maximum power voltage for this module of about 56 volts, the modulation amplitude at one sun intensity was 5 Volts down from the voltage at no current. At the peak intensity of 2.2 suns, the voltage was modulated by about 10V.
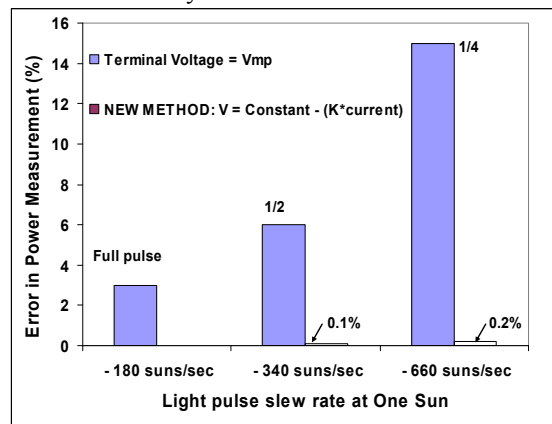
Figure 9: The errors (difference between measurements during a flash pulse and the steady state result) for the three pulse shapes shown in Fig. 7. For the case of constant voltage during the pulse, the errors were large. For the method proposed in this paper, the errors were insignificant.
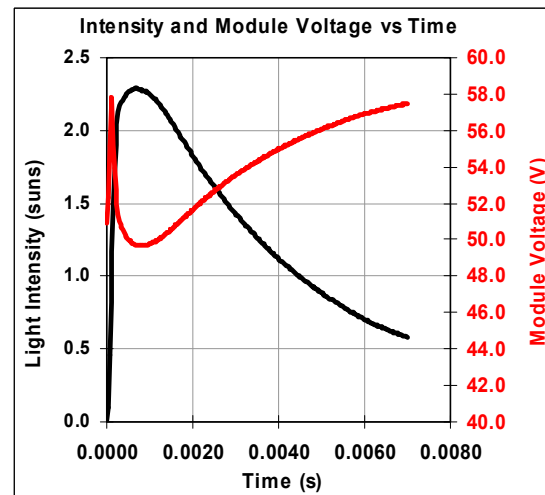
Figure 10: The amplitude of voltage modulation used to obtain the results shown in Fig. 8 and Fig. 9.

81

3. ADDITIONAL DATA FROM SUNS-VOC

Fig. 11 shows discrete data points taken in the method described here, along with the Suns-Voc curve for the device. The Suns-Voc curve is taken with a single flash, where the voltage at each intensity is transformed into the form of a light IV curve using the principle that neglecting series resistance, the solar cell voltage is determined by the difference between photogeneration and extracted current[7,8]. In other words, the open-circuit voltage at 0.05 suns differs only by series resistance from the case of the operating voltage at 1 sun when 95% of the current is extracted as terminal current.

This Suns-Voc curve gives an upper bound on the efficiency possible for this module, and is determined primarily by the solar cell material quality, surface passivation, metal contact areas, and shunting. It represents the upper bound on the efficiency that could be extracted from these solar cells. Its tremendous advantage is the wealth of detailed information contained within this curve that are clearly displayed without interpretation or modeling assumptions. Effects such as the varying ideality factors due to material quality or surface passivation are all contained within this curve.

The interesting point in comparing this Suns-Voc curve to the actual IV data is that the DIFFERENCES between the curves highlight the losses due to series resistance and module fabrication. For example, the best measure of the series resistance loss for the module is the difference in voltage between the Suns-Voc curve and the IV data at the maximum power current. If this exceeds what was measured at the cell level, it could indicate a problem in module design or fabrication.

Also, the notches shown on the short-circuit side of the curve are a clear indication of cell mismatch (or simulator non-unifomity). These are caused by individual cells that are performing at low currents. Detailed experiments have shown that these losses, compared to the Suns-Voc curve corrected for the measured series resistance, provide a very accurate measure of the cell mismatch losses[9].

4 CONCLUSION

This paper presents a methodology for measuring high-efficiency silicon solar cells or modules using short flash pulses. The terminal voltage of the cell or module is modulated during the light pulse in order to maintain constant charge in the solar cells. This neutralizes the effects of the cell capacitance on the
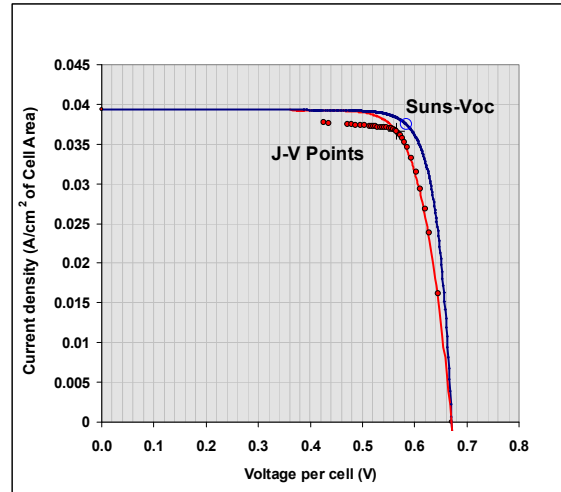
Figure 11: A comparison of discrete IV-curve data points to the Suns-Voc curve.

measurement. When this is done, there is no charging or discharging of the cells, and the measured instantaneous current is found to be the same as the steady-state result at the same intensity and voltage.

The method is self-validating, with the accuracy between the flash data and steady state data indicated by the phase of the terminal current with respect to the incident light intensity. This offers a multiple short-flash alternative to the "long pulse" simulators of 100 ms or longer that have sometimes been considered as necessary for accurate measurements of high-efficiency silicon modules.

Combined with the use of the Suns-Voc technique, a complete characterization of shunting, cell mismatch and/or illumination non-uniformity, and a separation of series resistance from other device characteristics can be accomplished.

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Mechanical Properties of Multi-Crystalline Silicon: Correlation with Impurities and Structural Defects

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A primary factor impacting the failure of silicon PV wafers is the formation and advancement of a microcrack, which is intimately related to residual stresses and defects developed in the wafer during crystal growth and processing. We have addressed this issue from a fundamental materials science perspective via experiments on pressure-induced deformation, which enables one to understand the complex roles of crystallinity, defect/impurity interactions, residual stresses and wafer thickness on failure mechanisms that are activated under stress. At last year's workshop we showed that differences in mechanical properties between various grains in the same mc-wafer were impacted by variations in impurity type and concentration, defect classification, specific grain orientation, and the local value of residual stress. Our recent studies have used nanoindentation to explore the effects of crystallographic orientation variation across a planer 2D cast mc-Si boundary, both a twin and a grain boundary (GB); as well as impurity contamination(Fe and Cu) of the interface of a unique 110/100 GB, intentionally constructed close to and parallel with the sample surface via a direct-silicon-bonding (DSB) process.

During increasing nanoindentation loads, Cu-contaminated GBs show a gradual <u>decrease</u> in hardness, whereas an <u>increase</u> in hardness occurs at Fe-contaminated GBs. Interestingly, both clean and Fe-contaminated samples displayed abrupt hardness changes due to the presence of GB-induced local deformation, while Cu-contaminated samples exhibit a gradual weakening. Grain orientation also influenced the mechanical behavior and has been verified by EBSD (Electron Back Scatter Diffraction) of mc-Si wafers which illustrates grain-to-grain and across-grain crystallographic orientation variations and their influence on hardness during nanoindentation. Program to correlated the above mechanical property dependencies with crack initiation and propagation behavior will be outlined.

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Lifetime and diffusion length mapping and imaging techniques for silicon solar cells

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Abstract

Lifetime and diffusion length are useful parameters for monitoring material quality, processing, and cell performance. For lifetime, an example of microwave reflection mapping, photoluminescence imaging, and carrier density imaging is shown. Light beam induced current maps are also compared to electroluminescence images for diffusion length measurements.

Introduction

The minority-carrier lifetime and related diffusion length are important parameters in semiconductor solar cell devices since they relate to material quality and collection efficiency. Many techniques for measuring or monitoring lifetime have been developed[1,2]. Popular techniques based on photoconductivity have been commercialized and available for many years. These include the Sinton lifetime tester[3] and the Semilab lifetime scanner[4]. The Sinton tester can measure lifetime by monitoring a photoconductivity transient for long lifetimes or by using quasi-steady state for short lifetimes[5], while the Semilab scanner measures microwave reflection transients[6,7]. Free carrier absorption allows for an all-optical technique to probe the concentration or decay of minority carriers, and several variations of this measurement have been assembled[8-10]. Time-resolved photoluminescence (TRPL) is also an optical technique that has long been applied to direct-gap semiconductors[11]. While the above techniques have generally been applied to measure single points of a sample, and possibly scanned around to make maps, recent advances in technology have produced detector arrays in cameras such that some lifetime-related properties can be imaged to quickly provide high resolution two-dimensional lifetime measurements. Photoluminescence (PL) imaging[12-14] is the steady-state, camera-based equivalent of TRPL and takes advantage of the high sensitivity and large pixel counts of the Si charge-coupled device (CCD) camera market. A commercial system is expected to be available soon[15]. The same type of camera can also be used to collect electroluminescence[16,17] (EL) data images from a finished cell, which can be compared to diffusion length typically measured by light-beam induced current[1] (LBIC) or electron-beam induced current[1] (EBIC). Carrier density imaging[18,19] (CDI) is the steady-state, camera-based equivalent of optical free carrier absorption measurements. Technology of infrared cameras is also quickly growing, providing larger detector arrays for better resolution. CDI monitors infrared absorption or emission of excess minority carriers and is also under commercial development[20]. The same type of infrared camera can also be used for dark and illuminated lock-in thermography for the rapid imaging of shunts in finished cells[21]. There are also similar imaging technologies for series resistance imaging[22].

Semilab Lifetime Mapping

The Semilab wafer scanner is capable of quickly measuring photoconductive decay transients by the microwave reflection technique. The excitation light consists of 200 ns pulses with 904 nm wavelength. The maximum power corresponds to 1.2×10^{13} photon/pulse, and this power can be varied depending on the sample. The spot size is 1.1 mm in diameter, so assuming the carriers

are quickly distributed in the thickness of the wafer after excitation, the carrier injection level is roughly 10^{17} cm^{-3} or lower. The microwave source has a frequency near 10 GHz and is also adjusted for the particular sample. The measured lifetimes can range between 0.1 μs and 30 ms, and the system can measure samples with a resistivity between 0.1 and 1000 Ω-cm. The transients are acquired at a rate of roughly 30 ms per measurement point, so a 100 mm diameter wafer would take approximately 4 minutes to measure with a resolution of 1 mm.

An n-type double-sided polished CZ Si wafer was chosen for lifetime measurement and comparison. The wafer is 100 mm in diameter and 500 μm thick. It is nominally in a range of 1 to 10 Ω-cm resistivity, or a doping of roughly 10^{15} cm^{-3}. Although this single-crystal wafer initially had uniform high lifetime, it was intentionally contaminated with iron to produce regions of varying lifetime. A speck of iron-sulfide, approximately 1 mm^3 in size, was dissolved in a large beaker, ~500 ml, of deionized water. A drop of this solution was dropped onto the surface of the wafer. Other drops of further diluted solution were also added to the wafer, and then the wafer was heated in a small atmospheric furnace at ~800º C for ~1 hour. The Semilab lifetime map of this wafer is shown in Fig. 1a. The scan resolution was set to 0.25 mm, even though this is smaller than the beam spot, to show the best possible resolution for this system. At this fine resolution, the scan took ~1 hour to complete.

Photoluminescence Lifetime Imaging

We collected PL imaging data using a Si CCD camera from Princeton Instruments/Acton. This model, PIXIS 1024BR, has a 1024 x 1024 array of 13 μm square pixels and is back illuminated and deep depleted for best quantum efficiency out to 1100 nm. The detector is cooled to -75ºC. A Schneider Optics Cinegon compact lens is mounted to the camera, along with a stack of two 810 nm notch filters around a Schott RG1000 black glass filter. The filter stack is designed to sufficiently attenuate reflected light from the 60 W, 810 nm laser diode excitation source. The fiber output from the laser diode is expanded to the sample area by a collimator and engineered diffuser. Figure 1b shows the PL image from a 1 s exposure and 30 W of laser diode power.

Carrier Density Imaging

CDI data was acquired using an ElectroPhysics/Cedip Silver 660M InSb infrared camera. This camera has a 640 x 512 array with 15 μm pixels and a spectral response from 3.6 to 5.1 μm. A built-in Stirling stage cools the detector to ~76 K. It also has a built-in lock-in feature and a maximum frame rate of 100 Hz for the full detector. We collect CDI data in the lock-in mode, and in this case, the laser diode is pulsed on and off with a square wave of 27 Hz. A hot plate having its surface spray-painted with flat black high-temperature paint, is used as a black body source, usually between about 50º and 100º C. Figure 1c shows the wafer's CDI data, which is the module, or amplitude, plot of the lock-in acquisition. Using the 100 Hz frame rate, approximately 1000 frames, or about 30 cycles, are analyzed in about 10 s.

At several coordinates of the wafer, image pixel counts from the PL image data and the CDI data are plotted against the corresponding lifetimes from the Semilab map. As shown in Fig. 1d, there is a good correlation over the range of lifetimes in this sample.
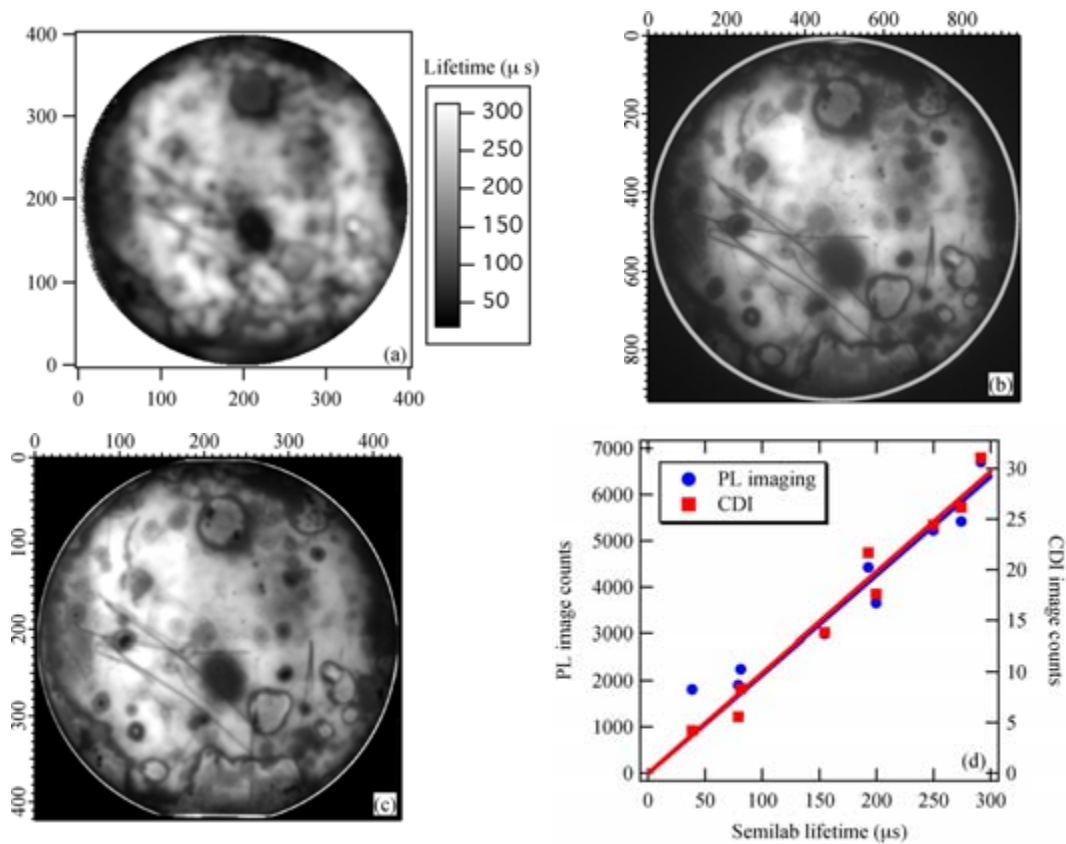
Figure 1. Lifetime of CZ Si wafer acquired from: (a) Semilab lifetime scanner, (b) PL imaging, and (c) CDI. (d) Comparison of lifetime images to Semilab lifetime values at various points.

Semilab LBIC

The Semilab scanner's LBIC option uses four wavelengths to measure current and reflectivity on a finished cell and calculate quantum efficiency and diffusion length. The four wavelengths on our system are 406, 850, 949, and 1014 nm. The 100 μm spot size allows for better resolution than the lifetime maps. LBIC for two cells are shown in Figs. 2a and 2b. Using 0.25 mm resolution for these 5-inch cells, LBIC data took nearly 20 hours to acquire for each cell.

Electroluminescence Imaging

The same Si CCD camera used for PL imaging can also be applied to collect EL data. We have used the same filter stack as PL imaging, but others have used various filter arrangements to enhance EL data and analysis[17]. We measured the same LBIC cells and show the EL data in Figs. 2c and 2d. The cells were forward biased at 0.7 V, and the camera integration time was 15 s. Histograms of both the LBIC and EL data are shown in Figs. 2e and 2f. A relative shift of the histograms shows correlation between the LBIC and EL data. Such correlation has been quantified in detail previously[16].

Acknowledgements

Figure 2. Semilab LBIC maps (a) and (b) and a histogram of values (e), EL images of the same wafers (c) and (d), and histograms of the image pixel counts (f).

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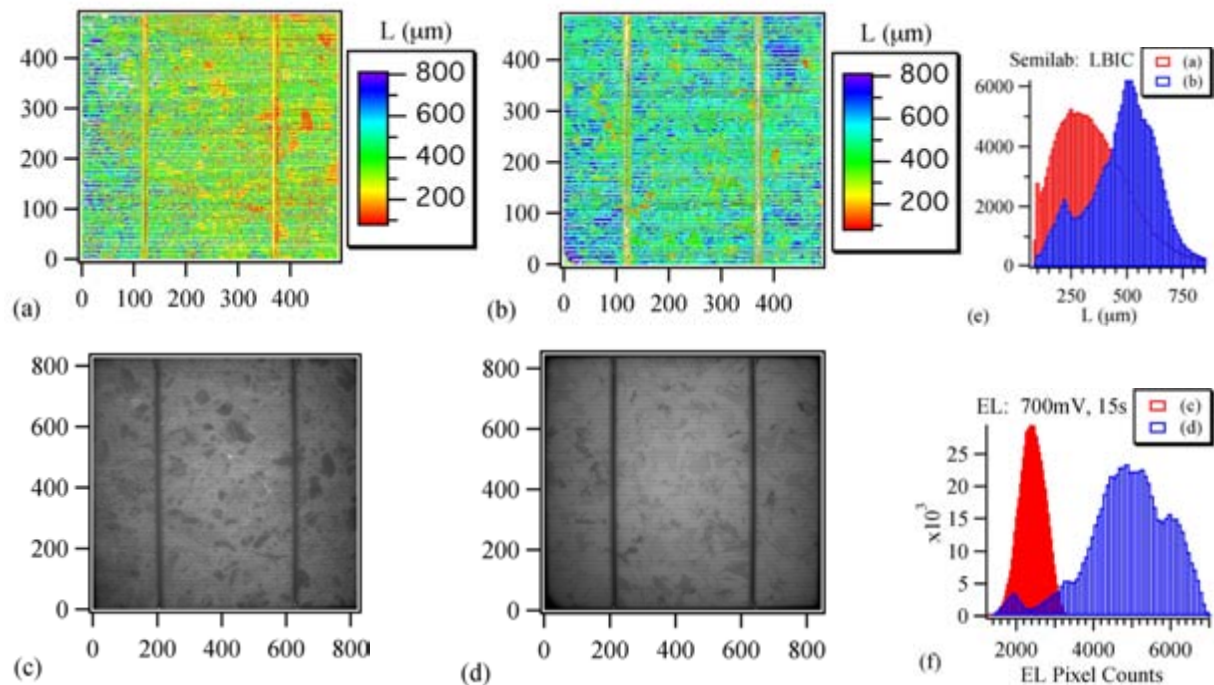[3]Sinton Consulting (www.sintonconsulting.com)

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Photoluminescence characterization of silicon wafers and silicon solar cells

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INTRODUCTION

Over the last few years we have demonstrated that non-imaging[1] and imaging[2] quasi steady state photoluminescence (QSS-PL) measurements are effective and quantitative tools for the characterization of silicon wafers and silicon solar cells. In this paper we analyze QSS-PL measurements on cast multicrystalline wafers from different positions within an ingot and at various processing stages, including as cut wafers and finished cells. Some general aspects of minority carrier lifetime measurements on Silicon wafers relevant to the analysis of QSS-PL data are reviewed.

BACKGROUND

The luminescence emission from a silicon wafer is determined by the rate of spontaneous emission from the bulk, which is proportional to the product of electron and hole concentrations. Neglecting reabsorption of photons within the wafer and assuming low injection conditions the measured luminescence intensity I_{PL} is given as[1]

$$I_{PL} = C \cdot N_{D/A} \cdot \frac{1}{d} \cdot \int_0^d \Delta n(x)dx = C \cdot N_{D/A} \cdot \Delta n \quad (1)$$

with $N_{D/A}$ the background doping concentration and Δn the average excess minority carrier concentration across the wafer thickness d. The constant C in Eq.1 is determined by the fraction of photons that can escape the sample and contribute to the measured photon flux. C depends on a wafer's optical properties such as the surface texture and the spectral reflectance.

The wafer specific parameters in Eq.1 (i.e. the product of C and $N_{D/A}$) need to be determined for quantitative QSS-PL measurements. In practice this means that a separate calibration must be carried out for each distinct type of sample. This is in contrast to, for example, quasi steady state Photoconductance (QSS-PC) measurements[3], where a calibration is performed once for a specific experimental set-up, which is then valid for most common types of silicon wafers.

EXPERIMENTS

Samples: 200 μm thick 6-inch wafers cut from a cast multicrystalline p-doped silicon ingot were investigated in a PL imaging study between REC ScanWafer and BT Imaging. Sister wafers from different positions within the same brick were investigated at different stages of processing:

- as cut,
- after Phosphorous emitter diffusion and SiN Firing,
- without emitter diffusion, with SiN firing,
- fully processed screen printed cells.

Spatially resolved Microwave Photoconductance Decay (μ-PCD) and Light Beam Induced Current (LBIC) measurements were performed using a Semilab WT-2000PV wafer tester. PL imaging on wafers and on fully processed cells was performed using a BT Imaging LIS-R1 prototype luminescence imaging system. Injection
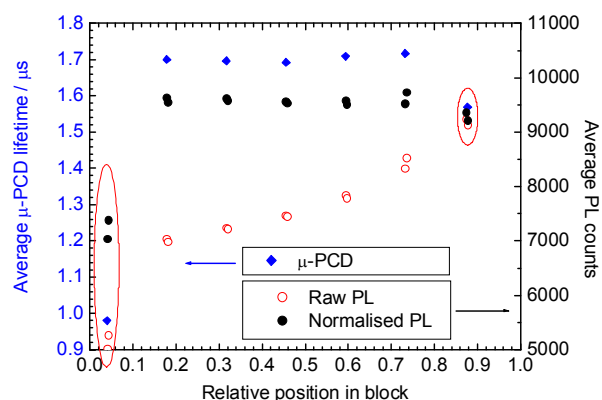
Fig.1 *Average effective lifetime from μ-PCD maps (diamonds) and average count rate from PL imaging measured on as-cut wafers as a function of the position in the brick. Open circles represent the measured average PL signal, closed circles the PL signal normalised to the nominal background doping.*

level dependent QSS-PC minority carrier lifetime measurements were performed with a Sintonconsulting WCT-120 in combination with monochromatic illumination from a high power infrared laser, both integrated into the LIS-R1 prototype. Absolute calibration of luminescence images was achieved by correlation with spatially averaged QSS-PC measurements.

As-cut wafers

PL images and μ-PCD maps were measured on as-cut wafers from different positions of the brick. Fig.1 shows the average lifetime from μ-PCD (diamonds) and the average count rate from PL imaging (calibrated PL measurements will be discussed below) as a function of the relative wafer position within the brick. An increase in the average PL signal (open circles) towards the top of the ingot is observed, which is caused by the variation of the background doping concentration $N_{D/A}$ within the ingot. That variation was modeled according to the Scheil equation[4]:

$$N_{D/A}(x) = N_{D/A}(0) \cdot K_{eff}(1-x)^{K_{eff}-1} \qquad (2)$$

a)

b)

0.18   0.3
                                          ^
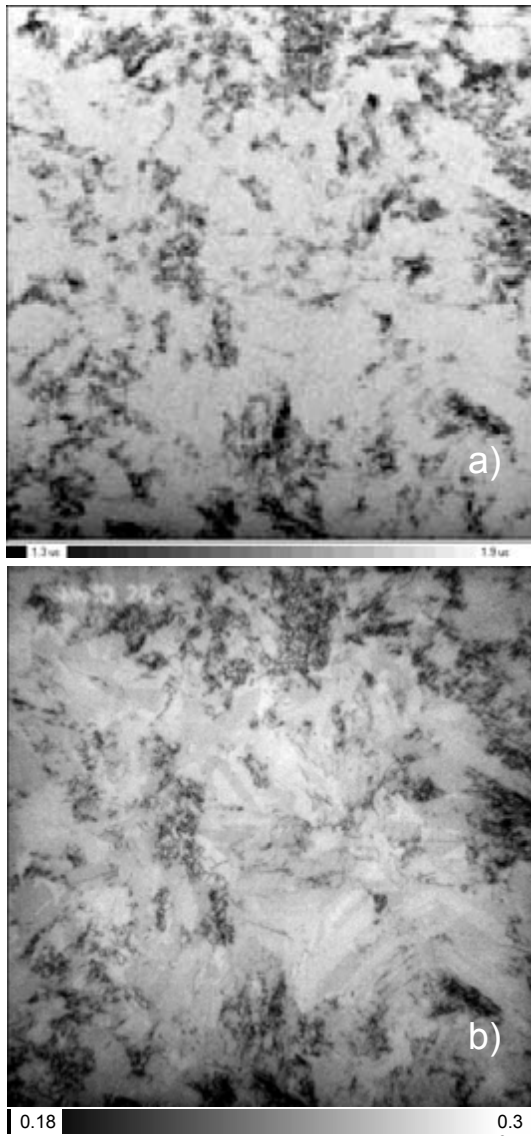
Fig.2 *Effective lifetime in μs from μ-PCD (a) and from a calibrated PL image (b) on an as-cut wafer from the central part of the brick (x=0.46).*

where x is the relative position in the brick. The measured PL data were normalized with regard to the nominal doping concentration according to Eq.2 with K_{eff}=0.84 (full circles in Fig.1). The relative variation along the brick of the normalized PL count rate is in good agreement with the relative variation of the average μ-PCD lifetime data. Both data sets show sections of low average effective lifetime at the bottom and at the top of the ingot (red ovals in Fig.1), the latter caused by high impurity concentrations (Oxygen, Carbon, transition metals), which are commonly observed in those parts of the ingot. In the middle section ($0.15 < x < 0.8$) both μ-PCD and normalized PL predict an almost constant average effective lifetime with only 2% relative variation.

The scatter of the PL data between different samples is very low. For example two sister wafers were measured with PL imaging at each position and the average PL signals for each pair vary by less than ±1%.

Calibrated measurements on raw wafers - dependence on illumination wavelength

Fig.2 shows the effective minority carrier distribution in μs of an as-cut mc-Si wafer from the middle of the block (x=0.46) obtained from μ-PCD (a) and from a calibrated PL image (b), respectively. The measurement time and spatial resolution in the measurements was ~30 minutes and 500μm for μ-PCD and 10s and 320μm for PL. Qualitatively the same features of high- and low lifetime regions are observed in both images, which is an example for the strong correlation between PL intensity and effective lifetime. Excellent correlation between the relative lifetime variations from μ-PCD and the PL intensity was observed on wafers throughout the brick.

Note however, that the two images shown in Fig.2 are plotted on different scales. The average effec-
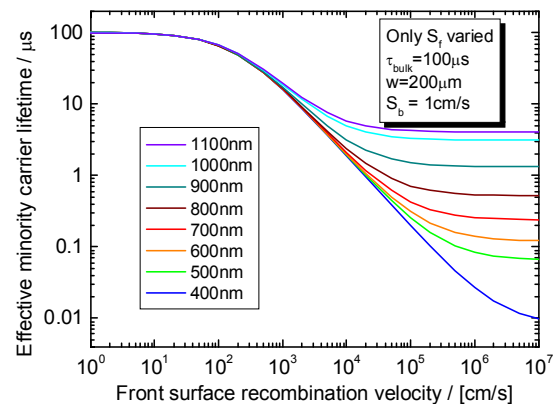
Fig.3 *PC1D simulations of the effective minority carrier lifetime measured under steady state conditions as a function of the front surface recombination velocity for different illumination wavelengths.*

tive minority lifetime across the wafer from μ-PCD is 1.7 μs whereas it is 0.24 μs in the PL image.

To understand this large deviation in absolute values we need to consider the influence of the illumination wavelength on the measured lifetime. In transient measurements a fundamental mode for the carrier density profile across the thickness of the wafer is established shortly (within a few times the transient time) after the excitation is switched off. The decay and the resulting lifetime deduced from it are then independent of the excitation wavelength. In contrast, lifetime data from QSS measurements can depend strongly on the excitation wavelength[5]. As noted previously, this dependence is particularly pronounced for poorly passivated wafers[6].

Fig.3 shows PC1D[7] simulations of the QSS effective minority carrier lifetime in a 200μm thick 1Ωcm p-type wafer for various illumination wavelengths λ_{exc} and as a function of the front surface recombination velocity S_f. The rear surface recombination velocity S_b was set to 1 cm/s and the illumination intensity to 0.01 W/cm^2 for all calculations. The bulk lifetime is 100μs. For low front surface recombination velocities all curves approach the bulk value with negligible dependence on the illumination wavelength. In contrast, for front surface recombination velocities $S_f > 10^4$ cm/s the measured effective lifetime varies dramatically with the illumination wavelength. For example at $S_f=10^6$ cm/s the *measured* lifetime varies by more than two orders of magnitude from τ_{eff} =0.028 μs at λ_{exc}=400nm excitation wavelength to τ_{eff} =4.05 μs at λ_{exc}=1100nm.

The PL image from Fig.2b and the QSS-PC measurement used for its calibration were both performed using λ_{exc}=808nm. Theoretical calculations for a 200μm thick wafer with $S_f=S_b=10^6$cm/s and a bulk lifetime of 100μs yield an effective lifetime of τ_{eff}=0.28 μs for λ_{exc}=808 nm, which is in good agreement with the experimental value (0.24 μs). The small deviation between theory and experiment points to a lower average bulk lifetime in the wafer than the 100μs used for the modeling. The deviations between the μ-PCD data and the calibrated PL image are thus caused by the wavelength dependence of QSS lifetime measurements on poorly passivated wafers.

The surface limited lifetime in transient measurements is given as[8,9]

$$\tau_{eff,(S=\infty)} = \frac{d^2}{\pi^2 D} \tag{3}$$

where D is the diffusion coefficient, which is the electron diffusion coefficient (for p-type) in low level injection and the ambipolar diffusion coefficient in high injection. In low level injection (D=D_n=26 cm^2/sec) Eq.3 gives 1.58 μs for a 200 μm thick wafer. The *average* experimental μ-PCD lifetime (1.7 μs) is higher than this value, which indicates that the μ-PCD measurement reports the

lifetime in high level injection, for which the surface limited lifetime is higher due to the reduced ambipolar diffusion coefficient. We will return to this point in the section on injection level dependence.

QSS experiments on poorly passivated wafers thus generally cannot be expected to agree with transient data due to their strong dependence on the illumination wavelength. Note that even for homogeneous excitation the diffusion limited lifetime varies by 21% relative $(12/\pi^2)$ between QSS and transient data[9]. The measured effective lifetime also depends on the wafer thickness, the surface recombination velocities, the injection level and the background doping. *Single values for the absolute effective minority carrier lifetime of poorly passivated silicon samples are therefore merely arbitrary numbers unless*
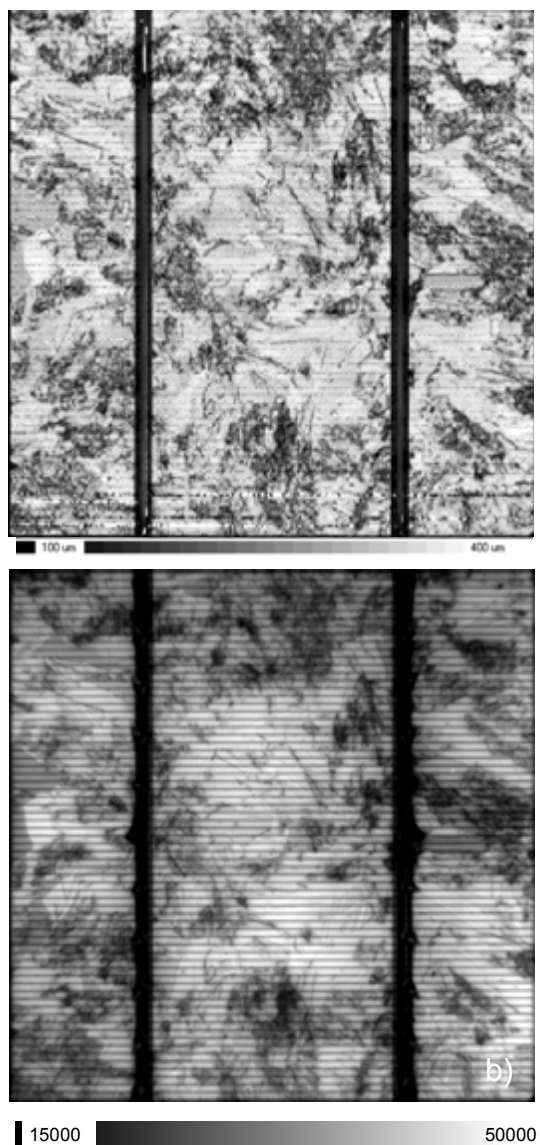
Fig.4 (a) *Diffusion length from LBIC and (b) count rate in a PL_{OC} image taken on a finished screen printed cell made from a wafer at x=0.51.*

90

they are combined with a quantitative analysis of the influence of the above noted parameters.

Spatial variations of the minority carrier lifetime

The regions of reduced effective lifetime in Fig.2 are caused by dislocation networks. Fig.4a and 4b show the diffusion length from a spectral LBIC measurement (in μm) and the intensity distribution within an open circuit PL image (PL$_{OC}$), respectively of a screen printed solar cell processed on a wafer from position x=0.51 (i.e. not directly adjacent but nearby the wafer shown in Fig.2).

Both measurements in Fig.4 reveal spatial variations in the diffusion length that are similar to the intensity variations observed in the PL image and in the μ-PCD map taken on the raw wafer (Fig.2). For a cell made from the same or directly neighboring wafer that correlation would be even more pronounced. The structural defects visible in the spatially resolved PL and μ-PCD data on the raw wafers thus remain as the dominant recombination active defects in the finished cells.[10]
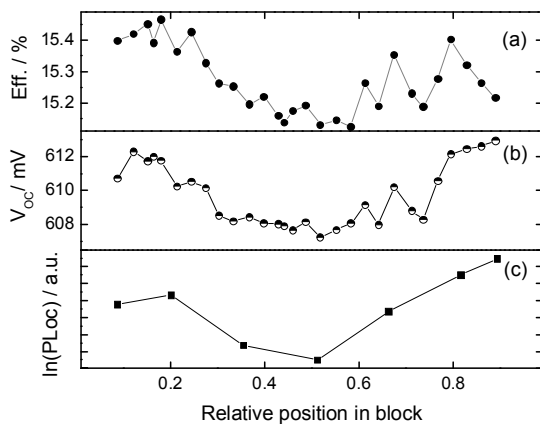
Fig.5 *(a) efficiency and (b) open circuit voltage of cells as a function of the relative position in the brick.(c) logarithm of the PL count rate measured under open circuit conditions.*

Wafers from the brick were processed into screen printed solar cells. Fig.5a and 5b show the efficiency and the open circuit voltage, respectively of those cells as a function of the position in the brick. Cell efficiencies are ~0.3% absolute lower in the central part of the brick compared to the bottom region. The logarithm of the average PL$_{OC}$ intensity is shown in Fig.5c. The data correlates well with Voc (R^2= 0.957) as expected[11].

In contrast the almost constant average μ-PCD lifetimes and average PL counts measured on as-cut wafers across the central region of the brick (Fig.1) do not allow a correlation with cell parameters. This is because in the wafers investigated in this study the efficiency limiting highly recombination active structural defects are localized and take up only a small area fraction of the wafer. In addition the difference in *effective* lifetime between these low bulk lifetime defect sites and the high-bulk lifetime regions surrounding them is small in the unpassivated as-cut wafers, resulting in an almost negligible influence on the *average* effective lifetime.

Dislocations in wafers can be made visible e.g. by various etching procedures, e.g. via Dash etching[12]. This is, however, a very cumbersome technique, destructive to the wafers and thus clearly not suitable as a production quality control method for a large number of wafers. The correlation between the patterns in the PL images on wafers and cells indicate that the relevant information about dislocation distributions can be gained from PL images. Our preliminary data from one silicon brick showed that measurement of dislocation densities on raw wafers from PL imaging works for wafers from the central part of the brick (0.15<x<0.8). On the very low lifetime top and bottom regions the bulk lifetime in the dislocation free regions is reduced by high defect concentrations, thereby reducing or completely masking the contrast in the effective lifetime between dislocation rich and dislocation free regions in PL images.

The results from this study thus suggest that particularly in the central part of a cast ingot the essential information that can be gained on as cut wafers is in the relative spatial variation rather than absolute lifetime values. The high spatial resolution of PL images and the short measurement times are essential advantages in this context that may allow PL imaging to be used as an efficient quality control tool. More statistical data on wafers from different positions of the ingot and made from various types of feedstock are required to gain more insight into how PL images on raw wafers correlate with cell efficiency.

Injection level dependence

Typical values for the front surface recombination velocity in screen printed mc-Si cells are on the order 10^3 cm/s. According to Fig.3 the illumination wavelength then only has a small influence on the measured minority carrier lifetime and experimental results from different experimental techniques performed on the same wafer generally become more comparable.

Fig.6 shows the average minority carrier lifetime from μ-PCD (squares) and the average count rate from uncalibrated PL images (circles) on diffused (open symbols) and non-diffused (full symbols) wafers (both after SiN and firing) as a function of brick position. The relative variation along the brick shows excellent correlation between the μ-PCD data and the PL count rate, the latter normalized with respect to the doping of the wafers (see e.g. the lines through the data for the non-diffused wafers in Fig.6).
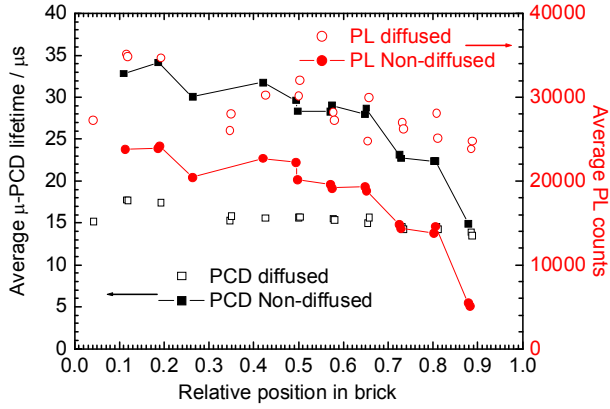
Fig.6 *Average lifetime from µ-PCD (squares) and average count rate (normalised to background doping) from PL imaging (circles) for SiN fired mc-Si wafers with (open symbols) and without (closed symbols) emitter diffusion as a function of the relative position in the brick.*

Across the entire brick the average µ-PCD lifetime is higher in the non-diffused wafers compared to the µ-PCD lifetime of the diffused wafers. Since the optical properties of the diffused and non-diffused wafers are very similar the variation in normalized PL count rates shown in Fig.6 is indicative of the corresponding effective lifetime variations. In contrast to the µ-PCD results the PL imaging data thus indicate a higher lifetime for the diffused wafers.

This inconsistency between PL intensity and µ-PCD lifetime is caused by the injection level dependence of the minority carrier lifetime. Fig.7 shows injection level dependent QSS-PC measurements performed with monoch-
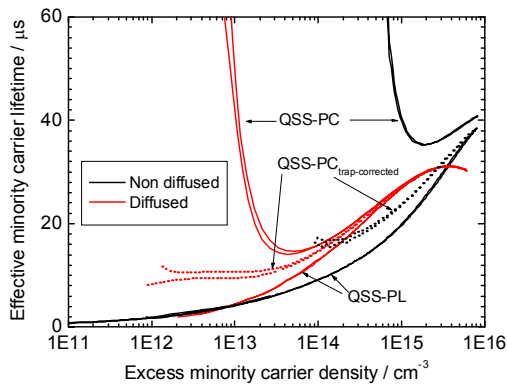
Fig.7 *Apparent lifetime as a function of apparent injection level(solid lines) from QSS-PC on non-diffused (black) and diffused (red) SiN fired mc sister wafers and the corresponding trapping-corrected data (dotted). QSS-PL lifetime measurements on the same wafers are unaffected by trapping.*

romatic laser pulses with up to 15 Suns equivalent illumination intensity on a wafer from position x=0.49 without emitter diffusion (black line) and on a wafer with emitter diffusion from position x=0.5 (red line).

The QSS-PC data of the non-diffused sample is heavily affected by minority carrier trapping[13] at excess carrier densities $<3*10^{15}$cm^{-3} and even the highest laser intensity is not sufficient to reach an injection level at which the QSS-PC measurement is unaffected by trapping artefacts. To correct the experimental QSS-PC data for the influence of trapping effects the QSS-PC data were modeled using an automated fitting algorithm, which first calculates the actual injection level dependent effective lifetime $\tau_{eff}(\Delta n)$ according to[9]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{S}{d} + J_0 \frac{[N_{D/A} + \Delta n]}{q n_i^2 d} \tag{3}$$

where S is the surface recombination velocity, d the wafer thickness, J_0 the dark saturation current density, q the elementary charge and n_i the intrinsic carrier density. For the non diffused wafers the last term in Eq.3 (junction recombination) was set to zero, i.e. the surface recombination term accounts for both surfaces in that case. A simplified Shockley Read Hall model was used to calculate the injection level dependent bulk lifetime

$$\tau_{bulk} = \tau_{n0} + \tau_{p0} \cdot \frac{\Delta n}{N_{D/A} + \Delta n} \tag{4}$$

Auger recombination can be neglected for the injection level and lifetime range we are interested in here. The modeled $\tau_{eff}(\Delta n)$ dependence was converted into apparent lifetime as a function of apparent injection level using the formalism described by Macdonald et al[13]. The trapping parameters and all parameters from Eqs.3 and 4 were then varied to get the best fit between the modeled apparent lifetime as a function of apparent injection level and the experimental data. Fig.8 shows the excellent fit between model and experiment for a diffused and SiN fired wafer.

The trap density N_t and the ratio of time constants for trapping and detrapping τ_t/τ_g, obtained from the fit were then used to extract the injection level dependence $\tau_{eff}(\Delta n)$ from the trapping affected experimental QSS-PC data. Similar to an analytic bias light correction approach[14] this analysis extends the range of usable QSS-PC lifetime data to significantly lower injection levels. Excellent agreement is observed between the trap corrected experimental data (circles in Fig.8) and the modelled $\tau_{eff}(\Delta n)$ according to Eq.3. Fig.8 also shows the individual contributions to the effective lifetime. The decreasing effective lifetime values in the diffused wafer at injection levels $>4*10^{15}$cm^{-3} are caused by the junction recombination. The value $J_0 = 1.7*10^{-13}$ Acm^{-2} obtained from fitting the data is typical for screen printed cells.
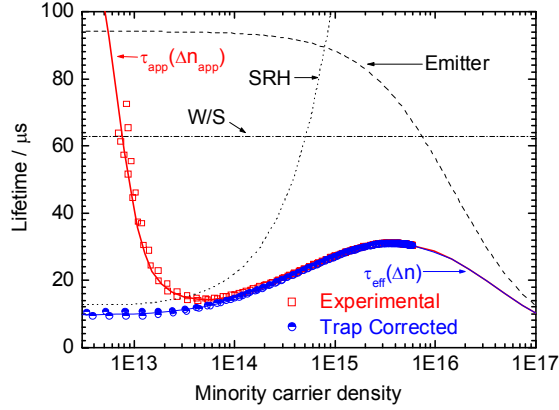
Fig.8 *Measured (open squares) QSS-PC (apparent lifetime as a function of apparent injection level) on a diffused SiN fired wafer and analytic fit according to Eq.3 (solid line). Broken lines show the individual contributions to the effective lifetime. Circles show the trap corrected QSS-PC data.*

QSS-PL lifetime measurements

Fig.7 shows the trapping-corrected QSS-PC data for the diffused and non-diffused wafers as dotted lines. QSS-PL lifetime measurements on the same samples are shown in Fig.7 for comparison. Since QSS-PL is not affected by minority carrier trapping[15] and extremely sensitive[1] it allows the variation of the lifetime at low injection levels to be measured. Note that the QSS-PL data are shown here down to $\Delta n=10^{11} cm^{-3}$, but were conveniently measured to much lower injection levels $\sim\Delta n=10^{9}\ cm^{-3}$. The trap corrected QSS-PC data on the diffused wafer at the highest injection level were used for the calibration of the QSS-PL data. Good agreement is observed in that injection level range between the injection level dependent trap corrected QSS-PC data and the QSS-PL data.

Towards low injection levels increasing deviations are observed between the QSS-PL and the trapping-corrected QSS-PC data. We currently interpret these deviations to be a convolution of various effects: 1) The trap correction method only provides reliable QSS-PC data over a limited injection level range and becomes increasingly inaccurate towards lower injection levels; 2) the QSS-PL data are affected by reabsorption effects, which are generally small but most pronounced in exactly this lifetime range[16] and which have not been accounted for in the analysis presented here; 3) the decreasing minority carrier lifetime towards lower injection levels is not accounted for in the theoretical model above. This decrease is likely due to an increasing surface recombination velocity at low injection levels[17].

The injection level dependent QSS-PL data and the trap corrected injection level dependent QSS-PC data in Fig.7 explain the apparent discrepancy between the μ-PCD and

PL data from Fig.6: PL imaging was performed in this study with homogeneous one Sun equivalent illumination intensity over the entire wafer area resulting in an excess minority carrier density on the order of $\sim3*10^{14}\ cm^{-3}$. As seen in Fig.7 the effective minority carrier lifetime is higher for the diffused wafer in that injection level range, an effect that could be caused e.g. by phosphorous gettering. The μ-PCD measurement is performed with local illumination by a laser beam and determines the lifetime at a higher but undefined injection level, where the effective lifetime of the diffused wafer is strongly reduced by the junction recombination, and is therefore lower than the lifetime of the non-diffused wafer.

Calibrated Images

Fig.9 shows a calibrated PL image and the minority carrier lifetime from μ-PCD measured on a non-diffused wafer from the middle (x=0.51) of the ingot after SiN deposition and firing. The deviations in the absolute average lifetime (τ_{eff}=28.3 μs in μ-PCD versus τ_{eff}=10.5μs in the PL image) have been analyzed in the last section. Qualitatively the same features of high and low lifetime regions are observed. Note that the PL image was measured with a total exposure time of only 1s (compared to ~30 minutes required for μ-PCD) and with higher spatial resolution of 160 μm per pixel (compared to 500μm in the μ-PCD map).

SUMMARY AND CONCLUSIONS

The above results confirm QSS-PL as a quantitative tool for minority carrier lifetime measurements on silicon wafers. Ahrenkiel et al. recently investigated the relationship between the luminescence signal and the minority carrier lifetime over a wide range of silicon wafer resistivities[18]. The authors plotted "the luminescence intensity" measured on a number of samples as a function of "the minority carrier lifetime" and concluded from this data that PL is "*not a reliable measurement tool for minority carrier lifetime*"[18].

We believe that the origin of this discrepancy is in the comparison by Ahrenkiel et al of single luminescence intensities measured on a variety of wafers with single lifetime values that are measured with a different experimental technique, which is a too simplistic approach as it ignores some fundamental aspects of minority carrier lifetime and QSS-PL measurements:

1) The effective minority carrier lifetime depends strongly on the injection level.
2) *Measured* QSS effective lifetime generally depends on the illumination wavelength, especially in poorly passivated wafers.
3) The effective lifetime can depend strongly on the illumination spot size and it varies laterally across the wafer.

Even for a single wafer it is therefore generally not a valid approach to compare a PL signal with a single lifetime value that is measured with a different technique, i.e. under different conditions and possibly in a different position on the wafer. In addition, as discussed above:

4) The PL signal corresponding to a specific effective lifetime value depends strongly on the sample geometry (thickness, surface morphology and anti reflection coating of both surfaces).

Without accounting for such sample specific effects the quantitative comparison of the PL emission from different samples by Ahrenkiel et al would be valid only for samples with identical sample geometry and optical properties. Finally:

5) The measured lifetime may also depend on the "history" of the sample. Depending on the measurement conditions, the measurement itself can have an impact on the result, e.g. via breaking of FeB pairs upon high-intensity illumination during the measurement[19].

No information is given by Ahrenkiel et al. on most experimental conditions relevant to points 1-5 above. We therefore strongly believe that the scatter reported by these authors in the PL versus lifetime data is caused by a combination of these effects, particularly points 1) and 4).

The data presented above demonstrate that if performed under well defined experimental conditions and in combination with suitable calibration QSS-PL is an excellent quantitative tool to measure both the spatial variation and the injection level dependence of the minority carrier lifetime. This is demonstrated here e.g. by the low scatter in QSS-PL data measured on raw wafers from different positions of the ingot (Fig.1) or by the strong correlation between luminescence images and μ-PCD lifetime maps (Fig.9).

The review of some fundamental aspects of effective minority carrier lifetime measurements shows that for a quantitative analysis of absolute minority carrier lifetime values it is important to distinguish between well passivated ($S \leq 10^3$cm/s) and poorly passivated wafers ($S \gg 10^3$cm/s).

For well passivated silicon wafers ($S \leq 10^3$cm/s) a quantitative comparison of the absolute minority carrier lifetime measured with different experimental techniques and/or excitation wavelengths is generally a valid approach. It is essential, however to analyze the minority carrier lifetime at the same injection level, since otherwise the analysis leads to misleading results. In order to get information that is relevant to the operation of a solar cell minority carrier lifetime measurement should be performed with one Sun equivalent illumination intensity.

For transient measurements the transient decay would need to be analyzed at the corresponding injection level. Spatially resolved μ-PCD, while conveniently providing absolute numbers is inherently incapable of reliably measuring the minority carrier lifetime at injection levels equivalent to one-Sun illumination due to the limited sensitivity at low injection levels and due to the influence of minority carrier trapping and excess carriers in space charge regions[20]. Analyzing the photoconductance decay at a significantly higher and undefined injection level is disadvantageous not only because this procedure provides the lifetime under conditions that are irrelevant for
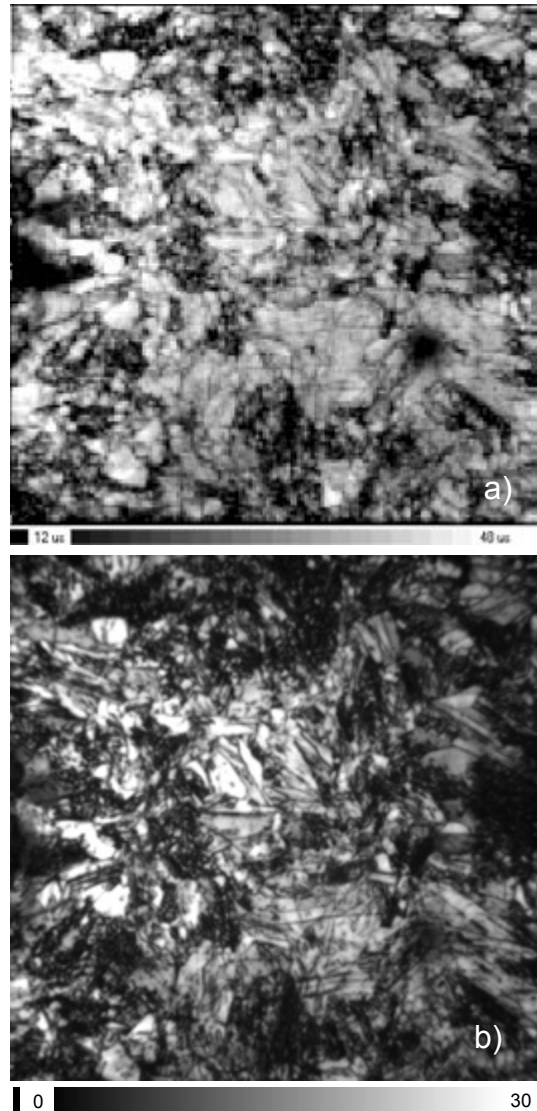
Fig.9 *Minority carrier lifetime in μs of a non-diffused and SiN fired wafer from x=0.52. (a) from μ-PCD (b) from PL image calibrated against QSS-PC.*

the operation of a solar cell under one Sun illumination but also because at injection levels $>10^{15}$cm^{-3} the conductance decay is affected by the injection dependence of the effective lifetime and of the mobilities. The latter is taken into account quantitatively in QSS-PC measurements in

typical experimental systems[21] but cannot be accounted for in transient measurements with unknown injection level.

In contrast, PL imaging is well suited to provide the spatial variation of the minority carrier lifetime at one Sun equivalent illumination intensity, since it is fast, non-contact and not affected by the above artefacts. Calibration of the measured PL intensity into absolute lifetime can be achieved by correlation with QSS-PC data and if required in combination with an analytic correction of the latter for trapping artifacts. The combination of PL imaging and QSS-PC in the same experimental set-up as in the BT Imaging LIS-R1 prototype system used in this study thus appears to be a well suited approach for characterization of silicon wafers for photovoltaic applications.

Absolute lifetime measurements on poorly passivated wafers at an early stage of processing must be interpreted in combination with a detailed analysis which accounts for the influence of various experimental and sample specific parameters, particularly for the strong impact of the excitation wavelength on QSS experiments. Within certain limits, such a quantitative analysis can be used e.g. to extract the bulk lifetime from the measured effective lifetime[6]. Such an analysis is however very sensitive to the exact absolute effective lifetime values. The above example of experimental μ-PCD values that are higher than the low injection level surface limited effective lifetime suggest that μ-PCD data are hardly suitable for this purpose.

Without a detailed analysis any absolute values for the effective minority carrier lifetime are merely suitable to be used as a figure of merit, e.g. via a relative comparison of lifetime variations within a sample or between different samples. In this case the uncalibrated normalized QSS-PL intensity itself can be used as a figure of merit, especially in industrial production, where thousands of samples with effectively identical optical properties are processed, eliminating the strong impact of the sample geometry on the results.

The results from this study also suggest PL imaging to be a suitable method for the determination of dislocation distributions in as-cut wafers from the central region of cast mc-Si ingots. In earlier work we showed that PL images of as-cut wafers also unambiguously show low bulk lifetime regions near the edge or corners of wafers that were cut from the edge or corner of a cast ingot[22]. The ability to identify such spatial features on as-cut wafers with very short measurement times makes PL imaging a promising candidate for quality control in solar cell and wafer production.

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Advances in Si Solar Cell Metallization

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FERRO

(Paper not available)

Minority Carrier Dynamics in Polycrystalline Silicon Solar Cells Investigated by Photo-assisted Kelvin Probe Force Microscopy

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1. Introduction

In polycrystalline silicon solar cells, a grain boundary is considered to be the major cause of the low conversion efficiency[1]. To investigate influences of the grain boundary, we have performed local measurements of surface photovoltage (SPV) by means of photo-assisted Kelvin probe force microscopy[2, 3] (P-KFM). Here, Kelvin probe force microscopy[4] (KFM) which is based on atomic force microscopy (AFM) enables us to measure the surface potential with high spatial resolution, and by combining it with the optical equipments the SPV measurements is realized. In this study, we introduce novel methods through the photovoltage measurements by P-KFM for a purpose of investigating minority carrier dynamics, such as lifetime and diffusion length, which are very important to dominate solar cell performance. The former was determined from temporally-averaged photovoltages at various modulation frequencies of the incident light, while the latter was characterized from dependence of photovoltage on wavelength of the incident light. We also discuss the distribution of the lifetime and diffusion length around the grain boundary in the polycrystalline silicon solar cell.

2. Experimental

Figure 1 shows our P-KFM system consisting of a commercial AFM system (SPI 4000/SPA 300HV, SII NanoTechnology Inc., Japan) and some external electronics to obtain an accurate surface potential value. This KFM operates in a high vacuum (typically, 10^{-5} Pa) at room temperature and in an intermittent contact mode with a piezo-resistive cantilever (PRC400, SII NanoTechnology Inc., Japan). A tunable Ti:Al$_2$O$_3$ laser system was used as a light source, and the laser light was transmitted through an optical fiber and focused on a sample surface just beneath a Pt-coated KFM tip. For the lifetime measurements, a monochromatic light was modulated by an acousto-optic light modulator (AOM) with a duty ratio of 50%, while a photon density of a continuous and monochromatic light
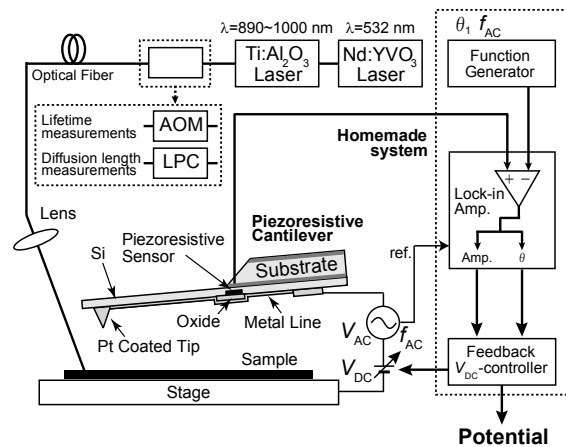

Fig. 1 Experimental setup of our P-KFM system.

in a range between 890 and 990 nm was stabilized by the laser power controller (LPC) at every wavelength for the diffusion length measurements. To evaluate the photovoltage, an intrinsic surface potential was firstly measured by KFM under dark condition, secondly the surface potential under the light illumination was measured, and lastly a potential change by the light illumination was calculated numerically.

Figure 2 shows an optical micrograph of the polycrystalline silicon solar cell sample fabricated on a p-type polycrystalline silicon substrate with a phosphorus doped surface *n*-layer of approximately 500 nm in thickness. In this figure, surface orientation as well as a type of boundary characterized by the electron back scattering diffraction (EBSD) method were indicated. In order to investigate an original characteristic of polycrystalline silicon material, we did not carry out any other surface processing.
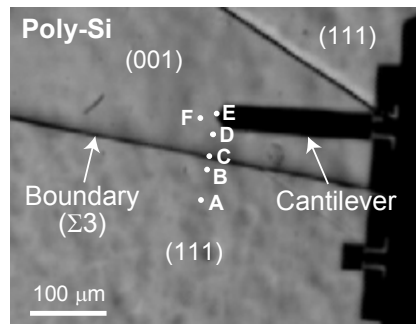
Fig. 2 An optical micrograph of the polycrystalline silicon solar cell sample.

3. Results and Discussion

3.1 Minority Carrier Lifetime

For the minority carrier lifetime measurements, the intensity of the incident light was modulated and the temporally-averaged photovoltage V_{Ave} over the modulation period was measured by P-KFM. From the dependence of V_{Ave} on the modulation frequency, the time constant of the photovoltage decay at off period of the light illumination, which corresponds to the minority carrier lifetime due to the bulk recombination, was evaluated[5].

Figure 3(a) shows the temporally-averaged photovoltage V_{Ave} normalized by V_{Max} (the photovoltage under continuous illumination) as a function of the modulation frequency f (=1/T: T is the modulation period) measured at point E indicated in Fig. 2. As shown in Fig. 3(a), V_{Ave} was just a half of V_{Max} at the low modulation frequency, where the modulation period was sufficiently long

Fig. 3 (a) The temporally-averaged photovoltage V_{Ave} normalized by V_{Max} as a function of the modulation frequency f measured at point E indicated in Fig. 2. (b) lifetime at points A-E indicated in Fig. 2.

compared to the carrier lifetime and the photovoltage seemed to simply follow the intensity change of the incident light. In the middle frequency region where the modulation period

became comparable to the lifetime, on the other hand, V_{Ave} gradually increased as an increase of the modulation frequency. From this dependence the carrier lifetime was numerically evaluated. Note here that V_{Ave} was saturated again in the high frequency region but that the saturation value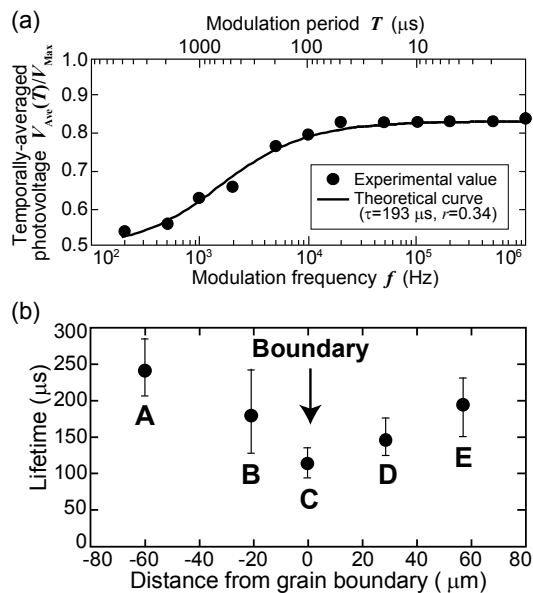 was below 1.0. We attribute this result to facts that a part of photocarriers, especially existing near the surface, recombined very quickly by the fast surface recombination process and that the photovoltage drop due to it was still apparent even in this frequency region. In this study, the contribution of this photovoltage drop was represented by a parameter r.

The theoretical curve of V_{Ave} calculated with r=0.34 and τ=193 μs was also plotted in Fig. 3(a), and this curve fits very well with the empirical values. Thus the minority carrier lifetime τ at point E was determined to be 193 μs. We have performed similar measurements on the other points indicated in Fig. 2, and the estimated carrier lifetimes were summarized in Fig. 3(b). As shown in Fig. 3(b), the lifetime gradually shortened as the measuring point moved close to the grain boundary, and the lifetime at point C in the most vicinity of the grain boundary was almost a half of the lifetime values at points A and E. This fact suggests that the grain boundary acts as a carrier recombination site and/or a leakage pass and degrades the solar cell performance.

3.2 Minority Carrier Diffusion Length

In a *p-n* junction like a solar cell structure, a relationship among the photovoltage V, the minority carrier diffusion length L and the optical absorption coefficient α for an incident light is given by the equation of $1/\{\exp(qV/kT)-1\}=C(L+1/\alpha)$ where C is a constant, in the condition of a constant photon density[6]. Experimentally, owing to a fact that α is varied by changing the wavelength of the incident light, L can be evaluated from the dependence of the photovoltage on the penetration depth ($1/\alpha$) by taking extrapolation where the above equation becomes zero.

Figure 4(a) shows the dependence of the photovoltage V on the penetration depth $1/\alpha$ at points A, B and F, indicated in Fig. 2, and from Fig. 4(a) the diffusion lengths at those points were evaluated to be 50, 20 and 80 μm, respectively. This reslut clearly indicates that the diffusion length at point B in the vicinity of the grain boundary is obviously shortened compared with those at points
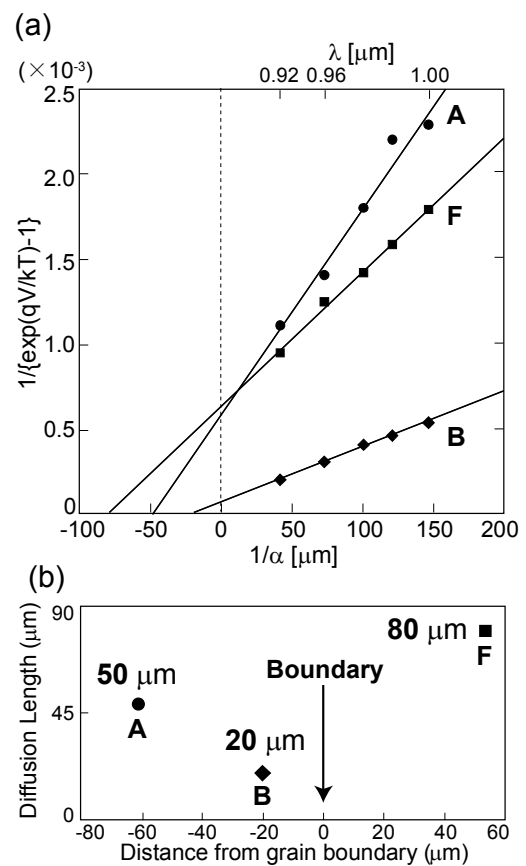

Fig. 4 (a) Photovoltage V as a function of penetration depth $1/\alpha$ or incident laser wavelength λ at points A, B and F indicated in Fig. 2. (b) diffusion length at points A, B and F indicated in Fig. 2.

A and F which are 70 and 50 μm, respectively, away from the grain boundary.

Here, the diffusion length values are evaluated based on the one-dimensional model without taking the lateral diffusion toward the grain boundary into account. Therefore, the marked shortening of the diffusion length observed at point B was attributable to two mechanisms: (i) true shortening due to the degradation of the crystal quality and (ii) artifact due to the lateral diffusion of the photocarrier toward the grain boundary. From the view point of the crystallography, it is hardly consider that the crystal degradation occurs very locally at Point B. Therefore, the latter one is more possible, and this mechanism is very consistent with our previous results of the photovoltage measurements[3] as well as the lifetime measurements discussed above, which indicated that the grain boundary acts as a carrier recombination site and/or a leakage pass[3, 5].

Conclusions

We have proposed the methods to evaluate both lifetime and diffusion length through the photovoltage measurements by P-KFM, and have found the degradation of lifetime as well as diffusion length in the vicinity of the grain boundary in the polycrystalline silicon solar cell material. These results indicate that the grain boundary degrades the solar cell performance by acting as a carrier recombination site and/or a leakage pass.

Acknowledgements

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RECYCLING OF SOLAR CELL SILICON SCRAP BY FILTRATION

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Abstract

In this study, recycling of top-cut silicon scrap is investigated. Top-cuts in the multicrystalline silicon ingots have a high content of solid inclusions which are SiC and Si_3N_4 particles. For this reason they are lost as scrap. However, on removing the solid inclusions by a simple filtration process with ceramic foam filters we can recycle silicon as PV feedstock. 10, 20 and 30 ppi (pores per linear inch) SiC filters are used in our experiments. Filtration efficiency is determined by counting inclusions before and after filtration. Furthermore, solid inclusions are collected after the silicon matrix is dissolved in an acid mixture (HF + HNO_3), and counting with an automated light microscope is carried out afterwards. With a 30 ppi SiC filter, removal of inclusions is 99%.

Introduction

Photo voltaic cells have been an attractive technology for power generation due to its clean and non-polluting nature. During the past decade there has been a strong growth in demand for solar cell modules. The current dominant semiconductor material used in photovoltaics are silicon wafers, particularly of multicrystalline silicon. Multicrystalline silicon is cast in a silicon nitride (Si_3N_4)-coated quartz crucible and is subsequently directionally solidified. A Si_3N_4 coating which prevents the adhesion of the silicon ingot to the quartz crucible walls, is the source of the silicon nitride inclusions in the silicon ingot. The lining refractory and graphite heating elements may be a source for silicon carbide particles [1].

After directional solidification the parts containing solid particles are cut off from the top of the ingot. Usually slices of 10-20 mm depth are removed. These regions have a high concentration of impurities such as iron, aluminium, SiC, Si_3N_4, etc. While the bottom and sides are recycled and used again in the solidification process, the top-cut is sold as low value scrap [2]. If SiC and Si_3N_4 particles can be removed from the top-cut scraps to a low content, the silicon can become feedstock in PV cell production [3].

Inclusion removal from silicon can be accomplished by filtration with ceramic foam filters, which have already proved to be efficient in removing harmful particles from liquid aluminum and steel. In this paper we present results on the removal of solid inclusions from silicon scrap by filtration.

Methods and materials

Top-cut silicon scrap was provided by Scan Wafer ASA, a Norwegian company that produces multicrystalline silicon wafers for PV industry. The material came in square pieces with dimensions of 150 mm × 150 mm with thickness that ranges from 10 to 20 mm. The silicon scrap pieces were crushed into smaller pieces before they were melted down and filtered. About 270 g silicon scrap was filtered in every experiment.

The filters for the filtration experiments were of SiC with 10, 20 and 30 ppi. They were provided by Eger-Sørensen, a Norwegian company and consist of 85% SiC while the rest is Al_2O_3 and SiO_2 binder. Pictures of SiC filters are shown in Figure 1.

10 mm
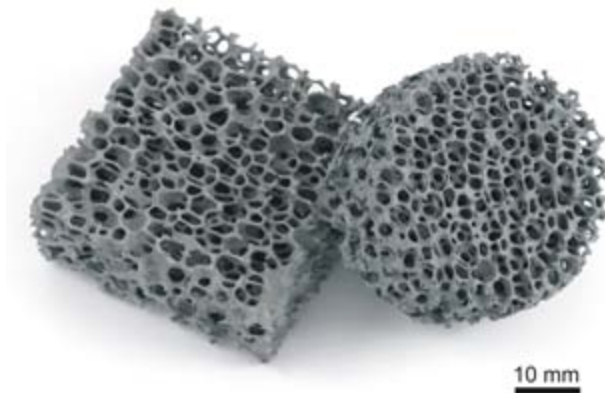
Figure 1: Photos of SiC filters.

For the filtration experiments a high vacuum furnace was employed. The furnace houses the heating coil and graphite crucible. The crucible holds the silicon pieces. The molten silicon passes through the filter in the bottom of the crucible and is collected in a copper bowl. The low temperature of the copper bowl causes silicon to solidify immediately. The design of the crucible allows removal of the filter afterwards so that the crucible can be used again in new experiments. The sketch of the experimental set-up and other details of the filtration experiments is reported elsewhere [3]. The experiments are carried out in argon atmosphere and the crucible is heated gradually up to a temperature of 1450°C.

Silicon samples before and after filtration were submitted to chemical and microscopic analysis. Acid dissolution with HF and HNO_3 in a ratio of 1:3 was carried out to extract inclusions from silicon. This acid mixture dissolves silicon while the solid particles, SiC and Si_3N_4 inclusions, are left behind and are collected on a paper filter. Finally the particles were analyzed with a photo automated microscope, and data on the total number of the particles and their size distribution were obtained.

Experimental results

Inclusions, collected after the dissolution of silicon scrap were analyzed by SEM and light microscopes. Figure 2 shows a picture taken by SEM of an inclusion cluster. X-ray analysis confirmed the presence of SiC and Si_3N_4. Figure 3 shows a picture before filtration taken with a photo microscope of large clusters of inclusions in silicon scrap. As it is seen from this figure, the Si_3N_4 particles form large networks. They have a golden to brownish color which is reported to be due to the presence of impurities such as Ti [3]. In most of the cases SiC particles are found together with Si_3N_4. According to the literature, the SiC particles nucleate on Si_3N_4 [4]. SiC particles have a dark grey to black color and are almost round in shape.

In our experiments we dissolved top-cut silicon scrap before filtration, and all the inclusions collected after dissolution were counted by automated photo microscope Bead Check 830. Inclusion size distribution for inclusions in silicon before filtration given as %number of particles versus mean diameter is shown in Figure 4. From this distribution we can see that the maximum size of the particles lies in the range size of 5 – 10 μm.
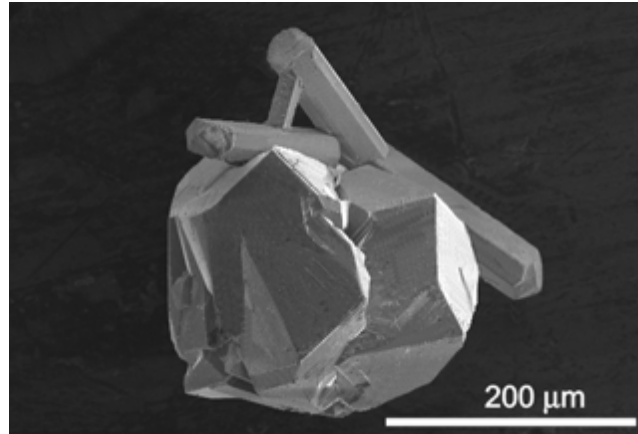
Figure 2: Inclusion cluster in silicon scrap before filtration. Round SiC particles and rod-shaped Si_3N_4 particles are shown.
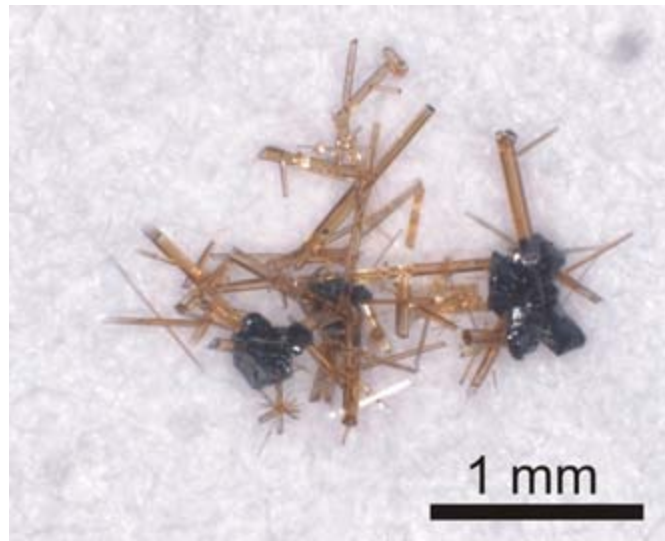
Figure 3: Inclusions in silicon scrap before filtration collected on a paper filter. Si_3N_4 particles have a golden to brownish color and with needle-like shape. SiC are dark grey to black and round in shape.

Several samples from filtered silicon with 10, 20 and 30 ppi were dissolved in the acid mixture and inclusions extracted were carefully collected and counted. The data obtained from the analysis is summarized in Table I. The number of particles is for dissolution of 100 g of silicon scrap in each filtration experiment with various SiC filters and also from silicon scrap before filtration. Standard deviation data are placed in brackets.

Table I: Results from dissolution of silicon scrap before and after filtration.

	Si before fil.	10 ppi filter	20 ppi filter	30 ppi filter
Nr. of particles (STDV)	11030	2464 (146)	1159 (974)	32 (31)
Filtration efficiency [%]	-	77.7	89.5	99.7

Filtration efficiency, η, is calculated from equation (1).

$$\eta = \frac{Nr._{\cdot before\ fil.} - Nr._{\cdot after\ fil.}}{Nr._{\cdot before\ fil.}} \times 100\% \tag{1}$$
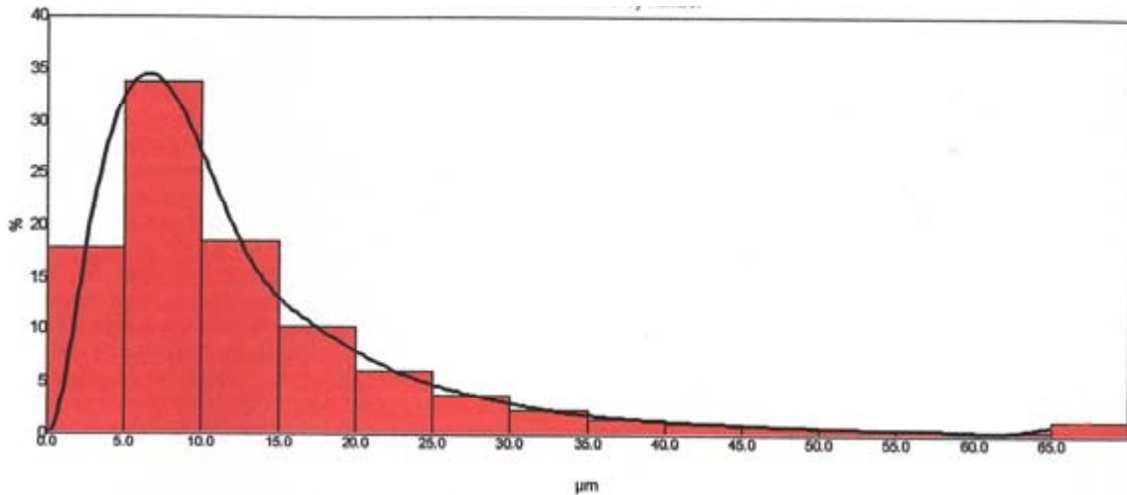
Figure 4: Inclusion size distribution by number % before filtration from dissolution experiments.

As one can expect, filters with smaller pores have higher removal efficiencies. 30 ppi SiC filters remove more than 99% of inclusions from silicon. The graph in Figure 5 presents the number of particles given in Table I.
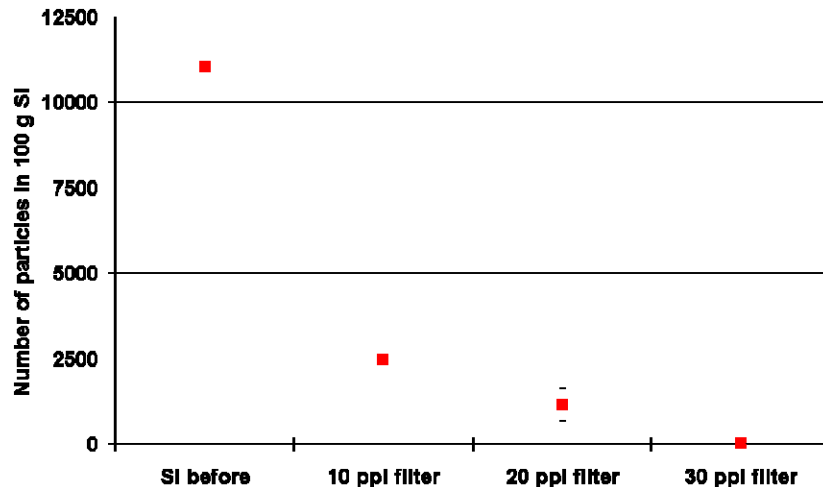
Figure 5: Total number of particles in 100 g silicon before and after filtration given in Table I.

Conclusions

Filtration experiments to remove SiC and Si_3N_4 inclusions from solar cell silicon scrap have been performed. SiC ceramic foam filters with 10, 20 and 30 ppi were used. Acid dissolution of silicon made it possible to extract inclusions and to analyze them by light microscopy. The results show that SiC and Si_3N_4 particles are removed from the silicon scrap material. Removal efficiency increases with decreasing pore size of the filter and a value of above 99% is reached with 30 ppi filters.

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Evaluation of multi-crystalline silicon substrates
with p-n diode array

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INTRODUCTION

Multi-crystalline silicon (mc-Si) substrate is widely used for solar cells, because the production costs are lower than those for single-crystalline silicon (sc-Si) [1]. However using mc-Si, the energy-conversion efficiency of solar cells has not been as high as that of sc-Si [2-6]. In order to verity the efficiency, we evaluated the uniformity of crystal quality in mc-Si substrates in conjunction with electrical properties. As solar cells essentially consist of p-n junctions, we fabricated a small p-n diode array on mc-Si substrates. Then the diode array was evaluated by various methods.

EXPERIMENT

In the experiment, a p-n diode array was fabricated on 50 × 50 mm mc-Si substrate grown by the casting method. Figure 1 shows the diode structure fabricated in this study. Phosphorus was doped by

Fig1. Structure of p-n diode, (a) layout, and (b) cross-section (A-B)

diffusion through a 1 × 1 mm SiO_2 mask to form the p-n junction. The Al electrode was then deposited and patterned into 1 × 1 mm square covering a quarter of the P-doped area. Therefore, three quarters of the diode surface was exposed for the evaluation of the crystal quality by non-destructive techniques [7].

The electrical properties were evaluated by I-V and DLTS measurements. Crystal qualities were also evaluated in each diode by PL, EBIC, and TEM in conjunction with the electrical characteristics.

RESULTS AND DISCUSSION

Typical three I-V characteristics are shown in Fig. 2. In this study we would focus on the evaluation of type (b) diode, because the diode showed some deterioration in the electrical characteristic comparing to the type (a) diodes although no obvious grain boundary was observed by the optical microscope unlike the case of type (c) diode. In the type (b) diodes dark lines were observed in PL mapping images quite often as shown in Fig. 3.
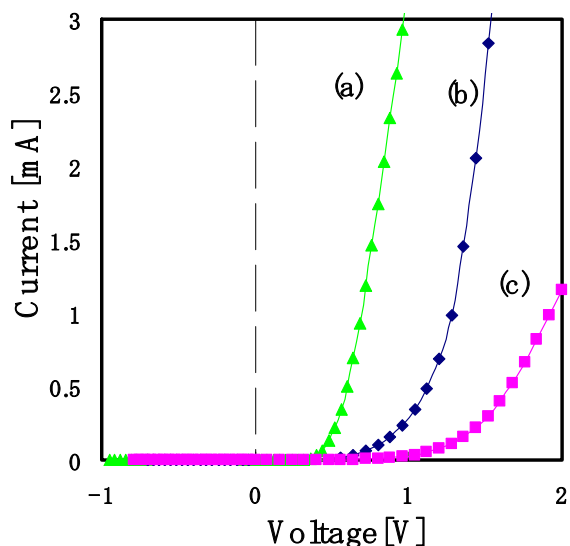
Fig.2 I-V characteristic

EBIC image was also observed in the same diode, and found the same contrast as some of PL dark lines. Therefore, we would conclude these dark lines are recombination centers for the minority carriers. A little difference in both images, *i.e.*, some missing PL dark lines in EBIC images, may be due to the depth confinement of the carrier generation depending on the electron acceleration voltage in EBIC measurement.
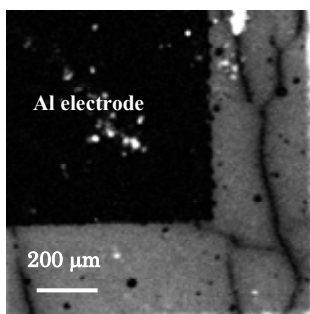
Fig. 3 PL mapping image
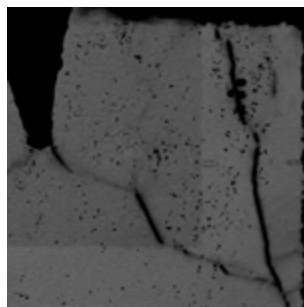
Fig. 4 EBIC image

Next, we performed TEM observations of the defects observed both in PL mapping and EBIC images. Figure 5 (a) is a low magnification TEM image of the defect. Obviously a straight line defect with black and white fringes is observed. The TED patterns taken from both side of the defect (Fig. 5 (b) and (c)) shows small difference meaning slight misalignment of the crystalline orientation. Therefore, we confirm this defect is small angle grain boundary (or sub-grain boundary). The magnified image of the defect (Fig. 5 (d)) revealed broken fringes, this may correspond to a dislocation.
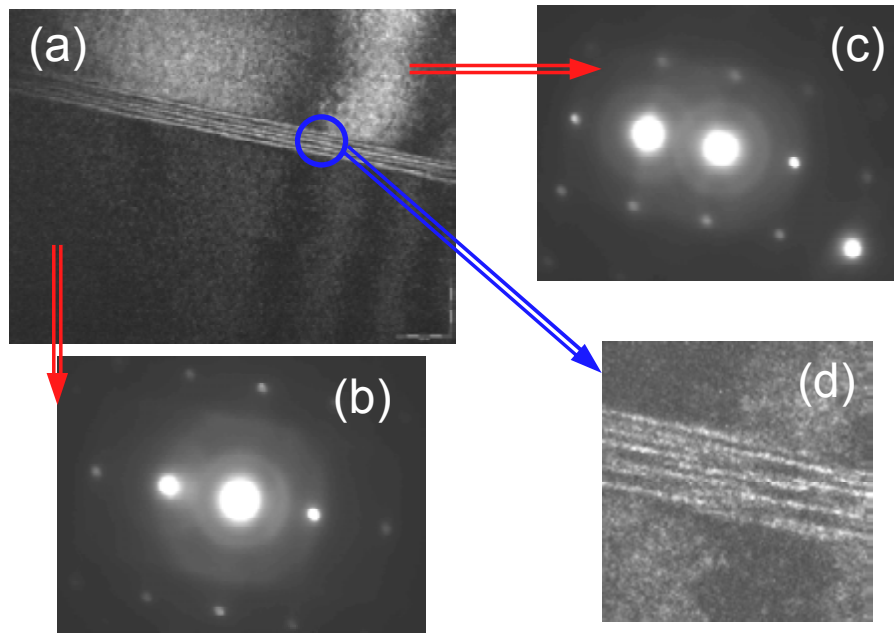
Fig. 5 TEM images of the defect, (a) low magnification image, (b), (c) TED pattern, and (d) high magnification image.

Figure 6 shows DLTS spectra taken from the diode (labeled (b)) and type (a) diode, respectively. The peak appears at approximately 200K in the diode with the defect, which is slightly shifted from that in the diode without defect (type (a)). The peak width also seems to be slightly narrower. The peak at 250K observed in

Fig. 6 DLTS spectra taken from the diode (labeled (b)) and one of the type (a) diode.

type (a) diode is similar to those observed from Fe in Si in the literatures [8]. The existence of the defect might modify the deep level and therefore the peak position and the shape in the DLTS measurement.

CONCLUSION

We fabricated a p-n diode array on mc-Si substrate, and evaluated both electrical and crystalline characteristics. The deteriorated diode without obvious grain boundary showed defect both in PL mapping and EBIC images. The TEM observation revealed the defect was small angle grain boundary. The DLTS spectrum observation with defect showed slightly modified peak from that without defect probably due to the deep level caused by the complex of defect and Fe contaminations.

ACKNOWLEDGMENT

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Passivation of boron-doped emitters in back-junction buried emitter solar cells by a phosphorus-doped surface layer

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ABSTRACT: We recently introduced the buried emitter solar cell concept that features a phosphorus-doped *n*-type surface layer on a boron-doped *p*-type emitter. The *n*-type surface layer can be employed as an effective insulation between a large area emitter and the metallisation of the base. Another purpose of the technique of covering a *p*-type emitter beneath an *n*-type surface layer is to provide a device structure where a boron-doped emitter can be effectively passivated by standard techniques such as thermal oxidation. Here we report on the status of our experimental buried emitter solar cell development. We furthermore present 1-dimensional device simulations by PC1D that emphasize the high-efficiency potential of the buried emitter solar cell.

INTRODUCTION

Back-junction solar cells are one of the most promising high-efficiency solar cell concepts for industrially relevant high-quality monocrystalline silicon wafer material such as *n*-type Cz silicon. This solar cell concept benefits from the absence of optical shading by front contacts as back junction solar cells accommodate the contacts for both polarities on the rear side of the solar cell. While efficient performance of this device structure strongly relies on a very high quality of front surface passivation, SunPower Corporation has already proven very high solar cell efficiencies of 22% and more in production [1] and also other leading solar cell manufacturers explore the benefits of using back-junction solar cell device structures [2]. Generally, the current collection efficiency of back-junction solar cells increases with increasing area fraction of the minority charge carrier collecting *p-n* junction between emitter and absorber. On the other hand, this asymmetry is disadvantageous for the metal contacts as the metallisations of both polarities have to carry the same current. The minimization of electrical series resistance and the cost-driven preference for thin layers of metal is a strong driving force towards metallisation designs that allocate similar area fractions for the metallisation of both polarities.

Consequently, dielectric insulation layers may be used to meet both requirements: asymmetric base and emitter area fractions in the semiconductor and at the same time symmetric area fractions for the metallisation of base and emitter. Figure 1 shows a cell with dielectric insulation [2]: A reliable insulation layer allows using an overlap between e.g. the metallization of the base with areas taken in by the emitter as shown in Figure 1.

In microelectronic applications thermal oxides have proven to fulfil such insulation purpose very efficiently when grown on polished wafers. However, as the silicon wafer material for commercial photovoltaic application has a rather rough surface and is not polished as in microelectronics, it is a challenging task to fabricate a reliable insulation layer by a thermal
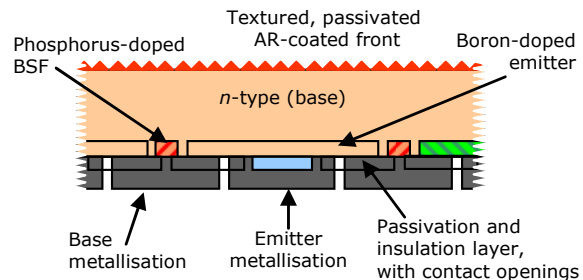
Figure 1: Cross sectional view of a back junction solar cell with a large area fraction covered by the emitter, and similar area fractions allocated for base and emitter metallization.

oxide [3]. We therefore recently introduced the concept of the buried emitter solar cell [4,5] that does not rely on dielectric insulation. Figure 2 shows a schematic cross section of the buried emitter solar cell, which uses a *p-n* junction to shield the metallization of the base from the large area emitter. This solar cell concept features large areas of overlap between heavy *p*-type and heavy *n*-type doped regions which is known to potentially give rise to junction shunting via trap assisted tunnelling [6]. This effect could be highly detrimental for the fill factor of the solar cell and would lead to very low solar cell efficiencies.

Textured and passivated front   Boron-doped emitter

n-type (base)

Phosphorus-doped "BSF"   Base metallisation   Emitter metallisation   Passivation with contact openings
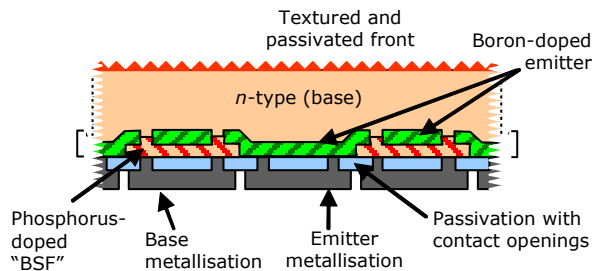
Figure 2: Cross sectional view of a "buried emitter" back junction solar cell. The buried emitter solar cell exhibits a large area emitter, and the possibility of using similar area fractions for base and emitter metallization without the need for any dielectric insulation. Note that the boron-doped emitter has only point-like openings. Thus, it is contiguous and covers virtually the full area.

It is therefore necessary that boron and phosphorus diffusion are well-controlled and optimised in order to avoid such parasitic effects. However, once successfully implemented, the solar cell does not suffer from junction shunting and exhibits a reverse breakdown at relatively low voltages and the associated heat dissipation is distributed across the whole area of the cell. Consequently, localised hot spots can be avoided and solar modules made from buried emitter solar cells do not require installing separate bypass diodes. In this paper we investigate the current mechanisms and device performance with particular attention to the regions of n^+/p^+ overlap. In the first part of this paper we report on the status of our experimental buried emitter solar cell development.

However, the concept of burying a boron-doped *p*-type emitter beneath a phosphorus-doped *n*-type surface layer can also be used to provide a dev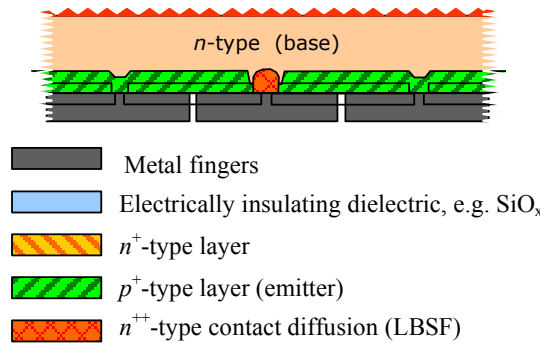ice structure where a boron-doped emitter can be effectively passivated by standard techniques such as thermal oxidation. Provided the existence of a reliable dielectric insulation, this technique may be used to passivate virtually the entire surface of a rear emitter that covers close to 100% of the solar cell area, as shown in Figure 3. In order to emphasize its high-efficiency potential we present in the second part of this paper PC1D [7] device simulations of this buried emitter solar cell configuration.

n-type (base)

	Metal fingers
	Electrically insulating dielectric, e.g. SiO$_x$
	n^+-type layer
	p^+-type layer (emitter)
	n^{++}-type contact diffusion (LBSF)

Figure 3: Cross sectional view of a "buried emitter" back junction solar cell that passivates virtually the entire surface area of a rear emitter. In this case, the device performance relies on the existence of a dielectric insulation layer.

INSULATING P-N JUNCTION

One advantage of the "buried emitter concept" [4, 5] is the possibility to exploit the fact that the space-charge region of a *p-n* junction has insulating properties. This allows shifting the task of insulating the emitter against the base metallization into the semiconductor as is shown in Fig. 2. All regions that are metallized by the base contacts have a surface layer of "base-type" doping, for example an *n*-type surface layer for solar cells made from *n*-type wafers. Consequently, any contact made between base metal and semiconductor would not lead to short-circuiting the solar cell, even if the contacting occurred at other locations than at the dedicated contact openings. Despite of having large portions of the surface covered by

base-type doping, it is still possible to have a contiguous and virtually full area emitter at the same time: We realise this task by having an emitter "buried" below the base-type layer as shown in Figure 2.

Even though it is not needed for electrical insulation, it is nevertheless advantageous to use a dielectric layer at the rear for passivation purposes. In case of the buried emitter solar cell presented here, we used a thermal oxide for passivating the rear side of the solar cell. Figure 4 provides a doping profile of our cells from one of those regions where phosphorus diffusion has been performed into a previously boron diffused surface. Note that the up to a depth of approximately 250 nm there is a phosphorus-doped *n*-type layer. Below this *n*-type layer there is a boron-doped *p*-type layer that serves as the buried emitter in the solar cell. The phosphorus concentration in the *n*-type layer is higher than the boron concentration in the *p*type layer. This situation allows the phosphorus within the surface-near *n*-type layer to overcompensate the remaining boron doping.

Figure 5 shows an *I-V* curve of our present rear-junction buried emitter solar cells under illumination equivalent to AM1.5. We measure a designated area solar cell efficiency of 19.5 %, using a shadow mask with an aperture of 3.92 cm^2. At the present state of our buried
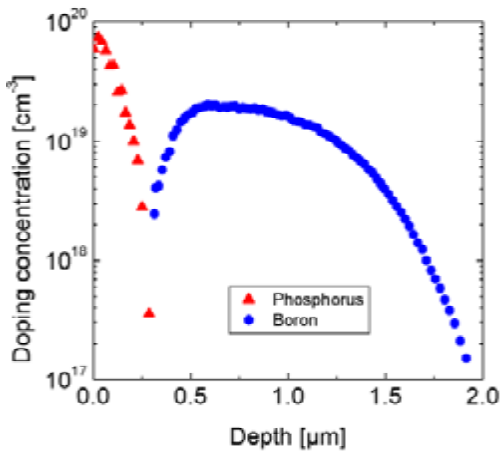
Figure 4: Solid symbols: Doping profile of the surface region, where phosphorus diffusion has been performed into a previously boron diffused surface as measured by electrochemical capacitance voltage profiling (solid symbols).

Figure 5: *I-V* characteristics of a non-tempered and of a slightly tempered (1min @ 330°C) buried emitter solar cell under illumination equivalent to AM1.5 spectrum.

emitter solar cell development, the open-circuit voltage is still rather low (V_{OC} = 644 mV). This is due to The fact that the cells reported here could not be properly alneal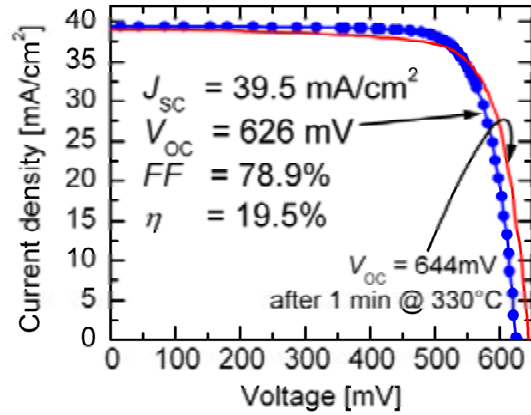ed by extended tempering at temperatures higher than 330°C. Note that after e-gun evaporation of aluminium the oxidised silicon surface needs to be tempered, preferably at approximately 400°C. However, such intense tempering was not viable for our present buried emitter solar cells: Due to processing imperfections, the contact openings to the base have not been well-aligned with the perforations of the *p*-type emitter (for a sketch of the ideal case see Figure 2 and 3). Consequently, tempering the solar cell produced spiking of the aluminium through the 250nm thin *n*-type layer into the *p*-type emitter, thus shortening base and emitter by aluminium already at 1 minute of tempering at 330°C. However, the fill factor of 78.9 % and the vanishing gradient of the *IV*-curve of the non-tempered cell near short-circuit indicate the absence of any significant junction shunting from trap-assisted tunnelling [6].

SIMULATION OF THE
P⁺-N⁺ JUNCTION PASSIVATION
We investigate the potential of the buried emitter solar cell structure by simulation with the PC1D model shown in Figure 6. In the simulation we use the measured doping profiles of Figure 4 and vary the passivation quality of
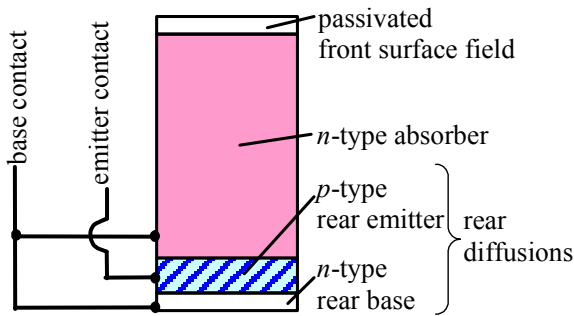
Figure 6: Schematic of the PC1D model used for exploring the efficiency potential of the buried emitter solar cell concept shown in Figure 3. The rear doping profiles used in the simulation are those of Figure 4.

the phosphorus-doped *n*-type surface layer by varying the surface recombination velocity $S = S_n = S_p$. The simulation results shown in Figure 7 are congruent with the assumption that the low open-circuit voltage of 626mV (untempered) of our first run of buriedemitter solar cells is associated with a depassivated SiO_x surface. According to the data of Ref. 8, we may assume that the oxidised surface of our cells with phosphorus surface concentration of $N_{dop,S} = 8 \times 10^{19} cm^{-3}$ reaches surface recombination velocities $S = S_n = S_p$ less than 4000 cm/s after tempering or alnealing. Consequently, the simulations suggest that our presently realised rear p^+/n^+ doping profile is already capable of producing buried emitter solar cells with open-circuit voltages reaching 680mV.

Figure 7: Simulated buried emitter solar cell performance, using the model shown in Figure 6 and the doping profile of Figure 4.

CONCLUSION

We have introduced the back-junction buried emitter solar cell concept and presented initial solar cell results with efficiencies o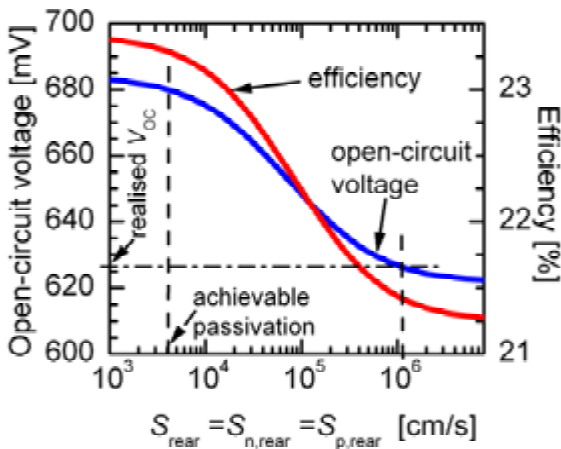f 19.5%. The buried emitter structure uses an *n*-type layer on the surface of a *p*-type boron-doped emitter. This technique allows efficiently passivating boron-doped emitters by standard techniques such as thermal oxidation. Our 1-dimensional device simulations suggest that the buried emitter solar cell is capable of achieving open-circuit voltages of 680mV as well as efficiencies well above 22%.

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Free energy losses analysis for solar cells

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Abstract: This paper analyses power losses in arbitrary solar cells in terms of free energy rather than recombination currents and Joule dissipation. We derive equations for the loss rates of free energy due to recombination, transport of electrons, and transport of holes, respectively. The electrical power extracted from the cell equals the photogeneration rate of the free energy minus all the above loss rates. By considering the free energy, all entities have units of mW/cm^2. Thus, transport losses due to Joule heating, due to diffusion, or a combination of both become directly comparable in magnitude with recombination losses (the latter are usually quantified in mA/cm^2 rather than mW/cm^2). The impact of various loss mechanisms on cells efficiency becomes apparent with this procedure. In particular, losses in free energy due to minority carrier diffusion become an integral part of device optimization.

Motivation

Solar cells absorb solar radiation and produce electrical power. Electrical power is free of entropy and may therefore be considered as a rate of free energy $\dot{F}$ being produced by the solar cell. Numerical solutions of the semiconductor equations [1] are commonly used to optimize a cell design for maximum electrical power output $\dot{F} = J_Q\, U$, where U is the terminal voltage and J_Q is the terminal current, e.g. both taken at the maximum power point. In the analysis of these solutions, two often considered loss channels are carrier recombination and resistive losses. Recombination losses are commonly quantified as charge current-densities j_Q per cell area (mA/cm^2) while resistive losses are usually determined as dissipated resistive heat $\dot{f}_{heat}$ per cell area (mW/cm^2) [2,3]. The relative impact of the two losses on cell efficiency is difficult to judge due to the different units.

Recombination currents that occur at positions in the cell where the splitting of the quasi-Fermi level is large dissipate more free energy than recombination currents of identical magnitude occurring at positions with little quasi-Fermi level splitting. Thus, simply multiplying the recombination currents by the terminal voltage U is not appropriate. Instead, weighting the recombination current-losses with the local quasi-Fermi level splitting transforms current-losses into loss-rates of free energy and makes transport losses and recombination losses directly comparable (both in mW/cm^2). We therefore introduce a free energy loss analysis (FELA), which makes the potential gain in output power by avoiding losses immediately apparent.

Theory

Text book knowledge [4] of solar cells is the starting point for deriving our free-energy analysis. The free energy (or electrochemical potential) of electrons is identical to the quasi-Fermi level of electrons in the conduction band E_{FC}, while the free energy of holes (electrochemical potential of holes) equals the negative quasi-Fermi level of holes in the valance band $-E_{FV}$. The charge current-density of electrons

$$\vec{j}_{Q,e} = \sigma_e\, \vec{\nabla} E_{FC} \qquad (1)$$

and the charge current-density of holes

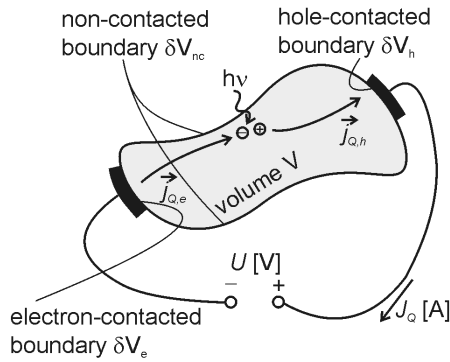$$\vec{j}_{Q,h} = \sigma_h \, \vec{\nabla} E_{FV} \qquad (2)$$

both depend on the respective conductivities σ_e and σ_h. The current-density of the free energy F carried by negatively charged electrons is

$$\vec{j}_{F,e} = E_{FC} \, \vec{j}_{Q,e} / q, \qquad (3)$$

With q being the elementary charge. The current-density of the free energy carried by positively charged holes is

$$\vec{j}_{F,h} = -E_{FV} \, \vec{j}_{Q,h} / q. \qquad (4)$$

Figure 1 sketches the solar cell volume V that has the boundary surface δV.

non-contacted boundary δV_{nc} hole-contacted boundary δV_h

$h\nu$

$\vec{j}_{Q,h}$

volume V

$\vec{j}_{Q,e}$

U [V]

electron-contacted boundary δV_e

J_Q [A]

Figure 1: A photon generates en electron-hole pair in a solar cell of volume V. Electrons and holes contribute to the electron- and hole currents $\vec{j}_{Q,e}$ and $\vec{j}_{Q,h}$ respectively. Some of the generated charge carriers are extracted through the respective contacts. The boundary δV of the cell volume V consists of contacted and non-contacted regions.

The surface of volume V consists of the electron contact δV_e to an n-type semiconductor, the hole contact δV_h to a p-type semiconductor, and the non-contacted surface δV_{nc}. We assume that the contacted surfaces δV_e and δV_e are equipotential surfaces. The free energy extracted per time is

$$U \, J_Q = \int_{\delta V_e} d\vec{A} \left[\vec{j}_{F,e} - \frac{\vec{j}_{Q,h}}{q} (E_{FC} - E_{FV}) \right]$$
$$+ \int_{\delta V_h} d\vec{A} \left[\vec{j}_{F,h} - \frac{\vec{j}_{Q,e}}{q} (E_{FC} - E_{FV}) \right] \qquad (5)$$

Where U is the voltage between the terminals (δV_e and δV_h) of the device and J_Q the external current. Equation (5) states that the extracted

free energy per unit time at the electron contact δV_e equals (a) the flux of free energy carried by electrons into the electron contact minus (b) a term representing the loss of free energy due to recombination at the contact. In each of the integrals, $d\vec{A}$ is an outward pointing area element on the boundary surface δV of volume V. We may rewrite equation (5) by extending the integration surfaces to the full surface δV:

$$U \, J_Q = \int_{\delta V} \frac{d\vec{A}}{q} \left(E_{FC} \, \vec{j}_{Q,e} - E_{FV} \, \vec{j}_{Q,h} \right)$$
$$- \int_{\delta V_{nc}} \frac{d\vec{A}}{q} \left(E_{FC} \, \vec{j}_{Q,e} - E_{FV} \, \vec{j}_{Q,h} \right)$$
$$- \int_{\delta V_e} \frac{d\vec{A}}{q} \vec{j}_{Q,h} \left(E_{FC} - E_{FV} \right)$$
$$- \int_{\delta V_h} \frac{d\vec{A}}{q} \vec{j}_{Q,e} \left(E_{FC} - E_{FV} \right) \qquad (6)$$

The latter two integrals in equation (6) represent the loss of free energy due to recombination at the contacts, whilst the integration over the surface δV_{nc} accounts for the recombination at the non-contacted surfaces. Using Gauß's theorem, we convert the first surface integral into a volume integral

$$\int_{\delta V} \frac{d\vec{A}}{q} \left(E_{FC} \, \vec{j}_{Q,e} - E_{FV} \, \vec{j}_{Q,h} \right)$$
$$= \int_V \frac{dV}{q} \vec{\nabla} \left(E_{FC} \, \vec{j}_{Q,e} - E_{FV} \, \vec{j}_{Q,h} \right)$$
$$= \int_V \frac{dV}{q} \left(\begin{array}{c} \vec{\nabla} E_{FC} \, \vec{j}_{Q,e} + E_{FC} \, \vec{\nabla}\vec{j}_{Q,e} \\ -\vec{\nabla} E_{FV} \, \vec{j}_{Q,h} - E_{FV} \, \vec{\nabla}\vec{j}_{Q,h} \end{array} \right)$$
$$= \int_V \frac{dV}{q} \left(\begin{array}{c} -q(E_{FC} - E_{FV})(g - r) \\ + \vec{\nabla} E_{FC} \, \vec{j}_{Q,e} - \vec{\nabla} E_{FV} \, \vec{j}_{Q,h} \end{array} \right) \qquad (7)$$

where the divergence of the current-densities

$$\vec{\nabla}\vec{j}_{Q,e} = -q(g - r), \qquad (8)$$

$$\vec{\nabla}\vec{j}_{Q,h} = +q(g - r), \qquad (9)$$

are given by the local carrier generation rate g and the local carrier recombination rate r.

Let now A be the cell area (projection of the volume V in the direction of the sun) and $j_Q = J_Q / A$. Using (1) and (2) for replacing the

114

gradients of the Quasi-Fermi levels yields the extracted free energy density rate

$$-\dot{U}\ j_Q = \dot{f}_g - \dot{f}_r - \dot{f}_s - \dot{f}_{t,e} - \dot{f}_{t,h} , \qquad (10)$$

where the photogeneration rate of the free energy density is

$$\dot{f}_g = A^{-1}\int_V dV\ (E_{FC} - E_{FV})\,g\ , \qquad (11)$$

the free energy density dissipation rate by recombination within the volume is

$$\dot{f}_r = A^{-1}\int_V dV\ (E_{FC} - E_{FV})\,r , \qquad (12)$$

the free energy density dissipation rate by recombination at the contacts and surfaces is

$$\dot{f}_s = A^{-1}\int_{\delta V_{nc}} \frac{d\vec{A}}{q}\left(E_{FC}\,\vec{J}_{Q,e} - E_{FV}\,\vec{J}_{Q,h}\right)$$

$$+\,A^{-1}\int_{\delta V_e} \frac{d\vec{A}}{q}\,\vec{J}_{Q,h}\left(E_{FC} - E_{FV}\right) , \qquad (13)$$

$$+\,A^{-1}\int_{\delta V_h} \frac{d\vec{A}}{q}\,\vec{J}_{Q,e}\left(E_{FC} - E_{FV}\right)$$

the free energy density dissipation rate by transporting electrons is

$$\dot{f}_{t,e} = A^{-1}\int_V dV\ \left|\vec{J}_{Q,e}\right|^2 / \sigma_e\ , \qquad (14)$$

and finally the free energy density dissipation rate by transporting holes is

$$\dot{f}_{t,h} = A^{-1}\int_V dV\ \left|\vec{J}_{Q,h}\right|^2 / \sigma_h\ . \qquad (15)$$

Equations (14) and (15) are the expressions to be expected for resistive heating. However (14) and (15) cause a loss $\dot{f}_t > 0$ even if the electric field vanishes and the current is driven by diffusion only. This is the case for minority carriers at low-level injection in a homogenously doped semiconductor. A current driven by a gradient of the electrostatic potential (drift), by a gradient of the chemical potential (diffusion) or by a mixture of both all cause a free energy loss expressed via the same equations (14) and (15).

The physical origin for the dissipation of free energy by diffusion is less intuitive than for resistive heating. Carriers diffuse from positions of high to positions of low concentration. A high carrier concentration

corresponds to a small amount of entropy per particle. When diffusing, the carriers increase their entropy and thus reduce the entropy-free part of their total energy. This explains the dissipation of free energy by diffusion.

Example
We now give a sketch of a first example for a FELA on the basis of a 2-dimensional simulation of a crystalline silicon emitter wrap through solar cell. Figure 2 shows a schematic of the simulated 2-dimensional unit cell. The shaded area on the left is the 2-dimensional representation of the diffused vias (EWT holes), which electrically connect the front-side and rear-side emitter.
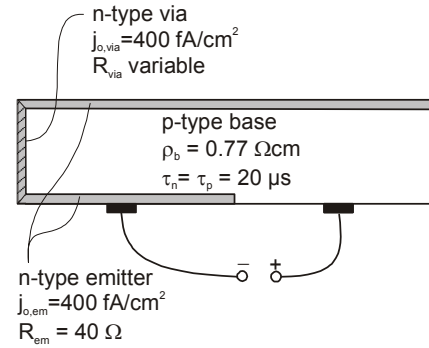
Figure 2: 2-dimensional unit cell of an emitter wrap through solar cell. The via on the left is marked shaded and has a resistance R_{via} that we vary in our simulations.

Similarly to the EWT-solar cell simulations of Ref 5, Figure 3 shows the simulated open-circuit voltage U_{oc}, short-circuit current density j_{sc}, fill factor FF, and the efficiency of the EWT solar cell as a function of the resistance R_{via} of the via. Figure 4 shows the FELA at the respective maximum power points. The full circles in Fig. 4 denote the power extracted from the cell while the open circles are the sum of the four above mentioned free energy density loss rates. The sum of extracted power density and all lost power density is the photogenerated free energy density. When looking at Fig. 3, one could argue that the poor fill factor near $R_{via} = 10^4\ \Omega$ originates from resistive losses in the via. The FELA, however, immediately shows that at $R_{via} = 10^4\ \Omega$ the free energy density dissipated in
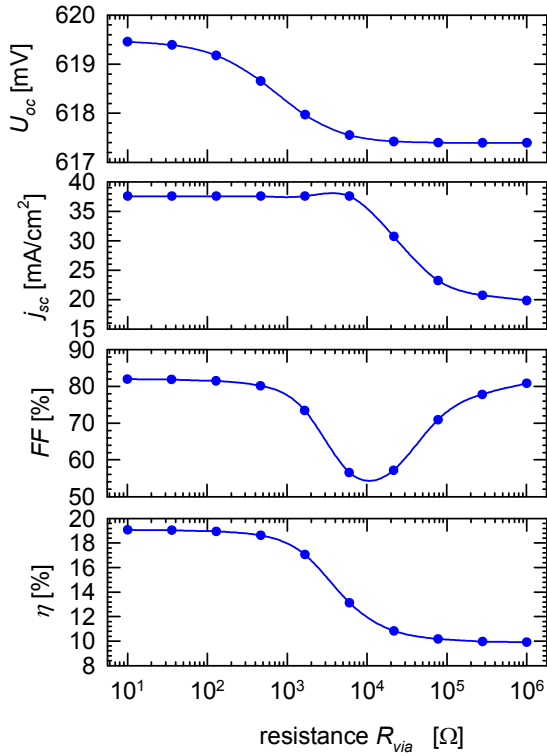
Figure 3: Open circuit voltage U_{oc}, the short circuit current density j_{sc}, the fill factor FF and the efficiency η of the illuminated current-voltage curve when varying the resistance R_{via} of the via.
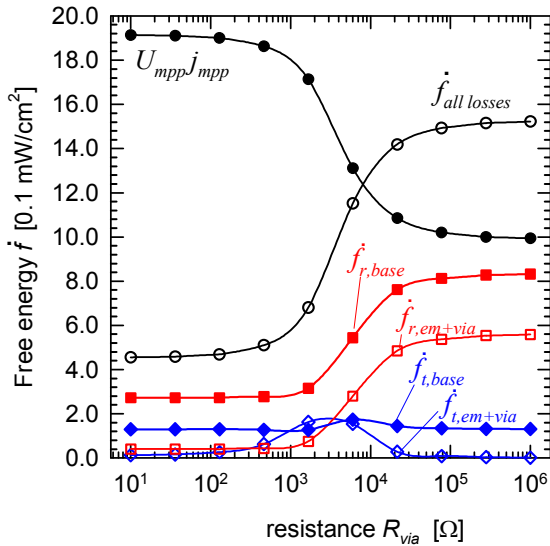
Figure 4: Rates of extracted free energy density $U_{mpp}j_{mpp}$ and of free energy density losses. Squares: Recombination losses within emitter+via and within base. Diamonds: Free energy losses related to charge carrier transport within emitter+via and within base.

R_{via} (relative to R_{via} =10 Ω) is much smaller than the increase of the recombination losses. The efficiency loss due to power density dissipation in the via is at maximum 1% and even negligible at very small and very large values of R_{via}, due to vanishing voltage at and vanishing current through the resistor, respectively. Thus it is not Joule dissipation deteriorating the efficiency, but a change in the recombination pattern [6] when changing R_{via}.

Conclusions

A procedure to analyze the losses in solar cells in terms of free energy rather than recombination currents and Joule dissipation is derived. Starting from the terminal current and voltage, local loss rates of free energy in the interior of the cell are derived by applying Gauss' theorem. By integrating separately over various device regions, contributions of these regions to the total losses can be analyzed. In particular, transport losses due to Joule heating, due to diffusion, or a combination of both become directly comparable in magnitude with recombination losses. This opens up new strategies for device analysis and optimisation.

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The solubility of carbon in liquid silicon equilibrated with silicon carbide and its dependence on boron levels

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The temperature dependence of carbon in liquid silicon equilibrated with silicon carbide has been determined through a direct experimental investigation. The solubility of carbon in liquid silicon has been determined to 65 ppm mass at the melting point of silicon. In addition, it has been demonstrated that the solubility of carbon in liquid silicon increases with increasing boron levels in the melt.

1 INTRODUCTION

Carbon, while not electrically active, does have a deteriorating effect on solar cell performance. It can be present in feedstock silicon from the reduction of quartz, or it can enter the melt from the graphite susceptor system in the furnace via the gas phase. The Si-C system is therefore an important system to study and understand. The same is true for ternary systems involving silicon and carbon together with a second important trace element. Since boron is a common doping element, the Si-C-B system falls into this category.

There exist many publications on the Si-C system [1, 2, 3, 4, 5]. However, published results are frequently at variance with one another, and the discrepancies are often very large; Table 1 shows literature values for the solubility of carbon in liquid silicon as an example.

This paper presents experimentally obtained solubility data on carbon in liquid silicon with varying boron levels. It describes the furnace and experimental setup used, and gives details on the sample-taking process. A discussion of the results obtained compared to the existing literature is also presented.

Table 1: Literature values for the solubility of carbon in liquid silicon at the melting point of silicon.

61 ppm mass	Hall, 1958 [1]
23 ppm mass	Scace and Slack, 1959 [2]
57 ppm mass	Ottem, 1993 [3]
80 ppm mass	Yanaba et al, 1997 [4]
112 ppm mass	Durand and Duby, 1999[5]

2 APPARATUS

The furnace used is a resistance heated tube furnace. The furnace chamber consists of a $\varnothing_{int}$50 mm x $\varnothing_{ext}$60 mm x 630 mm dense alumina furnace tube closed with water cooled brass plates at the top and at the bottom. Around this is a 200 mm long $MoSi_2$ resistance coil. The heating spiral is insulated by an $\varnothing_{int}$80 mm x $\varnothing_{ext}$290 mm x 350 mm cylinder of porous alumina, outside which is a water cooled shell of brass and aluminium.

The top flange of the furnace has four inlets, two of which are designed for gas. In the present work, one of these has been sealed off, while the other is used for argon flow into the furnace. Of the other two inlets, one is used for a type S Pt-Pt10%Rh thermocouple measuring the melt temperature. Another thermocouple is placed near the hottest point on the heating spiral, and is used to control the furnace temperature with a Eurotherm 903P temperature controller. All temperature measurements in this article refer to the melt temperature.

The final inlet is used for the sample taking and is fitted with a ball valve, a 115 mm long steel tube, and a sealing mechanism with three o-rings. The samples were extracted using $Ø_{int}2$ mm x $Ø_{ext}4$ mm quartz tubes fitted with a syringe. If approximately 0.5 mL/1 g melt is sucked into the tube, this corresponds to roughly 137 mm of the tube being filled with silicon, while the distance between the ball valve and the bottom o-ring is about 160 mm. This prevents damage to the o-ring, since the valve can be closed beneath the nozzle of the sampling tube with all the hot silicon inside the metal tube still below the o-ring.

3 EXPERIMENTAL PROCEDURE AND SAMPLE PREPARATION

In each experiment, a fresh graphite crucible ($Ø_{int}38$ mm x $Ø_{ext}44$ mm x 95 mm, Tanso AB IG-610 material) was stacked with high purity polycrystalline silicon feedstock (REC ScanWafer) and loaded into the furnace. The total mass of each casting was approximately 75g; in two castings elemental boron (Boron powder, crystalline, 99.9%, Alfa Aesar 44257) made up 1.5% and 2% of the mass respectively, while in the other four castings 100% silicon were used. The furnace was then evacuated and heated to 1000°C in vacuum over a period of approximately 150 min before the furnace was filled with Ar-gas to ambient pressure.

Next, the temperature was taken to 1414°C over a period of approximately 120 min, and the silicon melted. It was assumed, and subsequently confirmed during microprobe analysis, that once the silicon was melted, it would react with the graphite crucible and form a layer of silicon carbide on the crucible-melt interface. Equilibrium would then be established between carbon in the form of silicon carbide, and carbon dissolved in liquid silicon:

$$SiC \square \quad Si + \underline{C}$$

It was desirable to determine whether there existed an appreciable time delay before equilibrium was established. To this end, the settlement time, t_s, for which the melt had been held at the sampling temperature, was recorded for each sample.

To prevent air leakage, the pressure in the furnace was increased to slightly above one atmosphere before each sample taking. This would cause any leakage during sampling to be mainly argon flowing out of the furnace rather than air flowing into it.

The samples were etched in concentrated HF for a couple of days in order to completely get rid of the quartz tube. The silicon was then rinsed in distilled water, and analysed for carbon content using LECO. The analyses were carried out externally, at Elkem Fiskå.
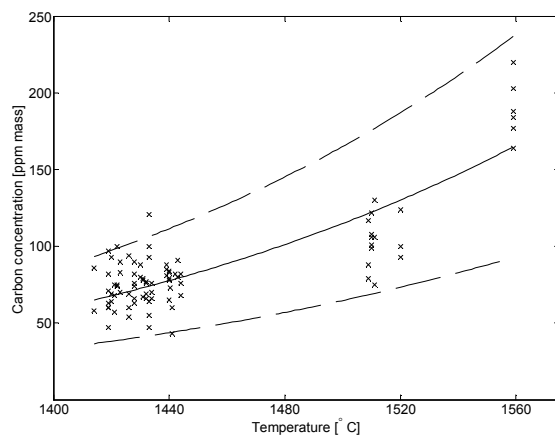
Figure 1: Carbon concentration as function of temperature. The best fit Arrhenius equation is shown together with the experimental points, with the dashed lines representing a 95% confidence interval for the predicted equation.

4 RESULTS AND DISCUSSION

From a total of four experimental runs with no boron additions, a total of 36 samples were extracted in the temperature range 1414°C-1559°C and analysed in three series of 13 samples each. In addition, two castings were performed with additions of 1.5% and 2% boron, from which a total of 15 samples, extracted between 1433°C and 1507°C, were analysed. All samples were analysed in 1-4 parallels, depending on the amount of sample available.

Since some parallels deviated rather much from the other results at a given temperature, it was decided to define any parallel that differed from the average value at its temperature by more than two standard deviations as an outlier, and leave it out of the. All parallels that were left out in this manner displayed too high values, indicating carbon contamination.

4.1 The solubility of carbon in liquid silicon as a function of temperature

Attempts to fit an Arrhenius type equation to the solubility data as a function of settlement time revealed that no time delay were detectable, and thus no samples had to be ignored in the discussion on account of them having been extracted under pre-equilibrium conditions.

The solubility data was fitted to an Arrhenius equation as a function of temperature using the method of least squares. The best fit equation was

$$C^C(T) = 8.394 \times 10^6 e^{\frac{-19856}{T}}$$

This equation is plotted together with the data points in Figure 1, while Figure 2 shows a comparison of the found equation with similar results from literature. At the melting point of silicon, the equation gives a solubility of 65 ppm mass at the melting point of silicon, which is more or less in the middle of the values from literature quoted in Table 1.

4.2 The effect of boron on the solubility of carbon in liquid silicon.

Arrhenius equations were also fitted to the solubility data for the cases when boron had been added, giving

$$C^C_{1.5\%B}(T) = 2.756 \times 10^6 e^{\frac{-17099}{T}} \quad \text{and} \quad C^C_{2.0\%B}(T) = 4.100 \times 10^6 e^{\frac{-17721}{T}}$$

for the cases of 1.5% and 2% boron respectively. Extrapolated to the melting point, these give 109 and 112 ppm mass for the solubility of carbon in liquid silicon, increases of 68% and 72% compared to the boron-free samples. Figure 3 shows a plot of the three equations for the carbon solubilities, with 0%, 1.5% and 2% boron.
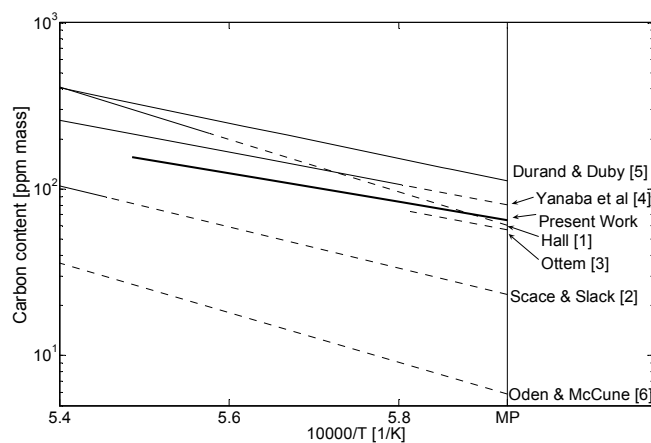
Figure 2: Carbon concentration as function of temperature, compared with results fron literature. Dashed lines represent extrapolations outside the region of experimentation.

It should be noted that at the time of writing, analyses to confirm the boron levels in the samples have not yet been carried out, so a precise quantification of the boron dependence of the carbon solubility is not undertaken as of yet. But the current work clearly demonstrates that the carbon solubility increases with the presence of boron, and furthermore that the increase is larger for higher boron levels. This is consistent with the work of Yanaba et al[4].
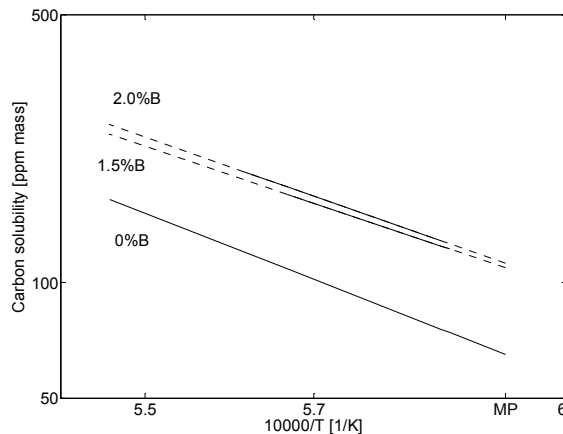
Figure 3: Carbon solubility as a function of temperature for varying boron levels. The dashed lines indicate extrapolations outside the area of experimental investigations.

5 CONCLUSIONS/FURTHER WORK

An equation has been determined that describes the temperature dependence of the solubility of carbon in liquid silicon equilibrated with silicon carbide. At the melting point of silicon, this equation gives the solubility as 65 ppm mass. These results fall in the middle of existing results from literature. In addition, it has been demonstrated that the carbon solubility is dependant on the boron content, and that it increases with increasing boron levels. The precise dependence has not yet been established, as the precise boron contents have not been confirmed by chemical analysis. Future work will include performing such analyses, in addition to the performing of additional experiments to increase the available data.

ACKNOWLEDGEMENTS
The authors wish to thank Elkem Solar for financial support with analyses.

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Effects of Annealing on Electrical Properties of Polycrystalline Silicon

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Abstract

Effects of annealing on the recombination velocities at grain boundaries and on the distribution of nickel are investigated by electron beam induced current (EBIC), μ-x-ray fluorescence (XRF), and x-ray absorption near edge spectra (XANES) methods. In the as-grown crystal, most of grain boundaries including $\Sigma 3$ act as recombination centers. The recombination velocity at $\Sigma 3$ drastically decreases by the thermal annealing. The velocities at $\Sigma 9$ and $\Sigma 27$ boundaries also decrease due to the annealing, but still relatively high. The recombination activities at some random grain boundaries remain high and a large amount of nickel exists as nickel silicide along the boundary even after the annealing. In the grains, the electrical properties at the particular area of intra-grain were deteriorated by the high temperature annealing and the nickel precipitates were formed.

1. Introduction

Crystalline silicon (Si) technology has dominated the production of solar cells, which contributed over 90% of the world's PV production. Because of the lower cost and relatively better conversion efficiencies, the poly- crystalline Si solar cells are dominant in the crystalline Si solar cell market. The recent rapid growth of Si solar cell market causes the lack of Si feed stock. Then, to increase the production of Si feed stock and to reduce the cell cost, much effort has been focused on the development of the solar-grade Si (SOG-Si). However, the impurity concentration in the Si wafer grown by using SOG-Si is commonly high. The small amount of metal impurities, such as iron and nickel, cause the minority carrier lifetime severe degradation, resulting in the low conversion efficiency of solar cells. In order to establish new processes for fabricating the solar cells with the satisfactory high conversion efficiency even from the SOG-Si, it is important to understand the behaviors of these impurities and to reduce them. The most of metal impurities can be removed from the polycrystalline Si by a phosphorous gettering. During the gettering process, many impurity atoms diffuse in the crystal due to the high temperature and they are trapped at the gettering sits. Then, the average minority carrier lifetime is improved and the relatively high conversion efficiency is realized. But, some impurity atoms remain at some particular grain boundaries and at the defects in the crystal. They deteriorate the solar cell performance. Therefore, it is strongly required to understand the gettering process, that is, the effects of thermal annealing on the electrical properties of the poly crystalline Si. In this study, the recombination velocities at the grain boundaries, the distribution of metal impurity nickel, and its chemical state were studied as a function of annealing condition by EBIC, XRF and XANSE analysis.

2. Experiment

The Ga doped polycrystalline Si was used in this study. It was grown by our original traveling heater furnace [1]. The silicon feedstock used here was off-specification of electronics grade. The heater transfer rate during growth was 15 - 30 mm/hr. The grown ingot has a cylindrical shape with a diameter of 10 cm and height of 10 cm. The ingot was sliced to a thickness of 300μm wafer. The neighboring three substrates, which have the relatively same grain structures, around the fraction solidified, X=0.85, were used, because the concentration of impurities were relatively high due to the segregation phenomena. The averaged impurities concentrations were as follows; iron: 3.5 x10^{13}, cupper: 1.0x10^{14}, and nickel: 3.3 x 10^{14} atoms/cm^3. They were determined by the inductively coupled plasma mass spectrometer and the atomic absorption spectrometry methods. The resistivity of crystal was 0.3μcm, and the average lifetimes of the as-grown substrate were 0.3 - 0.4μsec. Before the measurements, the surface damage layers were removed by chemical etching with a mixture of nitric and hydrofluoric acids. One substrate was unprocessed, the others were annealed at 650℃ for 120 min and 1000℃ for 90 min in a N$_2$ ambient, respectively. The electrical activities were characterized by the EBIC measurements. Here, Al-Schottly structures were adopted. The crystallographic orientation was analyzed by the scanning electron microscope (SEM) equipped with an electron backscatter diffraction (EBSD) pattern collection system, and the sigma number of each boundary was determined. The distribution of nickel and its chemical state was evaluated by using the synchrotron beam line 37 XU at the Spring-8. The distribution was measured by the μ-XRF mapping with energy of 10keV. The beam size was 0.7μm x 1.5μm and the sampling pitch was 5μm. The chemical states were determined by XANES measurements.

3. Results and Discussion

The EBIC images and crystallographic orientation maps were shown in Fig. 1. The darker line in EBIC images indicates the higher recombination velocity. Most of grain boundaries including Σ3 act as recombination centers in the as-grown crystal. The contrast differences indicate that the recombination velocities vary depending on the structure of the grain boundary
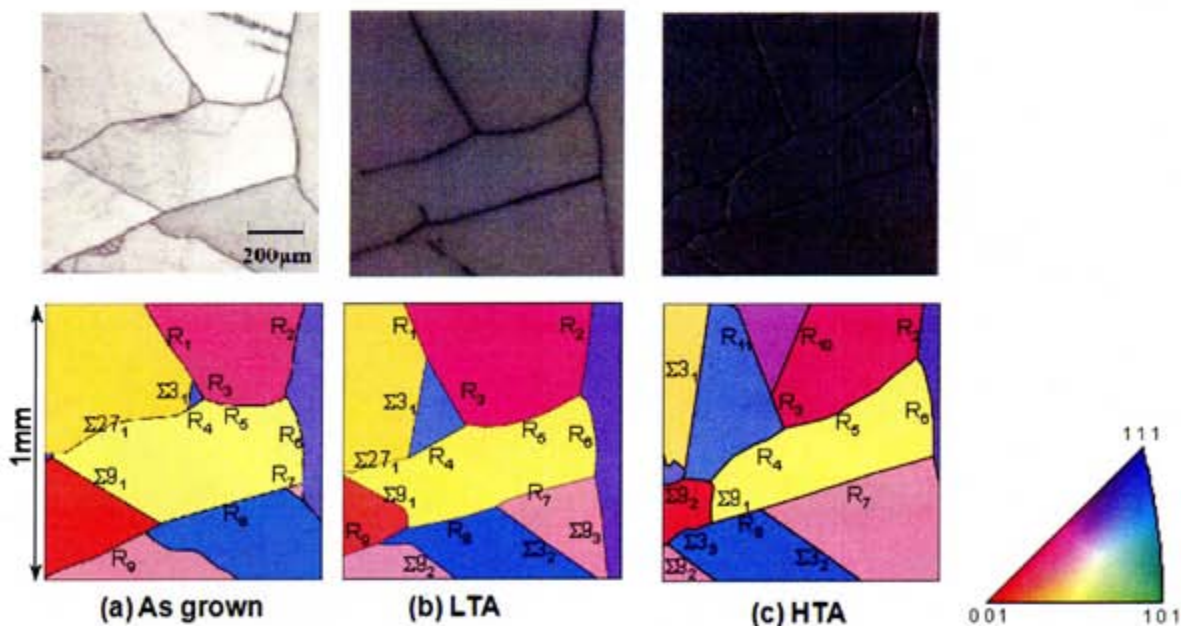

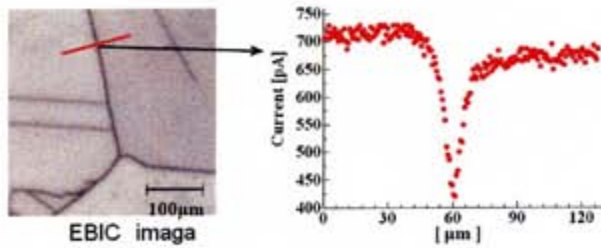Fig. 1 EBIC images and crystallographic orientation maps

Fig. 2 EBIC image and line profile of EBIC current.

2), the diffusion length L of the minority carrier and the recombination velocity S at the boundary were estimated using the following equation.

$$\frac{I(L,S,X)}{I_\infty} = 1 - \frac{2}{\pi}(1+\alpha L)S \times \int_0^\infty \frac{\sinh^2 t \cdot \exp(-X\cosh t)}{\cosh t(S+\cosh t)(A^2+\sinh^2 t)}\,dt \qquad (1)$$
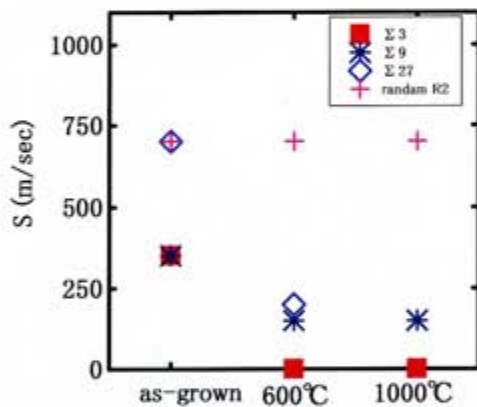

Fig. 3 Recombination velocity at grain boundaries.

and these values change by the low temperature (LTA) and high temperature (HTA) thermal annealing. For example, $\Sigma 3$ becomes not recombination site after the annealing. To discuss the effects of annealing condition on the recombination velocity at each grain boundary quantitatively, the velocities were evaluated by using the Zook's equation [2]. From the line profile of EBIC current (Fig. 2), the diffusion length L of the minority carrier and the recombination velocity S at the boundary were estimated using the following equation.

Here, I(L,S,X) is the EBIC current at the position X and I_∞ is the one at the position far from the boundary. The recombination velocity at $\Sigma 3$ boundary is shown in Fig. 2, as a function of annealing temperature. This is a twin boundary, which has a high symmetry and has no dangling bond along the boundary. However, in the as-grown crystal, this boundary acts as a recombination center. On the other hand, the annealing drastically decreases the recombination velocity, resulting in not recombination site. The $\Sigma 9$ and $\Sigma 27$ boundaries also act as the recombination centers (Fig. 3). These velocities also decreased by the thermal annealing. But, the velocity remains still high, and the value at $\Sigma 27$ is larger than that at $\Sigma 9$. As increasing the annealing temperature, the driving force of dissolution increased. Then, the metal impurities near the coincide boundaries diffused and the electrical properties were improved. But, it is not clear yet which the residual impurities at the $\Sigma 9$ and $\Sigma 27$ boundaries, or these boundaries themselves without impurities is the cause of high recombination velocity. The recombination velocity at the random grain boundary R2 is high and almost constant independent of the annealing conditions (Fig. 3). On the other hand, the minority carrier diffusion lengths L near these boundaries were improved by the thermal annealing. By the high temperature annealing, the dark spots appear in the grains. In some grains, there were many defects, which appeared as a etch pit by the etching. It is considered that they became the active recombination centers due to the high temperature annealing.

The nickel distributions of as-grown, low temperature annealed, and high temperature annealed substrates were shown in Fig. 4. In the as-grown crystal, the nickel atoms exist at the particular grain boundaries, such as random boundary, R1, R2, R7, R8, and R9. On the other hand,

nickel was not detected along R5, R6, and coincide sites. In the grains, the nickel can not be detected from the as-grown and low temperature annealed crystals. By the high temperature annealing, nickel exist at the random boundaries R2, R3, R5, R7, and at some coincide boundaries. The strong nickel signals were also obtained at the intra-grains. The defects in the grain accumulated the metal impurities and became the strong recombination centers.

The XANES spectrums of each sample are shown in Fig. 5. They are slightly different from each other and similar to that of nickel silicide. This indicates that many nickel atoms existed as nickel silicide and that they were precipitated along the grain boundaries and at the defects in the grain.
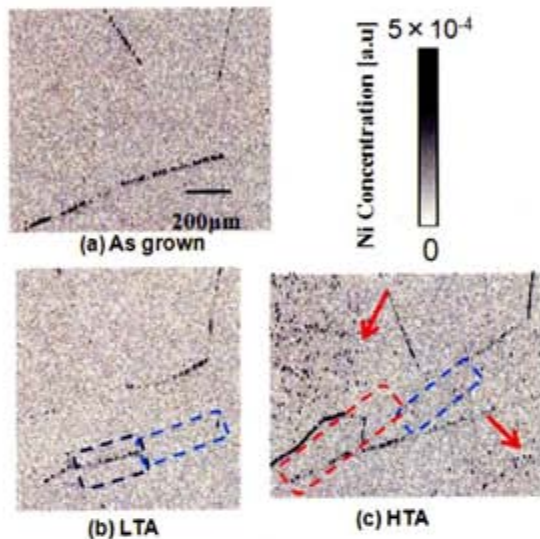
Fig. 4 Nickel distribution obtained by XRF.
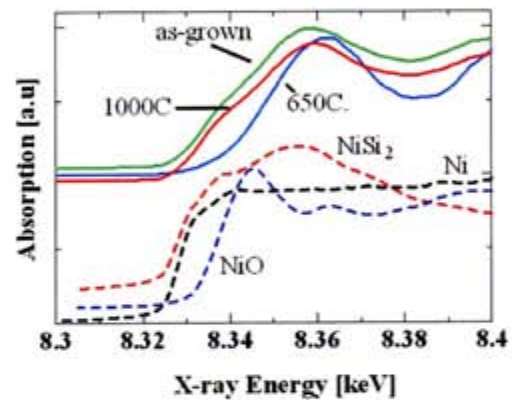
Fig. 5 XANES spectrums.

4. Summary

Effects of annealing on the recombination velocities at grain boundaries and on the distribution of nickel impurity were studied by EBIC, μ-XRF, and XANES measurements. In the as-grown crystal, most of grain boundaries including $\Sigma 3$ acted as recombination centers. The recombination velocity at $\Sigma 3$ drastically decreases by the thermal annealing. These velocities of $\Sigma 9$ and $\Sigma 27$ boundaries also decreased, but remained high value. The recombination activity at some random grain boundaries did not change by the thermal annealing, and the large amount of nickel existed as nickel silicide at the boundary before and even after the annealing. The high temperature annealing also caused the nickel silicide precipitations in the grains. They also deteriorated the electrical properties of polycrystalline Si.

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Extraction of Principle Stresses from Polariscopy Measurements

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Abstract

This paper summarizes the analysis of the extraction of principle stresses from polariscopy measurements. It is well known that polariscopy can be used to measure the maximum shear stress in thin silicon sheet samples, but the extraction of principle stresses is still a major problem in the measurement. In this paper, a method of extracting the principle stresses will be described.

1. Introduction

Georgia Tech is currently addressing the non-contact inspection of thin, flat silicon wafers to obtain the in-plane residual stresses. Residual stresses are believed to significantly influence breakage of wafers. Georgia Tech researchers have developed a polariscopy method that provides a way to obtain the in-plane residual shear stress in silicon wafers. However knowledge of shear stresses is not sufficient to determine the crack growth and wafer breakage because it is the principle stresses that are the key to understanding crack growth. In this paper, with the aid of four-point bending experiments, a way to extract the principle stresses from the polariscopy measurement is given.

The well known stress-optic law (Equation 1) can be used to obtain the shear stress in the wafers by the use of light scattering. The stress optic law is:

$$\tau_{max} = \left(\frac{\sigma_1 - \sigma_2}{2} \right) = \frac{\lambda}{4 \pi\, t\, C(\theta, \varphi)} \delta \quad (1)$$

where C is the stress-optic coefficient which is a function of θ (the principle stress orientation and φ (the crystal grain orientation), t is the thickness of the sample, λ is the wavelength of the light source, $\sigma 1$, $\sigma 2$ are the two principal stresses and δ is the phase retardation which can be measured by the six step phase stepping.

2. System description

The polariscopy system, Figure 1, shows the near infrared (NIR) light source, a narrow band filter, two polarizers, two waveplates, two lenses and a digital camera. A more complete description may be found in reference 1.
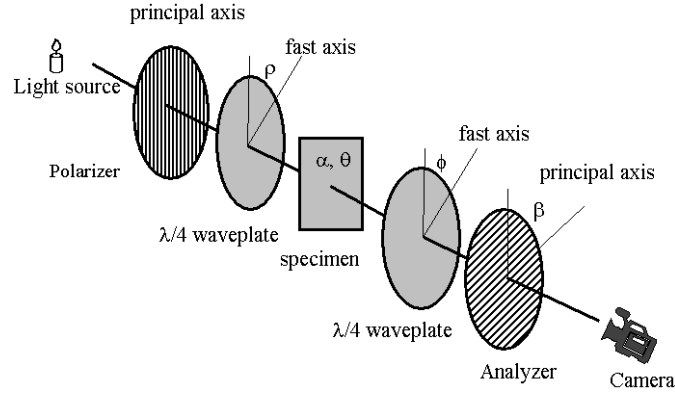
Figure 1: System Configuration of the Polariscope.

The system was calibrated using 4-point bending and Figure 2 shows the typical four point bending setup of the experiments, where a bending stress much bigger then the residual stress can be applied. Using equation 1, the stress-optic coefficient of a silicon wafer, or a grain within a wafer can be obtained, if the crystallographic orientations are known.
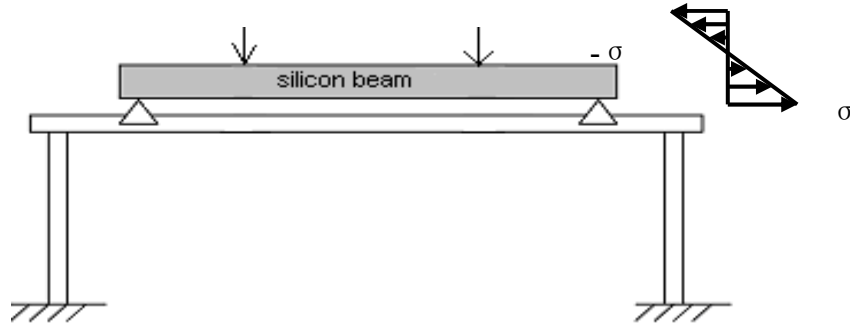
Figure 2: Schematic Diagram of the Four Point Bending Set-Up.

3. Determination of Principle Stresses

From equation 1, only the maximum shear stress is obtained. In order to determine the principle stresses, the first step is to determine the sign of the shear stresses measured. With the aid of four-point bending experiments, the sign of the shear stresses can be determined because the regions and distributions of the compressive and tensile stress are known. Equation 2 can be used to determine the sign of the residual stress and figure 3 shows the relations among the symbols in the equation.

$$\tan 2\theta = -\frac{\tau_r \sin 2\theta_r}{\sigma_{apply} + \tau_r \cos 2\theta_r} \quad \text{and} \quad \tau_r = \frac{\sigma_{1r} - \sigma_{2r}}{2} \quad (2)$$
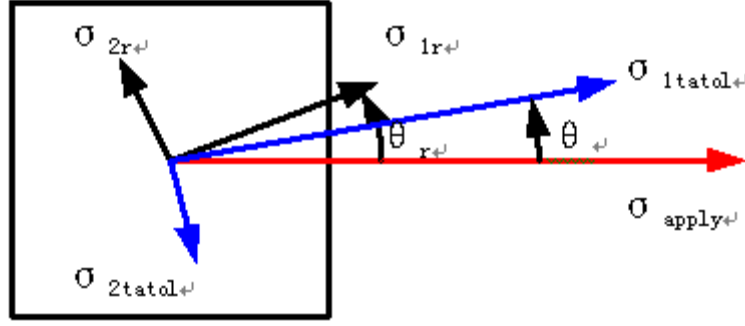
Figure 2 Relation between the applied stress and residual stress.

In the equation above, θ is the principle stress orientation of the total stress and θ r is the principle stress orientation of the residual stress. Assuming σ_{apply} is much bigger than the residual stress, then the sign of the denominator of the right hand side could be determined. θ and θ_r can be measured by polariscopy, so the sign of the residual shear stress can be determined.

The sign of the shear stress for the entire beam shown in Figure 1 can be obtained so the problem is then to extract the principle stress from a beam when the shear stress is known. The equations of equilibrium for a free body can be used to get the principle stresses and one equation of the type used for our geometry is shown in Equation (3).

$$\frac{\partial \sigma_y}{\partial y} + \frac{\partial \tau_{xy}}{\partial x} = 0 \qquad (3)$$

Converting equation 3 to a form amenable to FEA and at the free boundary of the beam $\sigma_y=0$, so that

$$\left(\sigma_y\right)_j = \left(\sigma_y\right)_i - \int_i^j \frac{\partial \tau_{xy}}{\partial x} dy \qquad \left(\sigma_y\right)_{i=0} = 0 \qquad (4)$$

Therefore the normal stress σ_y can be obtained through the width of the beam of Figure 2. Then the shear stress can be calculated using equation 5 and σ_x can be obtained using equation 6. Equation 7 is then used to calculate the principle stresses.

$$\tau_{xy} = \frac{1}{2}(\sigma_{1r} - \sigma_{2r})\sin 2\theta_r = \tau_r \sin 2\theta_r = \frac{\lambda}{4\pi t C(\varphi, \theta_r)} \delta \sin 2\theta_r \qquad (5)$$

$$\sigma_x = (\sigma_{1r} - \sigma_{2r})\cos 2\theta_r + \sigma_y = 2\tau_r \cos 2\theta_r + \sigma_y \qquad (6)$$

$$\sigma_{1,2} = \frac{\sigma_x + \sigma_y}{2} \pm \sqrt{\left(\frac{\sigma_x - \sigma_y}{2}\right)^2 + \tau_{xy}^2} \qquad (7)$$

4. Results

   This analysis was used to determine the principle stresses of a number of silicon beams: Figure 3 shows an example of the full components of residual stresses of the top portion of one such beam. The pixel size is 200μm.   Note that the normal stress σ_x is negative (compressive) therefore cracks will not propagate for this particular sample.
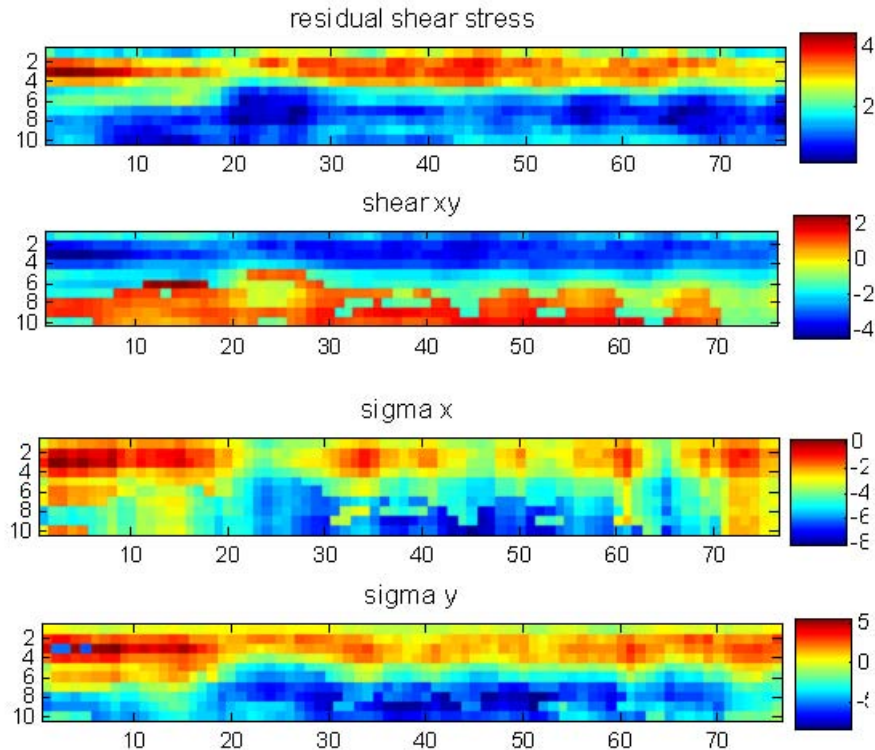
Figure 3 Full stress components of a beam.

5. Conclusions

1. Polariscopy provides a way to obtain maximum shear stresses.
2. Polariscope combined with four point bending allows the extraction of the full components of the stresses.

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Qualification of Wafers and Solar Cells Produced From Research-scale Minicaster

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Abstract

The wafers and cells produced from a 5 kg directionally solidified research-scale minicaster with a melt volume of 195 mm× 195 mm ×108 mm were evaluated. A tight resistivity range from 2.0~2.4 Ω-cm was obtained. The fully processed cells from the boron doped 5.0 kg multi-crystalline ingot were found capable of very good efficiency performance with an average of 15.03%. The minicaster was qualified to produce ingot to explore experimental trials with reduced cost and fast casting time compared to regular production crystalline furnace.

Introduction

In recent years, in order to resolve the shortage of polycrystalline solar-grade silicon feedstock photovoltaic, many silicon feedstock suppliers have made great efforts to produce the pure and low cost silicon suitable for terrestrial photovoltaic application. Consequently, a method is necessary to screen the candidate silicon and to reduce the cost for experimental trials for solar cell industries. "Minicaster", a research-scale directional solidification crystallization furnace with the melt volume scaled down for around 5 kg feedstock charging compared to a regular 265 kg production charging was constructed by Solar Power Industries (SPI), Inc. to meet this need [1].

In order to evaluate wafers from an ingot cast by the Minicaster, 5 kg of high purity polysilicon feedstock was cast into 195 mm× 195 mm ×108 mm vitreous quartz crucible, and was doped with boron for a target resistivity of 1.5 Ωm. The mini-ingot was then cropped into 156×156×40 mm brick and sliced into 156 mm square and 220 μm thickness multi-crystalline wafers. The wafers were sent to SPI regular production line for cell processing. The work presented in this paper is to characterize the wafers and cells produced from the doped minicast ingot and to evaluate Minicaster.

Experimental

The directionally solidified 5 kg multi-crystalline ingot was sliced by a commercial wire saw to produce 220 μm thickness wafers. The wafers were then cleaned with water and a commercial cleaning solution. Subsequently, the wafers were etched in KOH wet bench to remove saw damage, followed by a cleaning step with 1:5 HCl: H_2O solution and a rinse with DI water. After the wafers were dried in dryer for 30 minutes, three sample wafers were picked from the top, middle and bottom of the brick, photographed and then returned to their original positions, as shown in Fig.1.

Figure 1.   Pictures of wafers sliced from mini-cast ingots: 3 wafers from the top, middle and bottom locations of the doped mini-brick after KOH etching

All the wafers were then kept in order from the bottom to top of the brick, and the resistivity was measured on each wafer. Subsequently, three wafers from top, middle, and bottom locations, respectively, were selected and the material type was measured. The pre-diffusion lifetime was then tested after the surface was passivated using iodine methanol solution during photoconductivity decay (PCD) measurement. Next, another ten representative wafers from the top, middle, and bottom of the brick were identified as 3 groups T, M, and B. In this experiment, all the wafers pulled out from same location of the brick, such as the top (T), middle (M), and bottom (B), are the sister wafers with adjacent positions so that the quality of the same group wafers is similar, as shown in Fig. 2.
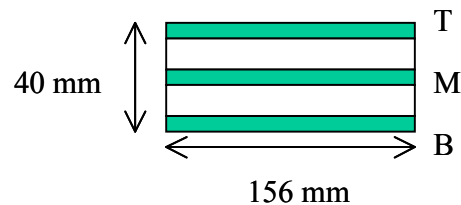
Figure 2.   Wafer location in mini-brick for group T, M, and B

The emitters were formed in a tube furnace using POCl$_3$ at a set temperature and with phosphorus diffused on both sides of each wafer and resulted in a ~40 Ω/square emitter. After diffusion, one wafer from the center position of each group was picked to measure minority carrier lifetime using the photoconductivity decay technique.

The remaining wafers were edge isolated using plasma etching. This was followed by the phosphorus glass removal and DI water rinse before a single layer

PECVD Si_3N_4 anti-reflection coating was deposited on the front at ~400 °C. Two wafers from each group were then selected for future test.

All the other wafers of three groups were then printed with Al back surface field (BSF) and dried at 200 °C. This was followed by Ag grid printing and drying. The samples then were co-fired in the IR belt furnace at a peak firing temperature optimized for the 156-mm^2 multi-crystalline solar cells. Each cell was then tested on performance and sorted by efficiency. Table-1 showed a summary of quantity of all the wafers used in this experiment.

Table 1. Quantity of wafers used in different tests of the experiment

GROUP ID	BRICK LOCATION	TOTAL WAFER QTY.	PRE-DIFUSSION (TYPE, RESISTIVITY, LIFETIME)	POST-DIFFUSION LIFETIME	FINAL CELL TEST	SAVE FOR FUTURE TEST
T	Top	11	1	1	7	2
M	Middle	11	1	1	7	2
B	Bottom	11	1	1	7	2

Results and Discussion

Resistivity, Lifetime and Sheet Resistance

Figure-3 shows the resistivity tested on all the wafers sorted by position. At the bottom side, resistivity is 2.0 Ω-cm, and it gradually increased to 2.4 Ω-cm at the top edge. The material type and lifetime measured on three sample wafers picked out after KOH etching were listed in Table-2. It was found that all three wafers were p-type. Pre-diffusion lifetime was measured at 5 locations on each wafer – upper left, upper right, center, lower left and lower right and an average was taken. Unlike resistivity, the highest pre-diffusion lifetime value (1.89µs) was found in sample from middle position, and the lowest lifetime (1.04µs) value was from the top location. This could be attributed to impurities formed near the top of the brick by directional solidification, which usually caused lifetime to increase from bottom end towards the top end, however showed a slight drop near the top end.
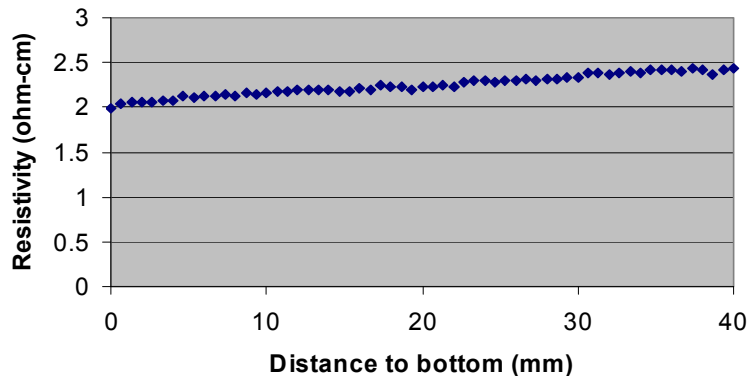

Figure 3. Resistively from bottom end to top end of mini-brick

Table 2. Wafer type, lifetime and resistivity

SAMPLE #	TYPE	AVERAGE PRE-DIFFUSION LIFETIME (µs)	RESISTIVITY (Ω-cm)	AVERAGE POST-DIFFUSION LIFETIME (µs)
T	P	1.04	2.3	16.48
M	P	1.89	2.1	15.58
B	P	1.73	2.0	15.57

Post-diffusion lifetime was measured on the center-position-wafer of group T, M, B using the photoconductivity decay technique, and the values were 16.48µs, 15.58µs, and 15.57µs, respectively, as shown in Table-2. It was found that the phosphorus gettering by $POCl_3$ process improved the minority carrier lifetime by over ten times compared to that of wafers before diffusion. As a consequence the quality of the wafers from the minicast ingot was judged to be good.

After $PCOl_3$ diffusion, the emitter was characterized by the sheet resistance of the 5th wafer (the center-position-wafer) in each group using SheRRescan. The sheet resistance was about 37 Ω /sq. with a low variation over the wafer area. So the sheet resistance of the emitter is relatively low but uniform (see Table-3). In the table, "Median" value means the number of wafers with a sheet resistance higher or lower than the median are equal.

Table 3. Sheet Resistance measured by SheRRescan

	Average (Ω /sq.)	Standard deviation	MEDIAN (Ω /sq.)	Max (Ω /sq.)	Min (Ω /sq.)
T	36.5	1.3	36.3	40.3	34.7
M	37.7	1.1	37.5	39.9	35.3
B	37.1	1.0	36.8	39.2	35.9

Cell Test Results Measured by Commercial Cell Tester

The IV-curves of the cells were measured using a commercial cell tester with a solar simulator at intensity of 1000 W/m^2 and in ~25 °C. The values of the series resistance and shunt resistance were obtained from the derivative of the IV curves around Voc (open circuit voltage) and around 0 V, respectively. Table -4 shows the median parameter values tested by cell tester after the wafers (totally 21 wafers, 7 wafers in each group) were run through whole cell processing procedures. Median results were used instead of the best results to fairly evaluate group performance. In table-4, the median series resistance from group T, M, and B are within $5\sim6\times10^{-3}$ Ω, and the shunt resistance are varies from 89.99 to 305.33 Ω. So, the shunt resistances and series resistance are good. The median value for Voc, Isc, and FF are 0.588~0.604 V, 7.76~7.86 A, and 0.774~0.787, respectively. These data are also within an acceptable good range. The highest median efficiency was observed in the middle group, and the lowest median efficiency is found at the bottom group. An over all average cell efficiency for the doped mini-brick is 15.03%.

Therefore, SPI constructed Minicaster can produce wafers from a 5 kg mini-ingot which is capable of very good solar cell performance.

Table 4. Median Cell Test Results in Each Group

	Wafer Qty.	Median Rs (Ω)	Median Rsh (Ω)	Median Voc (V)	Median Isc (A)	Median FF	Median Eff (%)
T	7	0.0058	305.33	0.603	7.76	0.787	15.12
M	7	0.0053	89.99	0.604	7.77	0.787	15.29
B	7	0.0063	119.75	0.588	7.86	0.774	14.67
Average		0.0058	171.69	0.598	7.80	0.783	15.03

Conclusions

We evaluated the wafers and cells produced from a research-scale minicaster. The boron doped mini-ingot (5.0 kg) cast by minicaster charging with high purity polysilicon chunks was successfully sliced into 156 mm square and 220 μm thickness wafers using regular commercial wire saw by SPI. A tight resistivity range from 2.0~2.4 Ω-cm was obtained. The fully processed cells were found capable of very good efficiency performance with an average at around 15.03%. Hence, the research-scale minicaster was qualified to produce very good wafers and cells using high purity polysilicon feedstock.

Acknowledgement

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Lock-in Thermographic Shunt Detection and Analysis of Upgraded Metallurgical Grade Silicon Solar Cells

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Introduction and Background

A great deal of effort has been directed at investigating methods of shunt detection in solar cells. The goal of this work has been to identify the mechanisms responsible for causing shunts. One method of shunt detection of particular interest is lock-in thermography (LIT). This method was first used by O. Breitenstein, et al. in 1994 to detect shunts by a technique called "Dynamical Precision Contact Thermography" (DPCT) [1]. In this method, a thermal sensor is placed in direct contact with the solar cell to identify areas of increased temperature caused by increased current flow while the solar cell is periodically biased. Contactless techniques have also been developed through the advancement of infrared (IR) camera technology. A thermal image of the solar cell under bias is acquired very quickly; less than a minute. As with the DPCT technique, Joule heating causes a local, periodic increase in temperature at an electrical shunt, which is detected by an IR camera. The sensitivity of the camera can be increased significantly by operating in a lock-in mode. The latter provides isolation of the periodic thermal signal from the noise while acquiring an image when synchronized with the periodically applied bias [2].

The term 'shunt' was defined by O. Breitenstein [3] in his earlier work. A shunt is generally described as a constant resistance that is in parallel with the p-n junction, and is thus indicated in an equivalent circuit model. Breitenstein refines this definition to include four 4 distinct types of shunts: pre-breakdown sites, linear or ohmic shunts, Schottky-type shunts, and recombination-induced shunts [3]. Of these shunt types some are process-induced shunts, while others are material-induced [3,4]. In order to identify these various types of shunts other techniques have been used including Light-beam induced current (LBIC), Electron-beam induced current (EBIC), Energy dispersive X-ray spectroscopy (EDX), Tunneling and Scanning Electron Microscopy (TEM and SEM). Lock-in thermography is used to identify the location, possible severity, and linearity of the shunt, while the other techniques provide microstructural and chemical analysis.

Experiment

We used upgraded metallurgical grade silicon (UMG Si) solar cells provided by CaliSolar Inc., and performed a series of LIT, LBIC, and SEM measurements in order to understand the amount of shunting and to investigate the mechanisms responsible for the shunting. Our lock-in thermography setup is based on a lock-in thermography system made by Electrophysics containing a 640×512 pixel InSb focal plane array thermocamera. The system was manufactured by Cedip Infrared Systems and included a 150x magnification lens [5]. The SEM images were taken with a Nova NanoSEM 630 by the FEI Company [6]. All images were taken with an acceleration voltage of 2 kV.

The LIT images were all taken with a lock-in frequency of 2.9 Hz, an applied square-wave AC voltage between 0-4V reverse bias, and a duty cycle of 50%. We measured 12, 125mm square, UMG Si solar cells provided by CaliSolar Inc. We selected three representative cells and defects to analyze using LIT and an SEM.

The first defect that we will report on is very detrimental to a solar cell performance and is becoming a more serious problem as the industry moves to thinner multicrystalline silicon wafers. This defect is a process-induced cracking of the wafer. The point during the processing at which the crack forms will determine the severity of the shunt. If the crack is formed after the processing has been completed, a weak nonlinear edge recombination current will be observed [7]. If the crack exists before the emitter layer is deposited or before the metal contact is screen-printed, a severe linear (ohmic) shunt will be observed. An example of this can be seen in figure 1. The optical signal from the crack is very large and was visible only with a traditional thermal image (lock-in thermograph was unnecessary to observe the defect). The data are shown in figure 1a, and became even more clear once the shunting area was magnified, figure 1b. The crack is clearly visible in figure 1b and extends from the lower left edge of the wafer, across the laser-cut edge isolation lines, and finally contacts the metal gridline on the upper right of the image.

The second observed defect appears to be a Schottky-type shunt. A solar cell with a good blue response requires that the emitter layer to be 0.3 μm or less. If during the sintering of the metal contacts, there is too much penetration of the metal into the silicon, the emitter metallization may diffuse through
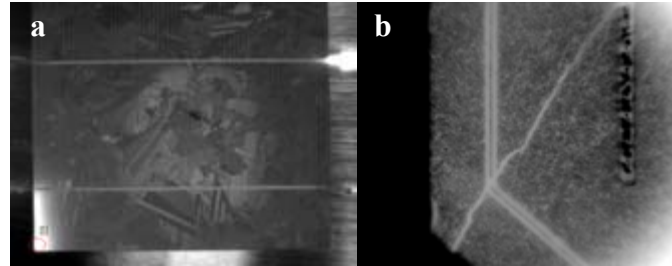
Figure 1: Thermal images of a crack, with (b) and without (a) 150x magnification.

Figure 2: A thermal image of the solar cell (a), a lock-in thermograph of the solar cell (b), a magnified thermal image of a shunt (c), one magnified lock-in thermograph of the shunt (d), one SEM image at 1000x magnification of the surface of the shunt (e) and one SEM image at 5000x magnification of the surface of the shunt (f).

the emitter layer and contact the p-type base material. This will lead to a Schottky-type shunt [3]. This type of shunt will be observed only under 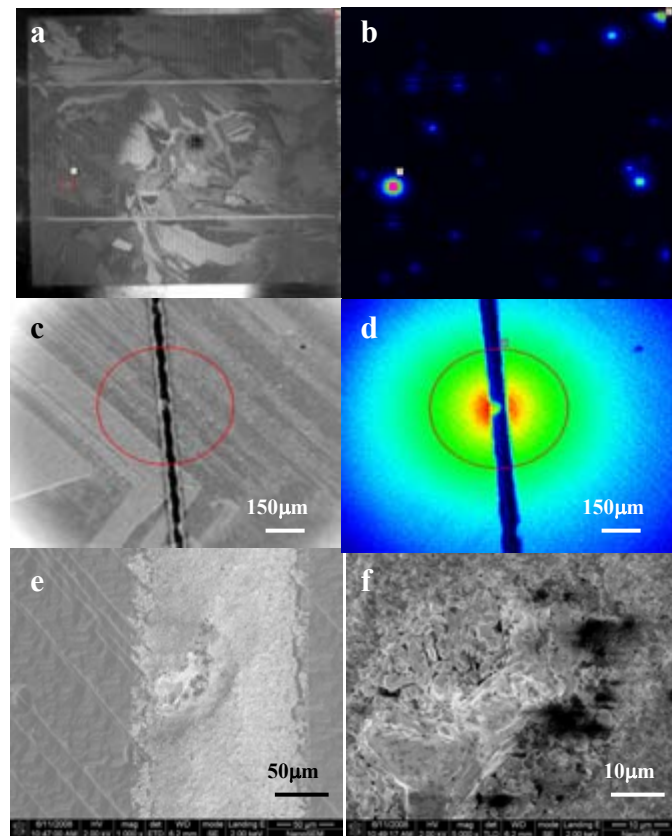metal contacts on completed solar cells. The majority of the shunts observed while investigating these CaliSolar UGM Si solar cells were located beneath gridlines and busbars. One example of this effect is shown in figure 2. This figure includes a thermal image of the entire solar cell (2a), a lock-in thermograph of the entire solar cell (2b), and two magnified images of the largest shunt (as indicated by the circle on the left side of the cell). Also, one a thermal image (2c) and one a lock-in thermograph (2d) are shown. We included two SEM images of the surface gridline at the location of the shunt. Here, one image is at 1000x magnification (2e) and the image at 5000x magnification (2f). It can be observed from the SEM images that there is a difference in the microstructure of the metal at the location of the shunt, which may be caused by a difference in the surface energy of the underlying silicon. This defect may also be caused by a localized variance in the sintering process. Further investigation will be required. In particular, an EDX chemical analysis along a cross-section of the defect would be very informative, and will be addressed in a future work.

The third defect observed in our work is an aluminum particle. Aluminum particles can be deposited onto the front surface of the solar cell through many methods of cross-contamination. The most likely cause is the stacking of pre-sintered cells. During the sintering process, the aluminum will alloy into the silicon creating a p+ -region around and beneath the particle. If this p+ -region penetrates though the emitter, it may form an ohmic contact with the base, thereby creating a shunt [3]. A 10×50μm aluminum particle was observed at the location of one of the shunts adjacent to a silicon defect in one solar cell. This shunt was investigated and can be seen in figure 3. This figure includes a thermal image of the entire solar cell (3a), a lock-in thermograph of the entire solar cell (3b), and two magnified images of the shunt (as indicated by the circle in the lower center of the cell). Also shown is a thermal image (3c) and a lock-in thermograph (3d). We included two SEM images of the surface of the aluminum particle located at the shunt. One image is shown at 2000x magnification (3e) and the other image at 5000x magnification (3f). An EDX chemical
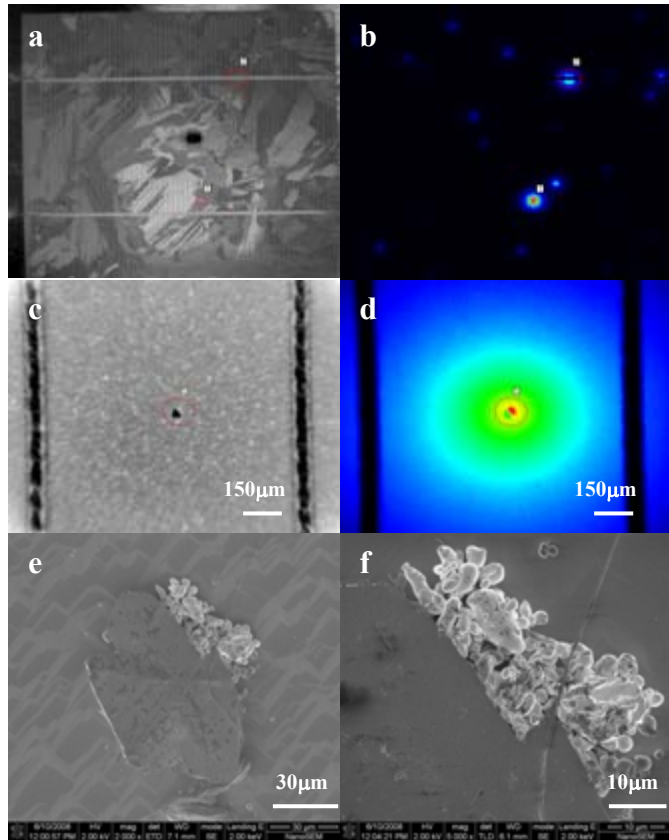

Figure 3: A thermal image of the solar cell (a), a lock-in thermograph of the solar cell (b), a magnified thermal image (c) and lock-in thermograph of the shunt located at the Al particle (d), an SEM image at 2000x magnification (e) and 5000x magnification (f) of the surface of the shunt located at the Al particle.

analysis along a cross-section of the defect to verify the depth of the Al penetration would be very informative. We plan to do this analysis in future work.

There are several other defects that can be responsible for creating shunts in silicon solar cells. As reported by Breitenstein, there are linear and nonlinear edge shunts, laser-cut holes, scratches, strongly recombinative crystal defects, macroscopic Si_3N_4 inclusions, inversion layers at precipitates, and pre-breakdown sites [3,4]. None of were believed to be responsible for creating shunts in these UMG Si solar cells from CaliSolar. However, it would be prudent to be aware of such defects while investigating shunting in solar cells.

Conclusion

Defects that are responsible for creating shunts can be better characterized through the advancement of lock-in thermography. While investigating upgraded metallurgical grade multicrystalline silicon solar cells, we have observed three defects responsible for creating shunts, which were identified in an earlier work by Breitenstein [3,4]. These defects are cracks, Schottky-type shunts, and aluminum particles. This analysis will allow solar cell manufacturers to identify the production processes that introduce these specific defects.

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Understanding the Mechanical Behavior of Multi-crystalline Si
Through Characterization of (110) / (100) DSB-HOT Wafers

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Abstract

This paper reports the effect of crystallographic orientation variation across a planner silicon 2D boundary, either a twin or a grain boundary (GB), as well as impurity (Fe and Cu) contamination of the interface on the mechanical strength and hardness as determined by nanoindentation. Further, a model 110/100 grain boundary obtained via the hybrid orientation technique (HOT) based direct-silicon-bonded (DSB) p-type Si wafers has been chosen to demonstrate the effect of Fe and Cu impurity contamination at different annealing temperatures. During increasing nanoindentation loads, Cu-contaminated GBs show a gradual decrease in hardness, whereas ~ 6% increase in hardness is characteristic to Fe-contaminated GB. Interestingly, both clean and Fe-contaminated samples displayed abrupt jump in hardness as grain boundary is perturbed by deformation volume, while Cu-contaminated samples have gradual weakening. Grain orientation also influenced the mechanical behavior of multi-crystalline Si.

1. Introduction

As PV silicon wafer thickness is reduced, wafer breakage has become a more challenging for process yield issue. From a fundamental materials science perspective, pressure-induced deformation of PV silicon enables one to understand the complex roles of crystallinity, extended defect/impurity interactions (e.g. dislocations, grain boundaries etc.), residual stresses and wafer thickness on failure mechanisms that are activated under stress. Multicrystalline Si solar wafers consist of several micro-structural factors, e.g. crystallinity, defects (dislocations, inclusions, precipitates, etc.) and their structure and interaction with impurities, etc., all of which can adversely affect the electrical and mechanical behavior of Si wafers [1-4]. Since the mechanical strength of Si is impacted by the density of mobile dislocations, immobilization or retardation of dislocation motion by the controlled introduction of N or O has been shown to improve the strength and hardness significantly [5]. Using nanoindentation, Youssef et.al. [6], observed a about 20 % variation in hardness and fracture toughness of two different grains of multi-crystalline Si in the same wafer. Recently, Youssef et. al [7] used EBSD mapping of adjacent grains and were able to quantify the effect of different grain orientation on the mechanical properties of multi-crystalline Si. These measurements were made within single or adjacent grains to reduce the impact of metallic or light element impurities. Although the effect of impurity-defect interactions on electrical properties in multicrystalline silicon has been analyzed in the past [8, 9], literature on mechanical properties is scarce due to difficulty in avoiding interactions between the above factors during nanoindentation analysis.

In this report we have examined the mechanical properties of a unique intentionally grown grain boundary (GB). The sample consists of a ~200 nm thick (110) Si layer transferred to the bulk p-type Si (100) wafer by hydrophilic wafer bonding and cleavage [10]. Note that, since the GB will act as a sink for impurity atoms and local precipitation, which can prevent or facilitate the extent

of deformation into the bulk, depending on type and concentration of impurity. Fe and Cu impurities have been chosen for current study as they are most notable lifetime killer for solar cell wafers. In addition to nanoindentation, the TEM, SIMS, SEM, µ-PCD techniques have been used to complement the mechanical property analysis.

2. Experimental

Five clean, Fe- and Cu-contaminated samples prepared by a hybrid orientation technique (HOT) based direct-silicon-bonded (DSB) p-type Si wafer. The Fe-contaminated samples were annealed at 1100°C and either immediately cooled, Sample-n1, or held in for 30 min at the annealing temperature, Sample-n3. Cu-contaminated samples

Fig. 1 – (a) Schematic demonstrating the grain boundary in HOT wafer. (b) TEM image showing oxygen-free interface between bonded (110) layer and (001) substrate.

were annealed at 400°C and 800°C. Cross-sectional TEM, see Fig. 1, revealed no interfacial oxide layer or oxide precipitates, and secondary ion mass spectroscopy, see Fig. 2, and ellipsometry measurements indicated no detectable oxygen at the bonding interface. Nanoindentations were made on all the HOT wafers (clean and contaminated) using a Hysitron TriboIndenter®. Loads were varied from 0.2 to 8 mN with loading/unloading rates of 1 mN/s. At least five measurements were made for each load in order to check reproducibility of the data.
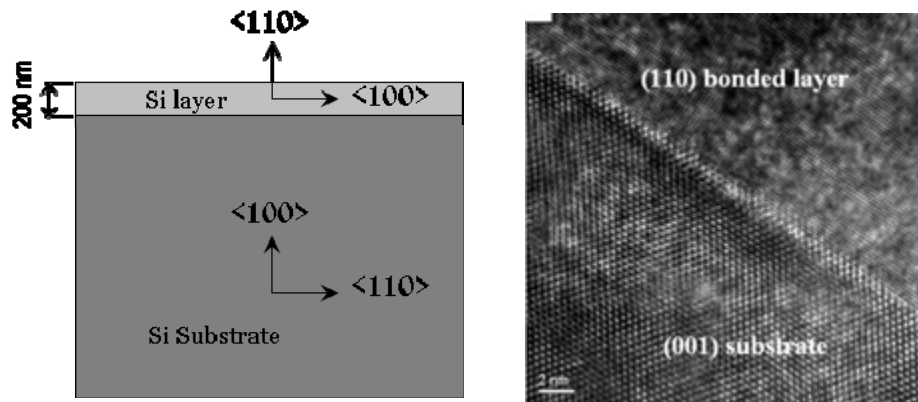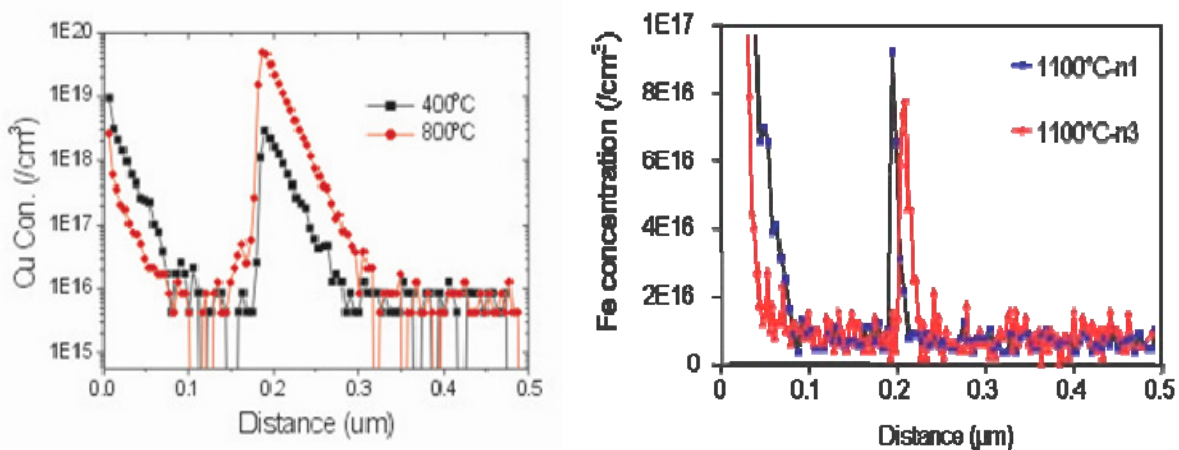

Fig. 2 SIMS data for Cu-contaminated and Fe-contaminated samples

3. Results and Discussion

Figure 3a shows the load-displacement curves for the various samples and their behavior during the loading-unloading. Note that the consistency in measurements through the overlapping of the loading and unloading curves for different indentation loads. Also the Clean sample exhibits an elbow shape during unloading, which indicates amorphous layer formation under the tip. While for Fe-Contamination the same trend exist but there is a shift in all the curves (black) to the left which suggest that the Fe-contaminated sample is stronger than the clean one. Also elbow formation is realized in all the Fe contaminated samples. The Cu-Contaminated at 800°C sample also shows a shift but to the right of the clean wafer, indicating a softer sample, which has been confirmed via the hardness data. Finally, the Cu-Contaminated at 400°C sample shows a large shift to the right which can be attributed to deterioration in the mechanical properties. Another feature called "pop-out" appears in this sample in addition to the elbow formation at high loads. This phenomenon is related to the formation of metastable Si-XII/Si-III crystalline phases [11].
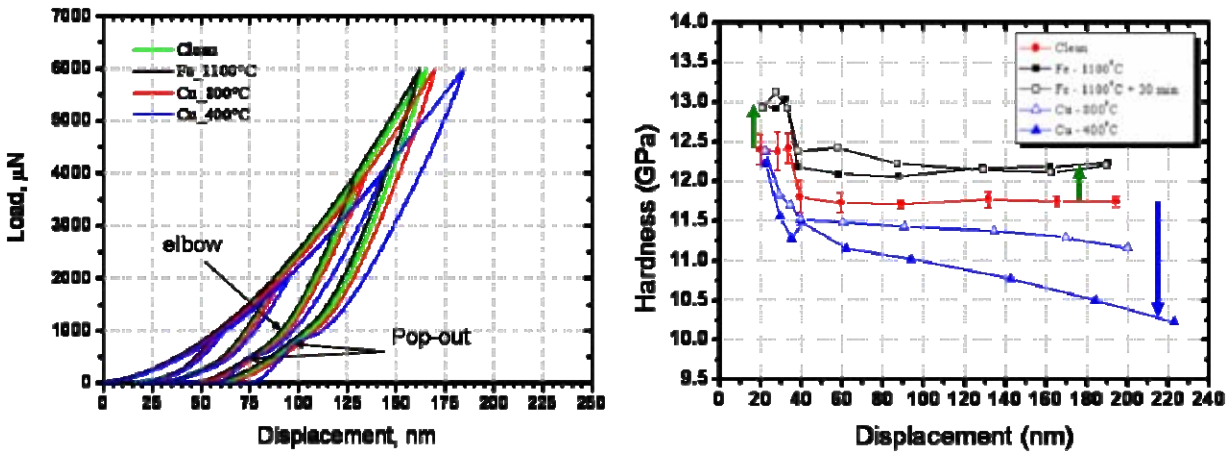

Fig. 3 – (a) Load-displacement curves for different samples (b) Hardness variation as the indenter displacement increase. Green arrows show increased hardness (5-6%) for Fe-contamination, whereas Blue arrow shows large drop in hardness for Cu-contaminated sample (400°C).

Variation in the hardness with increasing loads during nanoindentation is presented in Fig. 3(b), where all data exhibits a change at 30-40 nm as deformation volume senses the underlying boundary between the (110) and (100) orientations. Fe-contaminated samples shows a consistent increase of 6% in hardness values in both cases where deformation is present only in bonded (110) layer or extending to (100) substrate. This is likely related to segregation of Fe-impurity atoms, which may form a silicide at the grain boundary and has been confirmed by a SIMS profile, which clearly shows a 20-30 nm wide Fe concentration peak across the (110)/(100) interface, see Fig 2. Whereas, Cu forms a broader segregation profile of ~ 100 nm across GB, possibly due to the fact that Cu has a larger solid solubility and a is faster diffuser in silicon compared to Fe. At higher contamination levels, Cu with relatively lower hardness than silicon weakens Si the lattice. However, further study is necessary to analyze pressure-induced deformation behavior in HOT wafer based on the phases formed due to GB decoration, and their influence on stress-induced phase transformation.

During nanoindentation at very small loads, as the load increases the permanent displacement of the indenter increases deforming contact surface elastically. At some critical loads, maximum

shear stress (τmax) occurring at subsurface, exceeds the critical shear stress of silicon and small volume at some depth below contact region deforms plastically. Thus, to analyze a shallow ~ 200 nm deep grain boundary, smaller loads of 0.1 mN to 0.3 mN must be applied. On further increasing indentation load to a maximum of 8mN, indenter displacement gradually increased from 20 nm to 195 nm, see Fig 3b, with plastically deformed region extending to surface and beyond (110)/(100) grain boundary. Hardness on the clean wafer showed a behavior consistent with the effect of orientation and grain boundaries, see Fig. 4a. At low loads, the grain boundaries and the (100) substrate do not restrict the residual stress from the deformation zone under the nanoindentation tip. Up to 35 nm penetration depth, the first three points in the Figure 4a, the average hardness value is 12.45 GPa and represent the hardness of the (110) Si layer. With increasing the indentation load, the hardness suddenly drops ~ 6% and reaches a steady state with increasing the indentation load.

Figure 4b demonstrates the hardness vs. displacement profile based on elastic-plastic deformation of frictionless solids [12]. As load increase, initially sample deforms elastically, till critical stress is exceeded at some depth below indenter-sample contact, corresponding to the onset of plastic deformation. As load increases further plastically deformed volume enlarges. As this expanding deformation volume is influenced by the change in crystallographic orientation to less densely packed (001) substrate, hardness decreases.
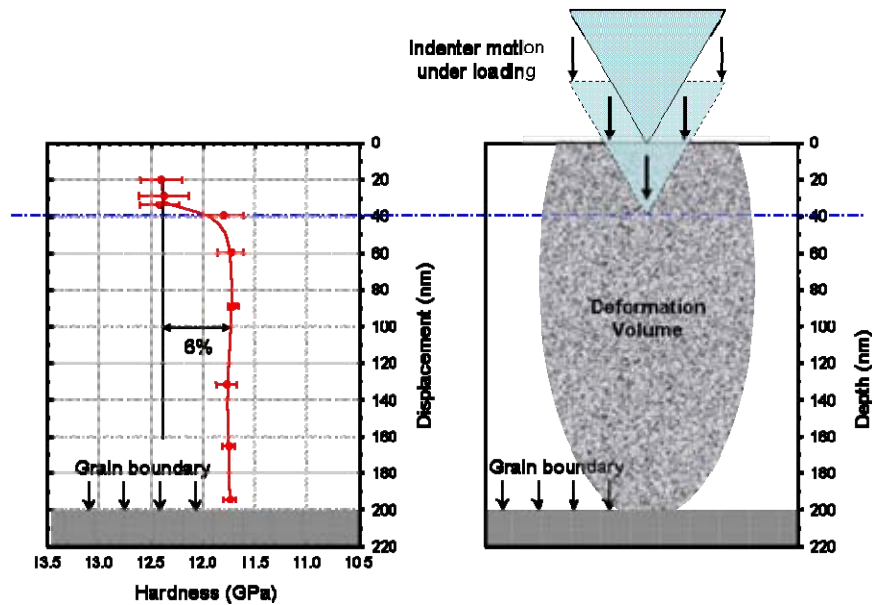
Fig. 4 – (a) Variation of the hardness as the load increases resulting in increased displacement of indenter and (b) Schematic demonstrating penetration of deformation volume upto 200 nm (GB location) while indenter displacement is ≈ 40 nm.

Conclusion

Grain orientation, grain boundary, and metallic impurities have a significant effect on the mechanical properties of Si. Fe precipitates at the grain boundary and strengthen the Si in both the (110) layer and the (110) substrate. However, Cu precipitates deteriorate the strength. The orientation (110) found to be ~ 6% stronger than that of the (100). The fundamental results

obtained in this study can be extended and used to evaluate the mechanical behavior of single crystal and multi-crystalline Si wafers with various types of impurities and orientations.

Acknowledgement

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Electrical Properties of a Metal Contaminated (110)/(100) Si Grain Boundary Prepared by Direct Silicon Bonding

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Abstract: The impact of metal contamination on the electrical properties of a "model" silicon grain boundary (GB) created by a direct silicon bonding of (110)/(100) wafers has been investigated. It is found that the metal contamination significantly change the electrical parameters of GB states, causing deeper energy levels with much larger hole capture cross-sections. Different metal contaminates produce different neutral levels at the GB, while the GB state density is dependent on the specific annealing conditions. Increasing the metal contamination at the GB by gettering at higher temperature results in a reduced density of GB states. It is believed that the electrically active metal-related states present at the GB interface are generated by localized metal precipitates, whereas a higher temperature annealing with quench cooling produces a lower density of large precipitates at the GB. This explains the apparent anomalous behavior of GB state density depending on the annealing temperature in metal contaminated samples.

1. Introduction

Grain boundaries (GB) in silicon are known to introduce electronic states in the forbidden gap. These states can arise from intrinsic structural defects such as dangling and distorted bonds, as well as the presence of segregated impurities. The interaction of metal impurities with silicon GBs has been extensively studied because of its importance for multi-crystalline silicon PV devices. It has been previously reported that metal contamination can cause the GB to behave like a double Schottky barrier [1]. Meanwhile, the interface of a metal-precipitate/matrix has been known to induce electronic states in the band gap [2]. However, specific mechanisms describing how metal contamination at a GB affects its electrical characteristics, such as density of states, carrier capture cross-section and the GB neutral level, are not yet well understood. In this report, we have intentionally introduced iron and copper impurities into a "model" large-angle GB created by the direct silicon bonding of two (110)/(100) wafers. A set of experimental data has been obtained using a charge transient method, which will enhance our understanding and present options to control the detrimental effects of metal contamination on the multicrystalline silicon used for solar cell.

2. Experiment

The starting wafer was p-type hydrogen implanted (110) silicon and (100) wafer which was directly bonded to a (100) substrate and cleaved to create a large angle

(110)/(100) GB positioned 200nm below the (110) surface. Both wafers had boron concentrations of $\sim 1 \times 10^{15}$/cm^3. The samples were contaminated by immersion in iron and copper nitric acid solutions, respectively. Fe was then gettered by the GB by a 910°C/1h+ 700°C/2h annealing in an Ar ambient, while Cu received a 600 °C - 950°C/30mins annealing followed by quench cooling. For electrical characterization, after Piranha cleaning (H_2SO_4:H_2O_2=1:1 in volume) to remove the surface contamination, Al Schottky diodes or Au ohmic contacts were prepared on the thin (110) upper layer, while an ohmic contact was formed by rubbing an InGa eutectic solution on the backside. A Bio-Rad DL8000 deep-level transient spectroscopy (DLTS) system was used to perform zero bias, 1 MHz capacitance transient measurements on different GBs following application of bias pulses.

3. Results and discussion

When applying a bias voltage across the GB, the energy band bending near the GB will be changed and certain empty GB states with energies below the zero bias Fermi level moves above the Fermi level, capturing holes to reach a new steady-state equilibrium [3]. According to charge emission theory, the charge decay rate (dN_{ss}/dt) due to hole emission at one energy level (E_T) with a state density of (N_T) can be expressed by:

$$\frac{dN_{ss}}{dt} = N_T e_p = N_T \gamma \sigma_p T^2 \exp\left(-\frac{E_T}{kT}\right) \qquad (1)$$

where e_p is the hole emission rate, γ is a constant, σ_p is the hole capture cross-section, T is the absolute temperature and k the Boltzmann constant. During the hole emission process, two mechanisms are distinguished [3]; for band-like GB states, the energy level (E_T) actually represents the highest charged states with an energy position near the time-dependent quasi-Fermi level at the GB, whereas for localized GB states [3], the level (E_T) represents a mean energy value of those states in a narrow energy range due to the hole emission rate depending sharply on the energy position. Figure 1 shows the charge decay rate due to hole emission from the clean GB as a function of charge density at different temperatures after applying a 20V pulse bias with a 200 ms width. According to Eq. (1), the GB state density (N_T) can be obtained by the slope of the linear function ln(dN$_{ss}$/dt) ~ N$_{ss}$. The energy level (E_T) and corresponding hole capture cross-section can be determined by making an Arrhenius plot according to Eq. (1), as shown in Fig. 2 for the clean GB at a charge density of 2.5×10^{12}/cm^2.

Our experiment results has clarified that the GB states in clean sample is localized, while the GB states in metal contaminated sample is bandlike. This indicates that the nature of the GB states related to metals is completely different from that of clean GB states. Table 1 lists the electrical parameters of GB states at the clean, iron- and copper-contaminated GBs. These results indicate that metal contamination can significantly change the electrical characteristics of a GB; these include the density of GB states and corresponding hole capture cross-section, the GB neutral level, the equilibrium Fermi level, and the built-in GB barrier at zero bias. Since the metal impurities often exist as

precipitates at the GB after annealing [4], it is believed that the new metal-related states are generated at a localized metal-precipitate/silicon-matrix interface, which can dominate the electrical properties of metal-contaminated GB [4]. Compared with copper contamination, the iron contamination produces a higher state density at the GB than copper, while the energy distribution of states is relatively shallower.
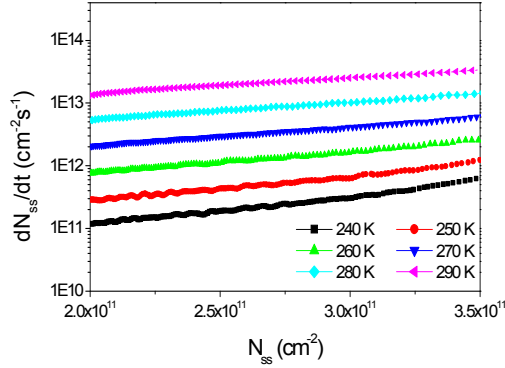

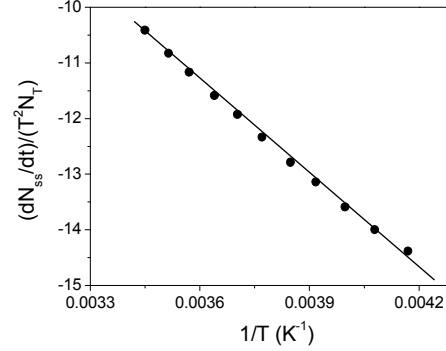Fig. 1 The charge decay rate as a function of charge density at different temperatures for the clean GB.

Fig. 2 The Arrhenius plot at a charge density of $2.5\times10^{11}/cm^2$ for the clean GB

Table 1 The electrical parameters of GB states at the clean GB, iron- and copper-contaminated GB subjected to 600°C annealing

	Clean GB	Fe-contam. GB	Cu-contam. GB (600°C)
State density $(cm^{-2}eV^{-1})$	5.8E12	2E13	7.4E12
Hole capture cross-section (cm^2)	~1E-17	~2E-15	~1E-15
Neutral level (eV)	E_v+0.52	E_v+0.59	E_v+0.63
Equil. Fermi level (eV)	E_v+0.49	E_v+0.58	E_v+0.60
Built-in barrier (eV)	0.24	0.31	0.35

Next we present the electrical characteristics of GBs with different levels of metal contamination. Figure 3 shows the SIMS determined copper concentration at the GBs in various Cu-contaminated sample, which increases with annealing temperature. The results show, see Fig. 4, that the state density at the copper-contaminated GBs decreases from 7.38E12 to 2.45E12 $cm^{-2}eV^{-1}$ as the annealing temperature increases from 600°C to 950°C. For a GB charge density of 2.5E12/cm^2, the corresponding energy levels are found to decrease with increasing annealing temperature, from E_v+0.59 eV to E_v+0.52 eV, while the hole capture cross-sections increase from $1\times10^{-15}cm^2$ to $5.4\times10^{-15}cm^2$. The neutral levels at all the copper-contaminated GBs remain essentially constant at about E_v+0.63eV suggesting that the metal induced donor-like and acceptor-like states will always exhibit the same energy distribution at the GBs, independent of annealing temperature. Consequently, the equilibrium Fermi levels at the GBs under zero bias decrease with annealing temperature from E_v+0.60eV to E_v+0.55eV. Therefore, the equilibrium built-in GB barrier at zero bias decrease from 0.35 eV to 0.3 eV as the annealing temperatures increase from 600°C to 950°C.

In order to fully understand the impact of metal contamination on the electrical properties of a GB, it is necessary to know the distribution of metal precipitates at a given GB subjected to different annealing temperatures. The concentration of incorporated copper at the GB increases with the annealing temperature increasing. During following cooling, metal precipitates start to homogenously nucleate at a critical temperature, which is determined by the copper super-saturation [5]. The critical temperature to initiate metal impurity precipitation is higher for the GB with copper incorporation by higher temperature annealing, resulting in a reduced density of larger size copper precipitates at the GB, due to faster diffusion of metal. Since the copper-related GB states are attributed to the precipitate/matrix interface [4], a higher temperature annealing will introduce a lower density of copper-related interface states, due to a reduced density of larger size GB precipitates.
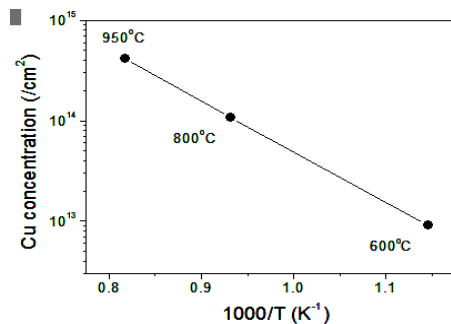

Fig. 3 The copper concentration at the GBs subjected to different temperature annealing
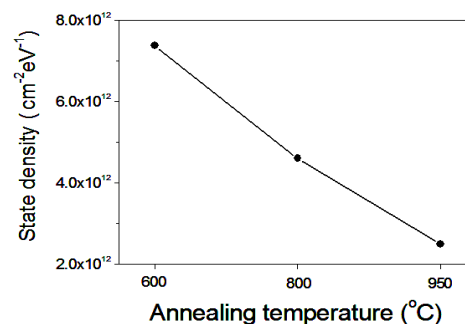
Fig. 4 The state density at the Cu-contaminated GBs subjected to different temperature annealing

4. Conclusion

Our results demonstrate that metal contamination at a GB will significantly change the electrical characteristics of the as prepared wafer GB states. The originally localized GB states have been found to transform into band-like states with much large hole capture cross-sections after metal contamination, while the neutral level at a metal-contaminated GB is much deeper than that at the uncontaminated GB. A higher temperature annealing followed by quench cooling will generate a reduced density of larger copper precipitate sizes at the copper contaminated GB with a correspondently smaller GB state density. This ultimately has the benefit of producing a smaller built-in GB barrier at the copper contaminated GBs, which alleviates the detrimental effect of GBs on the electrical properties of multicrystalline silicon solar cell.

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Analysis of Stresses and Wafer Breakage During Handling and Transport

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Abstract
A significant challenge in using thinner and larger crystalline silicon wafers for solar cell manufacture is the reduced yield due to increased wafer breakage. At a given process step, wafer/cell breakage depends on the nature and distribution of stresses produced in the wafer/cell due to processing, handling and/or transport and on the presence of defects such as cracks. This paper presents an analysis of the failure stress (i.e. breakage stress) in thin multi-crystalline silicon wafer handling using a Bernoulli gripper. An approach to determine the failure stress from measured wafer deformation, breakage experiments carried out on cracked wafers, and non-linear finite element (FE) analysis is presented. The results show that the failure stress is proportional to the inverse of the square root of the crack length, which is consistent with linear elastic fracture mechanics. The work also validates the capability of predicting wafer breakage during handling using the total stress state if the crack size, location and fracture toughness are known a priori.

1. Introduction

Increasing cost of silicon (Si) combined with the need to lower the cost of solar cells has contributed to the growing use of thinner and larger crystalline silicon wafers. However, studies have shown that the use of thinner wafers can lead to unacceptable yields arising from wafer breakage during handling, transport and/or processing [1]. Consequently, it is critical to understand the causes of wafer breakage [2]. Fundamentally, due to the brittle nature of silicon at room temperature, breakage of Si wafers is due to the propagation of cracks present in the wafer during a processing or handling step in solar cell manufacture. Knowledge of crack locations and sizes is therefore required to predict wafer breakage accurately. Several techniques have been developed to detect and quantify cracks in wafers [3-5]. A crack will propagate if a sufficiently large in-plane tensile stress is applied orthogonal to it (assuming Mode I fracture). In [6] a non-linear finite element analysis method was used to evaluate the nature, magnitude and distribution of the total stress state (including residual stresses) produced in crystalline silicon wafers due to handling by a Bernoulli gripper..

The focus of this paper is to establish and validate an approach for determining the failure stress for Si wafer breakage during automated handling using Bernoulli grippers. Specifically, breakage experiments are carried out on cracked EFG Si wafers. The failure stress is calculated from the measured wafer deformation. The relationship between failure stress and crack size is then analyzed and compared with results from standard linear elastic fracture mechanics theory.

2. Wafer handling

In a handling operation, the applied stress is a function of the handling control variables. Bernoulli based wafer handling methods are commonly used in the PV industry. In these devices, a suction force is created between the gripper and wafer by a radially diverging decelerating air flow. Bernoulli gripper design often consists of soft rubber pads that determine the stand-off distance. Friction between the wafer and pads enables faster transport speeds. Neglecting the dynamic effects of robot motion, the applied stresses are a function of the volumetric air flow rate and the stand-off distance imposed by the pads [6].

3. Approach

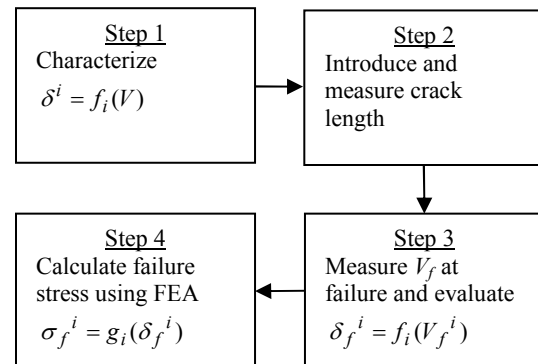The approach used for determining the failure stress due to Bernoulli gripping is illustrated in Fig. 1.

Fig. 1. Flowchart of the approach.

The first step in the approach consists of experimentally characterizing the influence of the volumetric air flow rate (V) on the actual wafer deformation, δ. Equation (1) describes this influence for every wafer i and is established empirically here. As a result, the influence of pre-existing residual stresses in the wafer is automatically accounted for.

$$\delta^i(x,y) = f_i(V) \tag{1}$$

As discussed in [6], for a given air flow rate, the function f_i can be represented by a fourth order polynomial regression model with two predictor variables x and y, which are the coordinates of a point on the wafer surface.

The second step consists of introducing a crack in the Si wafers using an indentation method. Although EFG wafers are multi-crystalline wafers, they are known to have a predominant grain orientation due to the crystal growth process. Specifically, EFG wafers are characterized by a {110} surface and a <112> growth direction [7]. A Knoop indenter is used to generate a small notch on the wafer edge and initiate a straight through-thickness crack along the growth direction. Figure 2 schematically illustrates the location and orientation of the crack generated in the wafer. The crack length, l, is measured using an optical microscope yielding a typical result shown in Fig. 3. The notch size being much smaller than the crack length, its influence on the failure of the wafer is neglected. The specific crack orientation was chosen to create {111} cleavage planes thus avoiding transgranular fracture of the wafer.
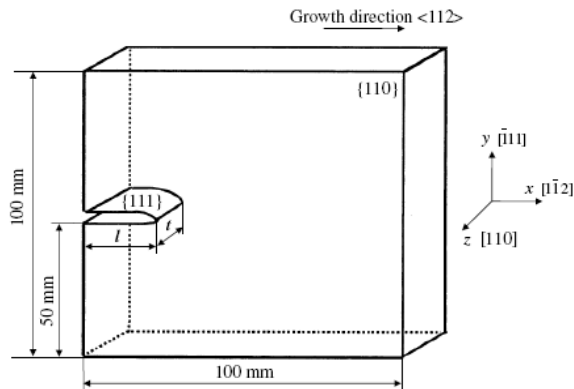
Fig. 2. Schematic of the through-thickness crack in EFG wafer.

Fig. 3. Optical microscope picture of 0.62 mm through-thickness crack (sample #2).
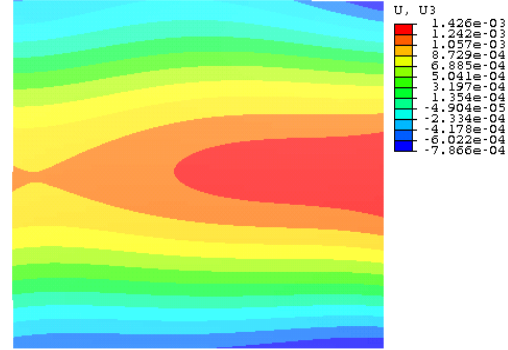
Fig. 4. Wafer deformation profile at failure calculated using Eq. 3 (sample #2).

Breakage experiments are then carried out using the Bernoulli gripper where it is important to keep the same wafer orientation as in the first step due to the non-symmetry of the wafer deformation profile. The volumetric air flow rate is increased slowly at a rate of 0.2 L/min till breakage occurs. Using Eq. (1) and the air flow rate at failure, V_f, the wafer deformation profile at failure is obtained as follows:

$$\delta_f{}^i(x,y) = f_i(x,y,V_f) \tag{2}$$

Figure 4 shows the wafer deformation profile at failure, which is seen to be not perfectly symmetric due to the wafer thickness variation perpendicular to the growth direction. The wafer thickness is observed to be thicker at the edges.
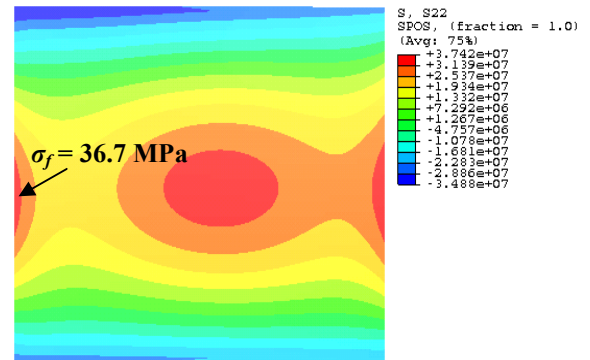
Fig. 5. σ_{yy} stress distribution on the wafer surface; the failure stress at the crack location is specified (sample #2).

Finally, the total stress state at failure is obtained using the wafer deformation at failure (Eq. 3) as input to a non-linear finite element model [6]. In this work, the anisotropic properties of the EFG wafer were specified using the compliance matrix defined in the proper coordinate system (x, y, z). The stiffness coefficients are obtained from the known stiffness coefficients for single cubic Si crystal with respect to the crystal coordinate system (x', y', z') [8]. Stiffness is specified using the (110) single crystal properties taking $[1\bar{1}2]$, $[\bar{1}11]$ and $[110]$ orientations as the x', y' and z' axes. The elastic stiffness matrix is given by:

$$C_{ijkl} = \begin{pmatrix} 203.85 & 44.83 & 44.83 & 0 & 0 & 0 \\ & 194.30 & 54.38 & -13.51 & 0 & 0 \\ & & 194.30 & 13.51 & 0 & 0 \\ & & & 60.40 & 0 & 0 \\ & & & & 60.40 & 13.51 \\ sym & & & & & 69.96 \end{pmatrix}$$

$$(3)$$

From linear elastic fracture mechanics theory, if a crack is located in an area of tensile stress, its propagation will depend on the following factors: magnitude of tensile stress perpendicular to the crack plane, crack geometry (size and shape), and fracture toughness K_{IC} of the material (assuming mode I fracture is predominant). Figure 5 shows the stress distribution perpendicular to the crack plane on the top surface of the wafer obtained from the FE model. The tensile stress at the notch indent location was extracted from the FE result and used as the failure stress. The resulting failure stress is denoted as follows:

$$\sigma_f^i = g_i(\delta_f^i) \tag{4}$$

4. Results and Discussion

Experiments were carried out on as-received 100mm x 100mm EFG wafers selected from the same batch. The wafers were etched by the supplier to remove surface damage from laser cutting operations. The experimental setup used in the tests is described elsewhere [6]. In the present work, the stand-off distance between the Bernoulli gripper and the wafer was fixed at 2 mm. Before introducing a crack, the volumetric air flow rate was varied from 27.5 to 40 liters/min and the wafer deformation profiles were measured.

Table 1 summarizes the experimental results. The wafer thickness, t, the crack size l, the volumetric air flow rate, V_f, and the failure stress, σ_f, are listed for every wafer. Preliminary analysis of the FE results

showed that the wafer thickness had a significant effect on the failure stress calculation. Hence, the thickness variation close to the crack location on the cleavage plane was measured after wafer failure and found to exhibit a total thickness variation (TTV) of ±9% along the wafer growth direction on the cleavage plane. The effect of this variation was accounted for in the failure stress calculation. The observed thickness variation is related to the control of the pulling rate during the growth process for EFG wafers.

Table 1. Calculated failure stress for EFG wafers

Wafer	t			l	V_f	σ_f
(#)	(μm)			(mm)	(L/min)	(Mpa)
1	158	±	14	0.26	34.3	45.2
2	155	±	14	0.62	35.5	36.7
3	129	±	12	1.15	31.4	15.8
4	115	±	10	1.77	34.3	17.8
5	137	±	12	2.37	31.8	13.0
6	142	±	13	2.56	30.1	7.6
7	141	±	13	3.13	32.1	10.4
8	156	±	14	6.22	30.6	6.9

From linear elastic fracture mechanics theory, the stress intensity factor for an edge crack of length, l, under a far field tensile stress, σ_∞, is given by [9]:

$$K_I = Y\sigma_\infty\sqrt{\pi l} \tag{5}$$

where Y is the shape factor for an edge crack in a specimen with finite width, w, and is computed as:

$$Y = 1.122 - 0.231\left(\frac{l}{w}\right) + 10.550\left(\frac{l}{w}\right)^2$$
$$- 21.710\left(\frac{l}{w}\right)^3 + 30.382\left(\frac{l}{w}\right)^4 \tag{6}$$

The crack will propagate when the stress intensity factor K_I reaches a critical value K_{IC}. In Fig. 6, the calculated failure stress obtained from Eq. (4) is plotted as a function of the crack length (labeled as "Experiment" in the figure). The figure also contains a plot of the theoretical failure stress determined from Eqs. (5)-(6) for two values of fracture toughness of silicon along the {111} cleavage plane reported in the literature [10-11]. The calculated failure stress values are seen to be in good agreement with the theoretical values. Although some scatter is evident in the calculated failure stress values, most of them fall within the range of the theoretical values. When plotting the failure stress as a function of the inverse square root of the crack length as shown in Fig. 7, a strong proportional relationship is found thereby validating the mode I failure assumption and more

importantly the failure stress calculation using the FE analysis.
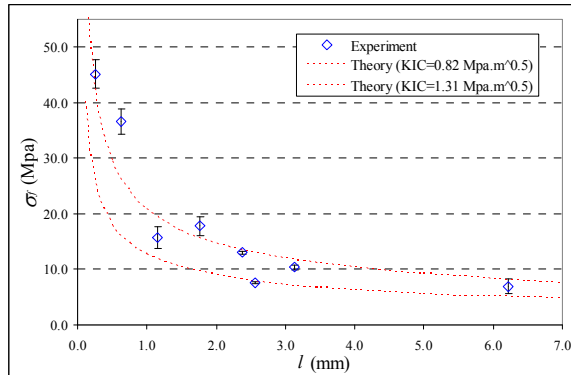
Fig. 6. Experimental and theoretical failure stresses as a function of the crack length
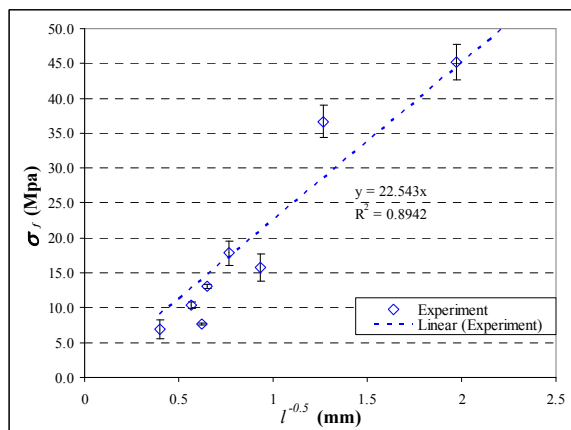
Fig. 7. Experimentally determined failure stress as a function of the (crack length)$^{(-1/2)}$.

Conclusions

This paper presented an approach for determining the failure stress for breakage of crystalline Si PV wafers during automated handling. Although the focus was on Bernoulli gripping, the approach is generic and can be applied to other wafer handling devices. The results show that the proposed approach based on using the total in-plane stress produced in the wafer during handling yields failure stress values that are consistent with linear elastic fracture mechanics theory. The experimental results also show that the failure stress calculated from the approach is proportional to the inverse square root of the crack length as expected from linear elastic fracture mechanics, hence validating the stress calculation. This work confirms the capability of predicting wafer breakage during handling using the total stress state provided the crack size, location and fracture toughness are known a priori.

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A COMPARISON OF TRANSIENT AND IMAGING TECHNIQUES FOR MEASURING MINORITY-CARRIER LIFETIME

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ABSTRACT

This paper serves as a comparison between several single point lifetime measurement techniques and lifetime imaging techniques. The single point methods include: Microwave Reflection Photoconductive Decay (uPCD), Resonant Coupled Photoconductive Decay (RCPCD), Free Carrier Absorption (FCA), and Quasi-Steady-State Photoconductive Decay (QSSPCD). The imaging methods are Free Carrier Absorption and Photo-luminescence (PL), which will also be compared to uPCD mapping.

INTRODUCTION

The minority carrier lifetime is an important parameter for semiconductor solar cell materials. Measured lifetime values are inherently dependent on the defect and impurity densities present in the material. The lifetime can be measured through transients or quasi steady-state methods that give a direct value for lifetime, or through imaging techniques. The latter generally is much faster and has higher resolution, but does not yield quantitative lifetimes. Injection level dependencies of the recombination rates further characterize the material and possibly provide information for the identification of specific impurities. Injection level dependent measurements are also applicable when measuring lifetime with respect to the material-doping level or the device-operating level, such as 1-sun intensity for typical solar cells. The technique for measuring injection-level dependent lifetime therefore needs to have linear response and high sensitivity for measuring over large ranges of excited excess-carrier density.

Lifetime may be measured using contactless, transient photoconductive decay techniques such as microwave reflection photoconductive decay (μPCD), resonant-coupled photoconductive decay (RCPCD), or quasi-steady-state photoconductive decay (QSSPCD). These are single point transient techniques, but it is possible to raster a sample with these measurements to make a lifetime map, though it is often a time consuming process. For μPCD (few to tens of GHz frequencies), the sample is coupled to the end of a microwave waveguide or antenna structure, and changes in reflected microwave power are sensed as short light pulses generate photoconductivity [1-6]. RCPCD (~400 MHz) senses coupled impedance between the sample and a small coil, or other antenna structure [7-9]. For μPCD, the sample is impedance matched to the waveguide by using an E and H plane tuner [3]. For RCPCD, the antenna with coupled sample can be impedance matched by adjusting a variable capacitor, frequency, and/or mutual coupling to the sample [9]. For each case, impedance matching is performed without a pulsed light source creating excess carriers, and the circuit's zero signal, or null, corresponds to no reflected power from the sample. For each pulse, changes in sample conductivity disrupt the impedance-matched circuit balance, resulting in reflected power that is detected and recorded using an oscilloscope. QSSPCD is very similar to RCPCD, however the injecting light pulse is as long or longer than the lifetime. By subtracting out the pulse decay from electrical response a lifetime can be found while the device is still in partially excited state. Unlike the other PCD measurements, this one does not look at just the excess carrier lifetime and has been claimed to be a truer measurement of lifetime [12].

Lifetime can also be probed by free carrier absorption (FCA) in the material. In this method the sample is pumped in the same way as in the PCD methods, but instead of probing conductivity the carrier concentration is probed directly. The principle is in the mid to far IR the opacity of the semiconductor increases linearly with the carrier concentration. In the case of a transient measurement a decay curve is measured in the transmission of an IR laser through the sample after an excitation pulse [10-11]. For imaging techniques a black body heat source is placed behind the sample and it's change in transmission when an exiting source is switched on and off is imaged onto an IR camera [13].

Photoluminescence is used often for lifetime imaging and can also create high-resolution profiles of a wafers lifetime in seconds. Though Silicon and other common solar cell materials are indirect bandgaps, they still have a small amount of radiative recombination that is proportional to the rate of recombination, which can be proportional to the lifetime [14-15].

EXPERIMENTAL SETUP

For the RCPCD technique we have a small coil antenna as our coupling source, which is tuned to resonance with a variable capacitor and slight

modifications to the frequency, which is at roughly 400 MHz. A directional splitter or circulator is then used to find the difference in reflected power from the coil as the samples conductivity is changed. The theory and setup is described in greater detail in previous work [16].
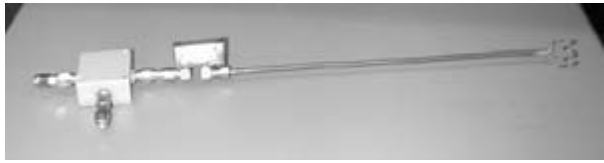

Figure 1. Small loop, capacitor, and splitter for RCPCD.

The setup for our single uPCD measurements was done with a simple 20GHz waveguide that was brought up against the sample with E and H tuners to match the impedance of the wafer to the guide. The guide is excited by a 20GHz diode and the reflected power goes through a circulator and is sent to a detector. The change in the reflected power is then measured directly and recorded on an oscilloscope. The mapping was done with an industrial Semilab Tool, but the principle of reflected power is the same.
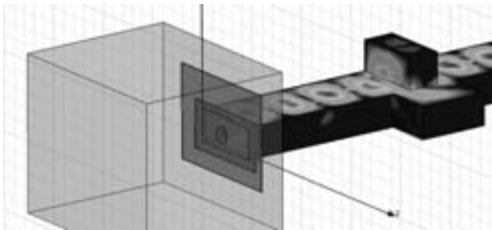

Figure 2. HFSS model of uPCD waveguide and sample.

For the transient setup of free carrier absorption we used a pulsed laser at 1064nm to create the carrier injection and then probed the change in absorption with a 3.4um CW HeNe laser in a pump-probe alignment. The probe beam intensity is measured by a InSb detector after going through the wafer and also beforehand to cancel out any laser noise. The noise-canceled signal is then read on an oscilloscope similar to all the other transient methods. In the case of imaging FCA, we use a 810nm fiber–coupled diode array with a diffuser as the pump source and a hot plate with an emissivity coating as the probe source. The heat transmission through the sample is then imaged onto an IR camera and the change in transmission is generated from a lock-in amplifier.

Figure 3. FCA imaging setup

The photoluminescence imaging setup is similar to the FCA setup. The major difference is there is no need for a hotplate and a different IR camera is needed closer

to the bandgap of silicon. This means that the 810nm light source can create noise in the measurement making a notch filter for the 810nm wavelength, along with a RG1000 IR Schott glass filter, useful to increase sensitivity.

TRANSIENT COMPARISONS

In this section the transient and QSSPCD techniques will be compared at various carrier injection levels on the same spot of a single crystalline silicon wafer.

For uPCD it can be seen below that the lifetime does get shorter at higher injections by roughly a factor of ten percent. At large injection the curve begins to level out though as the reflected power is saturated in this method. At very high injections the curve can be seen to flatten out completely until the carrier concentration drops below the detectable threshold [16].
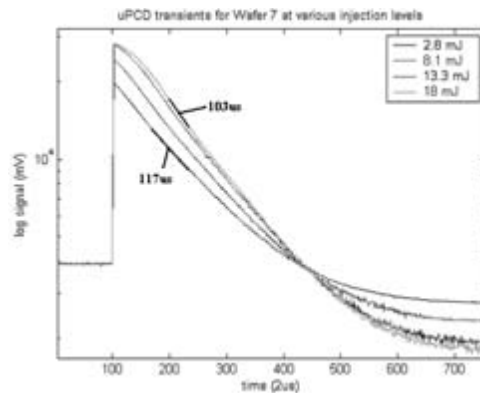

Figure 4. Carrier decay transient using uPCD at various injection levels in log scale.

The next method compared is the RCPCD technique, since it is a photoconductive decay method as well. Compared to uPCD the lifetime reading is much more stable, though the RCPCD laser could not get to the same injection levels that the uPCD system attained. The lifetime remained the same within a couple of microseconds. The signal isn't as strong as in the uPCD measurement, but its range can be tuned to still give readings at high injection and not saturate.
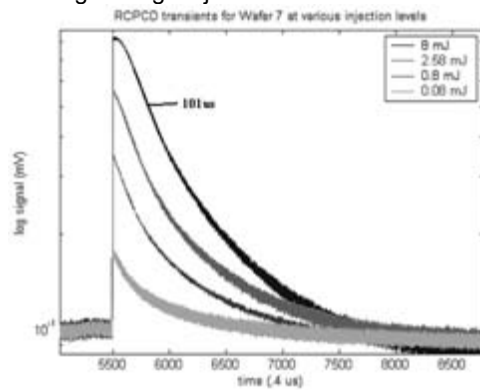

Figure 5. Carrier decay transient using RCPCD at various injection levels in log scale.

The last transient technique compared is the FCA method. As can be seen below this is the noisiest of the techniques and also has the largest difference in lifetime at different injection levels. However, it also yields the most linear response and is a direct measurement of free carriers in the sample.
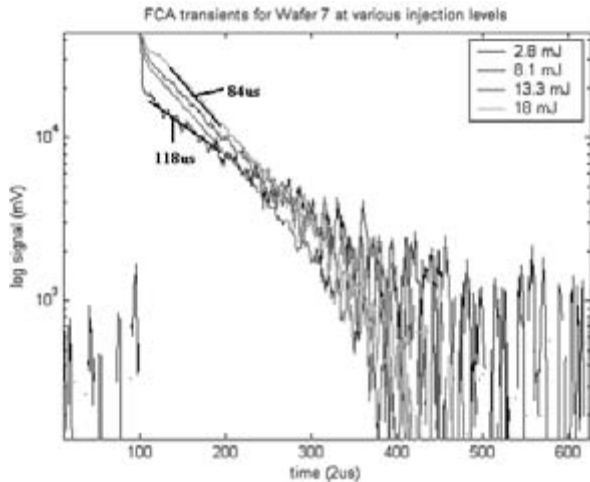

Figure 6. Carrier decay transient using FCA at various injection levels in log scale.

The last single point lifetime measurement is the QSSPCD. At high injections it displays a lifetime of roughly 100us and compares nicely to the other techniques. At low injection it can reach as high as 180us. A probable reason for this large lifetime is that the spot size of our Sinton Apparatus is large compared to the other techniques, and the sample measured has lifetime variations from 40 to 300us. If the device also detected a longer lifetime region, it would become dominant for the low injection readings, while the shorter lifetimes would be dominant at higher injection.
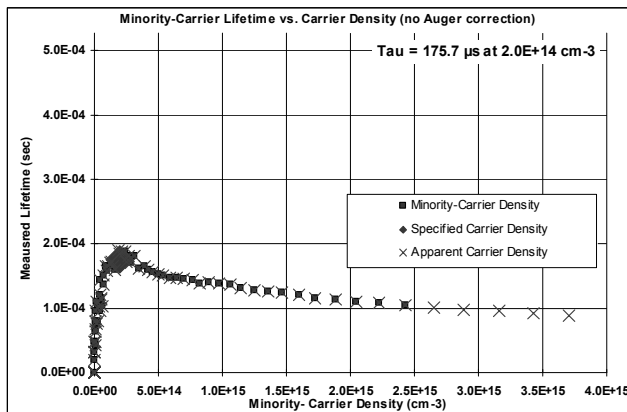

Figure 7. Plot of lifetime vs. carrier concentration using QSSPCD on a Sinton Apparatus.

IMAGE COMPARISON

In this section FCA and PL imaging will be compared to each other and then to uPCD mapping run on a Semi-lab Tool. The purpose of the uPCD map is to see how well the imaging techniques match the transient measurements and to what accuracy they can be calibrated to show real lifetimes.

Below are three lifetime maps of the same area a single crystalline silicon wafer with scratches and iron contamination. On the left is the Semilab uPCD measurement, the middle is the FCA image, and the right is the PL image. For both the images the units are arbitrary with the color red for long lifetimes and blue for short. From a qualitative comparison it seems that all the images match very well except the lower portion of the PL image (right image on Fig. 8). This is caused from the uneven illumination of the sample in our current setup due to the light being incident at an angle.
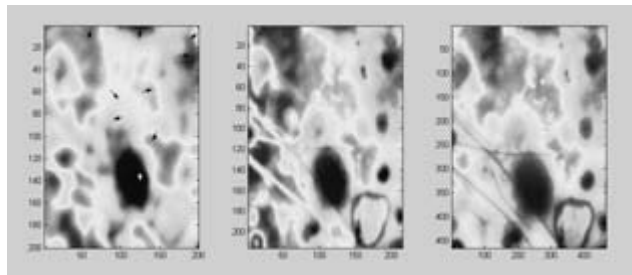

Figure 8. (left) uPCD lifetime map (center) FCA lifetime image (right) PL lifetime image

The next two plots are a quantitative comparison of FCA and PL vs uPCD with points indicated by the arrows in the uPCD map above.
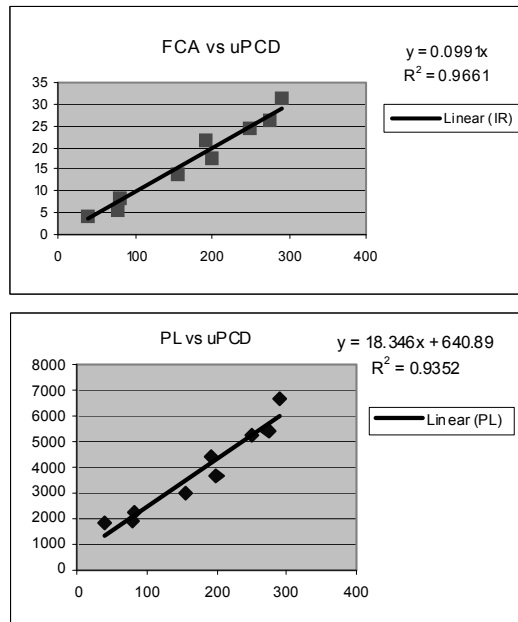

Figure 9. Quantitative comparison of imaging methods to uPCD at various locations on the sample.

From the comparison of each image to the uPCD map it is possible to then create a calibration constant to transform qualitative images to quantitative lifetimes, making it possible to have high-resolution images of actual lifetime.
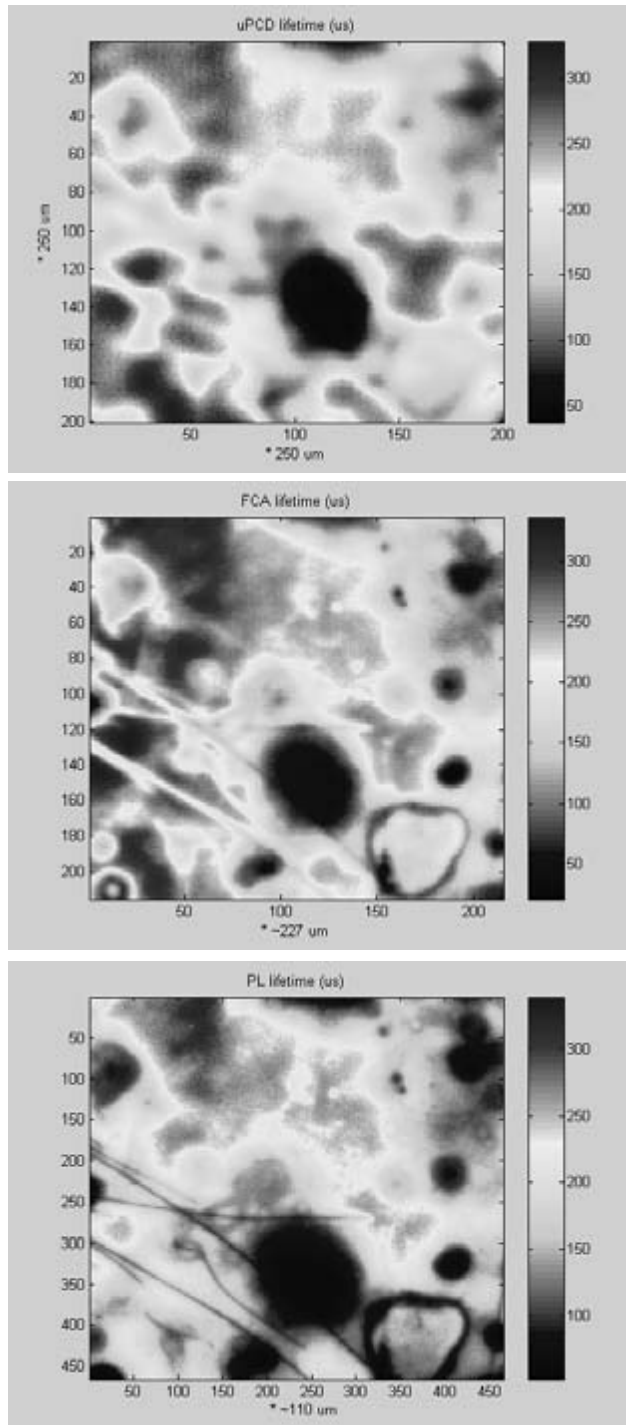

Figure 10. Calibrated lifetime images for (top) uPCD (center) FCA, and (bottom) PL

SUMMARY

We have compared uPCD, RCPCD, and FCA transient techniques at various injection levels as well as QSSPCD. A comparison of PL and FCA imaging was also shown along with a quantitative uPCD map to calibrate the image lifetime values. All the imaging and transient techniques seemed to agree with each other, though they each had different margins of error, sensitivity, and resolution.

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Defect Incorporation and Impurity Precipitation in Mono[2] Silicon

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Introduction

Monocrystalline silicon substrates make higher efficiency solar cells than their multicrystalline counterparts due to their lower density of trapping defects and because their surface can be readily textured to reduce light reflectance. Unfortunately, the most common technique of single crystal growth, the Czochralski (CZ) method, is expensive to implement and produces round wafers which must be cut to fit onto square panels. BP Solar has successfully produced monocrystalline silicon, named Mono[2] using casting techniques as described in reference 1. This material provides a unique crystal growth system for photovoltaics in that it has the quality of being single crystalline, as with CZ material, but shares impurity distributions with multicrystalline cast material. The experiments described in this report show the similarities between the single crystal growth methods and the effects impurities can have on such a growth system.

Experimental

A vertical slice from a Mono[2] ingot which extended from the bottom of the ingot to the top was selected for analysis. The slice was taken from a brick that was in contact with the crucible sidewall and this edge was removed from the sample. The original sample was 2 mm thick, 12 cm wide, and 25 cm tall and was cleaved into pieces convenient for measurement. A microwave photoconductance decay (MW-PCD) minority carrier lifetime map of the entire uncleaved slice was taken using a Semilab WS2000 with the sample surface under iodine/methanol passivation. Pieces were selected for defect delineation etching based on variations in the lifetime map. These pieces were polished and etched in s Secco solution for varying times. The etched pieces were then examined using optical microscopy. Some features of interest were examined using a Hitachi S3200 SEM equipped with an Oxford Isis Energy Dispersive Spectroscopy (EDS) system.

Results and Discussion

A section of the MW-PCD lifetime map is shown in Fig. 1 and shows a region of low lifetime at the base of the ingot that is 5 cm tall. Transitions in lifetime occur within this region and are labeled A, B, C, and D. At the base of the ingot is a thin band of very low lifetime. Just above this band, a transition occurs to a slightly higher lifetime, labeled by A. At an elevation of about 1 cm, this higher lifetime then abruptly transitions back to low lifetime and is labeled B. At an elevation of 5 cm, labeled C, the lifetime transitions from low to high over a distance of 1 cm. Labeled D, the high lifetime region then extends to the top of the ingot.

Samples were examined by defect delineation etching at each of the points shown in Figure 1 and the results are shown in Fig. 2. The transition at A is a flat boundary parallel to the ingot base with large voids along its length. The lower material is melted and solidified silicon while the upper material is annealed silicon. The transition at B is a switch from the annealed crystal to the grown crystal. The region between A and B has a relatively low defect density while the grown crystal has dislocation loops. These defects continue across the entire low lifetime region shown in Fig. 1 between points B and C. At C, the defects drop to a very low concentration with only a

few dislocation pits visible. Just above this transition at D, a high density of very small saucer pits becomes visible. Since, continued etching does not deepen these pits, as it would for dislocations, they are most likely due to vacancy clusters or vacancy related defects.

Dislocation loops observed between B and C suggest interstitial rich silicon, while the features above C suggest vacancy related defects, or at least a significant drop in interstitial concentration. Such shifts in defect type are observed in CZ silicon and were described by Voronkov in 1982 (Ref. 3). Vacancy and interstitial concentrations are controlled during crystal growth by two parameters: the solid/liquid interface velocity during growth, V, and the thermal gradient present at the interface, G_0. The ratio of these two terms determines which defect species will dominate and at what concentration. These results suggest that such control over point defect generation and incorporation is possible in Mono[2] silicon and might be a factor in optimizing the lifetime profile.
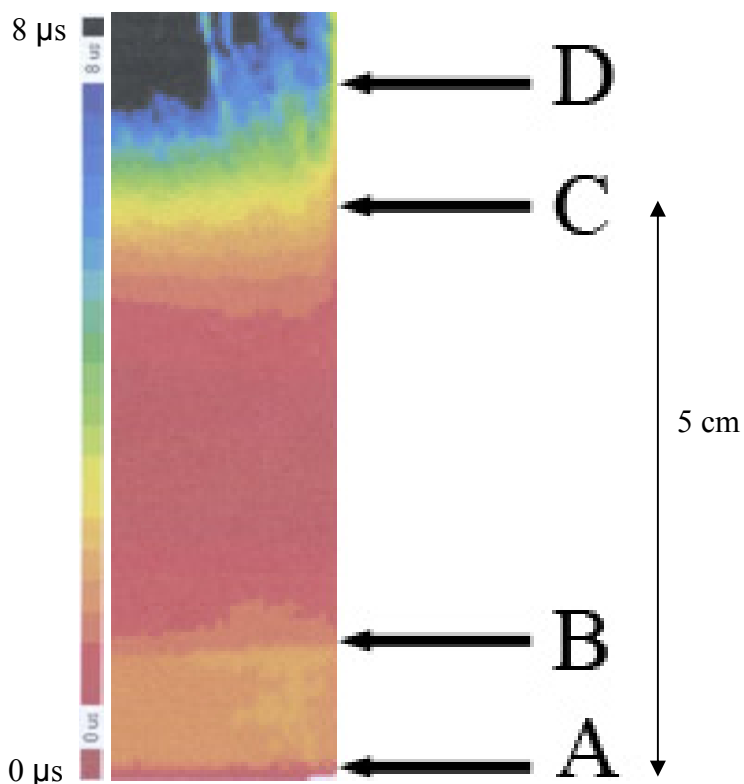
Figure 1: MW-PCD lifetime map of the bottom of the Mono[2] sample. The low lifetime band is 5 cm wide and three lifetime transitions are visible. The labels indicate transitions in lifetime and correspond to the labeling of Fig. 2.

A large scale defect type was observed in the upper half of the Mono[2] sample. These defects, termed dislocation "cascades", are small angle grain boundaries with a high density of dislocations present along them. They have high recombination activity as evident from their lifetime values in the MW-PCD map (not shown), disrupt the crystallinity of the ingot, and so are therefore undesirable. Determining their cause is crucial to their elimination. Shown in Fig. 3 are the etch pit results into the cause of dislocation cascades.

Figure 3A shows a line of dark precipitates at the bottom of the image. These precipitates were identified as silicon carbide by EDS. As the crystal grows upwards, dislocations are observed to form in lines above these precipitates. These lines remain mostly parallel as they propagate as shown in the right of Fig. 3B. The lines can then merge with other lines of dislocations that happen to cross their path during growth. Such a merging is shown near the middle of Fig. 3B as a vertical line cuts across the path of the parallel lines. After merging, the density of dislocations along a line increases. Fig. 3C shows two lines with higher density merging. Tracing such lines in the direction of crystal growth reveals that the continued merging of high density lines of dislocations leads to the formation of dislocation cascades. Lines of dislocations continue to extend and only end at other defects, either by merging with other lines or by termination at defects such as twins, as shown in Fig. 3D.
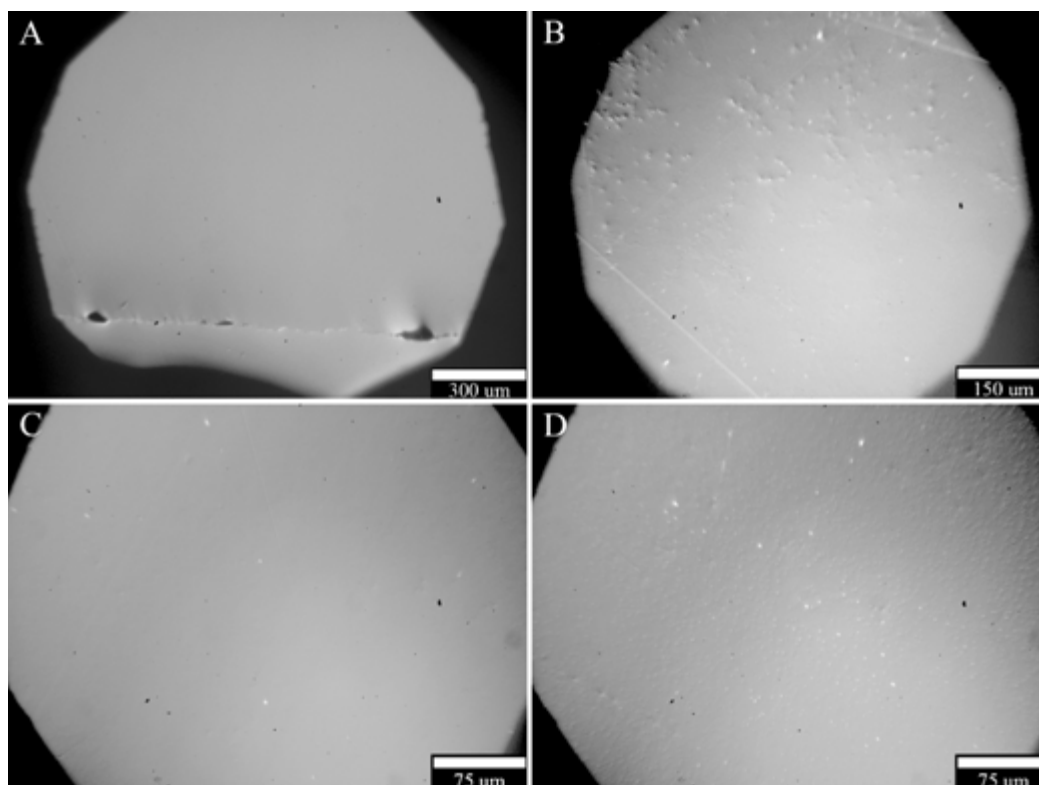

Figure 2: Composite of Nomarski images showing transitions in etch pit defect type with elevation in Mono[2] ingot. Image A shows the first boundary. Image B shows the transition from the annealed crystal (bottom) to the grown monocrystal which contains dislocation loops. Image C shows the region of transition from low to high lifetime. Very few defects are present at this transition. Image D shows very small pit features in a high density. This image is from a region of high lifetime and it is possible that these pits are caused by oxygen precipitation and/or vacancy clusters.

Impurities are introduced into cast silicon through the casting process. Nitrogen, oxygen, and metallic impurities enter the ingot from the casting crucible and carbon enters from the furnace environment. As seen from the study of dislocation lines, precipitation of these impurities can have detrimental effects, not only on the local crystal quality, but for all of the crystal that grows above. These precipitates may form in the melt and become trapped at the solid growth interface, locally disrupting the growing crystal. Controlling the levels of these impurities by stopping their introduction during the casting process will lead to improvements in crystal quality.

Conclusions

Mono^2 silicon has the potential for greater control over the incorporation of point defects than multicrystalline cast silicon because of the absence of large scale defects like grain boundaries that influence the concentrations of defects within grains. Like CZ silicon, vacancy and interstitial concentrations can be controlled through the crystal growth velocity and the thermal gradient across the solid/liquid interface. Impurities play a much larger role in the crystal growth of Mono^2 silicon than in CZ silicon because of the high levels introduced through the casting process. Precipitation of these impurities can lead to the formation of large scale defects such as small angle grain boundaries that can merge and become more severe. These boundaries, termed dislocation cascades, have higher densities of dislocations around them than typical small angle boundaries would.
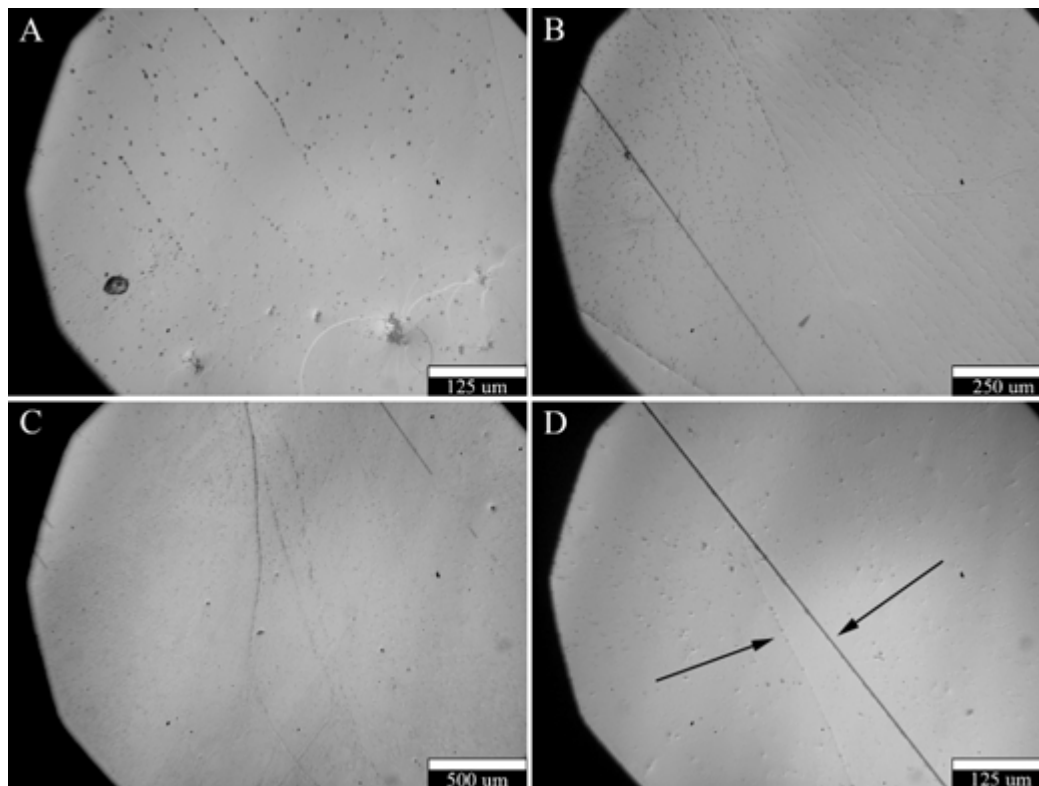
Figure 3: Nomarski images showing behavior of dislocation lines. Image A shows precipitates causing dislocation lines that propagate with the growth direction. Image B shows the lines from Image A visible in the right half of the image merging with other lines. Image C shows a merging of two dislocation lines with higher dislocation density. Image D shows a dislocation line (left arrow) terminating at a twin (right arrow).

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Impurity Significance and Sources in Multicrystalline Cast Silicon

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Introduction

Multicrystalline cast silicon is often used as a substrate material in solar cells due the simplicity and cost effectiveness of the growth process. The drawback of this process is that the resulting ingot has a high concentration of impurities and defects, particularly around its periphery. This results in a significant loss of material because much of the contaminated outer edges of an ingot must be removed prior to wafering. These impurities lead to the presence of bands or low minority carrier lifetime at the edges of wafers cut relatively close to the ingot edge. The majority of impurities originate from the quartz crucible and the furnace environment. The purpose of the experiments described in this report was to identify specific impurities and their concentrations and to trace their sources in the manufacturing process of traditionally cast multicrystalline silicon.

Experimental

A multicrystalline sample from an ingot grown using the traditional casting method was obtained from a solar company. The sample was a longitudinal slice 2 mm thick, 25 cm tall extending from the top to the bottom of the ingot, and 15 cm wide from the crucible edge into the ingot bulk. The ingot edges that were in direct contact with the crucible and the furnace environment during casting are intact in this sample. The sample was chemically polished in a mixture of nitric, acetic, and hydrofluoric acids in a ratio of ~2:1:1 to reduce surface roughness from saw damage. A minority carrier lifetime map of the sample was taken using an Amecon Janus 300-M Microwave Photo-Conductance Decay (MW-PCD) under surface passivation with quinhydrone/methanol solution (ref. 1). Data analysis to produce plots of minority carrier lifetime from the lifetime maps was performed using ImageJ. Fourier Transform Infrared Spectroscopy (FT-IR) was used to determine the interstitial oxygen and substitutional carbon concentration in the sample. A sample was selected from the initial slice for FT-IR at an elevation of 7 cm from the base. This sample extends 10 cm from the ingot edge into the bulk. Prior to the FT-IR measurements, the sample was dipped in HF to strip any oxide on the surface. Measurements were performed at room temperature using a 5 mm square aperture on a BioRad FTS-6000 spectrometer operating in transmission mode. Data analysis was performed according to references 2 and 3. Deep Level Transient Spectroscopy (DLTS) was used to measure electrically active metallic contamination. Concentration measurements were obtained at different elevations near the base of the ingot to determine if such contamination is the cause of the low lifetime regions at the ingot edge. DLTS was performed on these samples over a temperature range of 30K to 300K using a BioRad Digital DLTS System. Three samples were obtained from the same solar company for analysis of the furnace environments using during casting. These samples were exposed to different furnace conditions and the resulting surface contamination was examined using Energy Dispersive Spectroscopy (EDS) and Secondary Ion Mass Spectroscopy (SIMS). EDS was performed in a Hitachi S3200 SEM with an Oxford Isis EDS system. SIMS was performed using a Cameca IMS 6f using an O_2^+ beam running at 5.5 kV.

Results and Discussion

Figure 1 shows the MW-PCD determined minority carrier lifetime superimposed on the FT-IR determined oxygen and carbon concentration as a function of distance from the edge of the ingot. The FT-IR determined interstitial oxygen concentration has an essentially constant value of 1.3×10^{17} cm^{-3} at distances greater than 2 cm from the ingot edge. The substitutional carbon concentration profile at this elevation is nearly flat and has an average value of 1.0×10^{17} cm^{-3}. The minority carrier lifetime is below the detection level of 200 ns for 3 cm from the ingot edge and rises steeply to near 4 µs between 3 and 4 cm from the edge. The shifts in the concentration of substitutional carbon and interstitial oxygen do not correlate with the shift in the minority carrier lifetime. We conclude that neither element is responsible for the observed reduction in minority carrier lifetime at the ingot periphery.


FTIR Determined Light Element Concentrations - 7 cm
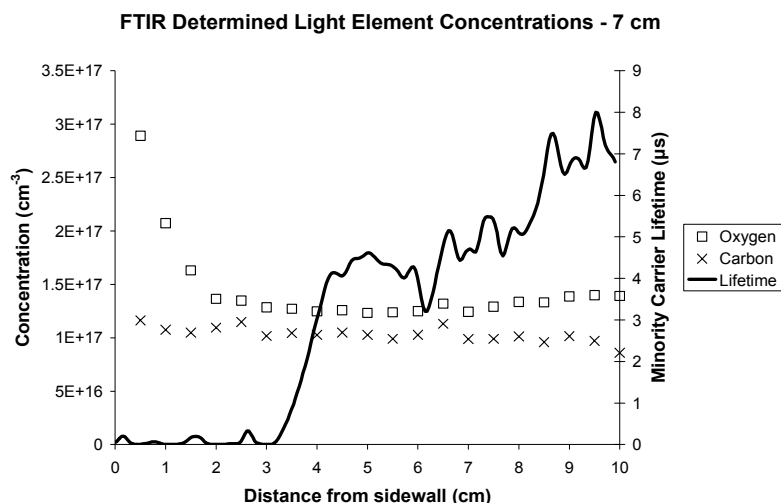
Figure 1: FT-IR determined interstitial oxygen and substitutional carbon concentrations with distance from sidewall at 7 cm elevation. Shown for comparison is the minority carrier lifetime for the same sample. Changes in oxygen and carbon are observed to not correlate with changes in lifetime.

DLTS was able to detect an iron-boron complex peak at 52K allowing the iron concentration profile with elevation from the base to be plotted by measuring diodes at many elevations. The samples used were taken from as close to the center of the base as possible to reduce the influence of impurities diffusing from the crucible sides. The iron-boron complex concentration profile is shown in Figure 2 along with a plot of the minority carrier lifetime at the same position. The concentration varies from 4.7×10^{12} cm^{-3} at an elevation of 0.2 cm and remains fairly constant until an elevation of 1.2 cm where it begins to drop gradually to 2.0×10^{12} cm^{-3} at an elevation of 2.3 cm. Grain to grain variation is responsible for the concentration profile not being smooth. Beyond this elevation the iron-boron concentration drops below our detection level of 1.5×10^{12} cm^{-3}. The detection limit is determined by the doping level, which for this sample is 10^{16} cm^{-3} concentration of boron. The rise in lifetime with elevation corresponds well with the drop in iron-boron concentration suggesting that iron is responsible for the low lifetime bands seen in the sample. This iron is believed to originate in the casting crucible, but the crucibles are known to be free of iron prior to being used in the casting process. Thus, iron must be introduced by the processes used during preparation of the crucible for casting, as well as the casting process itself.

Lifetime Correlation with [FeB] at Ingot Base
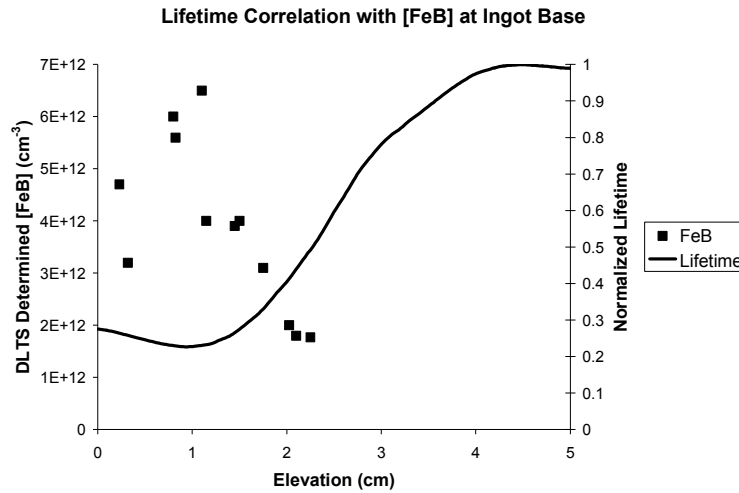
Figure 2: DLTS determined iron-boron complex concentration profile with elevation . Shown for comparison is the minority carrier lifetime of this region as measured by MW-PCD. A drop in FeB concentration is observed to correlate with a rise in minority carrier lifetime.

In order to determine the source of iron in the crucible, three samples were exposed to different furnace environments and the resulting contamination on the surface of these samples was analyzed. A large brick of multicrystalline silicon was exposed to the casting furnace environment and a slight green haze was formed on its surface. A CZ wafer was subjected to the environment of a furnace used to bake the release coating onto the crucible prior to casting. An olive green coating was formed on the surface. A piece of feedstock was partially melted in the casting furnace environment and during this process a dark coating formed on the surface. All of the samples were examined within the SEM by EDS.

CZ Sample SIMS Data
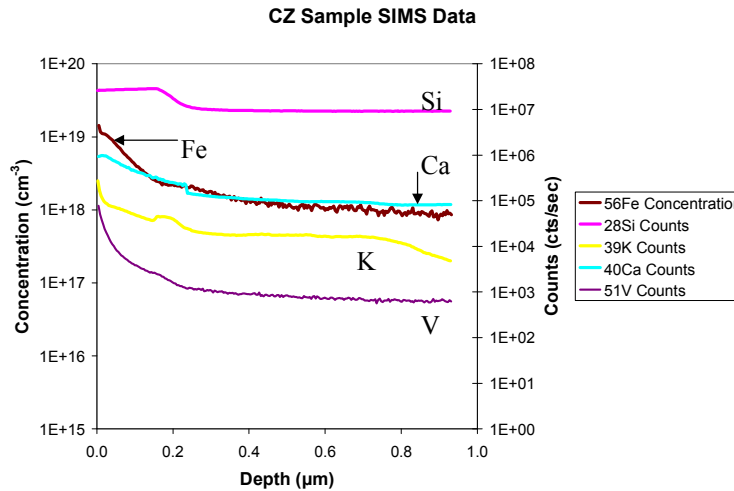
Figure 3: SIMS data from a second site on the contaminated CZ wafer. Only Fe has been compared with a standard so only its concentration information is trustworthy. All other elements are shown for qualitative purposes.

161

The slight green haze on the multicrystalline sample exposed to the casting furnace environment was found by EDS to contain C, O, and Fe. The dark coating on the feedstock piece was identified by EDS as silicon carbide. The CZ sample exposed to the release coating baking kiln only returned oxygen when analyzed by EDS. SIMS was performed on this sample to determine if any elements were present below the detection level of EDS and the results are shown in Figure 3. The elements detected in this surface layer are calcium, chromium, iron, potassium, and vanadium. The iron levels were compared to a standard, but no other elements were. Therefore, only the iron concentrations are truly quantitative and all other elements are only shown for qualitative purposes. The oxide deposited on the surface of the CZ wafer contains iron on the order of 10^{19} cm^{-3} iron which diffused into the wafer at a concentration of around 10^{18} cm^{-3}. This is a significant source of iron in the crucible and the resulting cast ingot and a likely cause for the reduced edge lifetime (ref. 4).

Conclusions

We have examined a longitudinal sample of multicrystalline cast silicon that has intact the edges of the ingot that were in contact with the crucible and the environment. We have found that oxygen and carbon concentration profiles do not explain the observed near-edge reduced minority carrier lifetime maps while the iron concentration profile does. We have located the sources of these three impurities in the casting process and believe that iron present at the ingot edge enters the ingot from the casting crucible via solid state diffusion that takes place after solidification while the ingot is still hot. Iron dissolved from the crucible into the melt and from the casting furnace environment is responsible for the bulk concentration levels of iron. Much of this iron segregates during solidification to the top of the ingot. The iron in the crucible likely originates in the furnace used to bake on a release coating. Carbon enters the melt from the casting furnace environment which explains why we see no significant variation in carbon with distance from the crucible. Oxygen enters the ingot from the casting furnace environment and by the crucible itself dissolving. The elevated oxygen levels near the ingot periphery are due to solid state diffusion from the crucible into the hot ingot during casting, as seen with the iron. Controlling the environments of the furnaces used during the casting process in future manufacturing will lead to a significant reduction of contamination in traditionally cast silicon.

Acknowledgements

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Hydrogen Passivation of a (110)/(100) Silicon Grain Boundary investigated by J-V, C-V and Capacitance Transient Characterizations

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ABSTRACT

The density of grain boundary (GB) states before and after hydrogenation was evaluated by J-V, C-V and capacitance transient methods using gold/hybrid orientation direct-silicon-bonded (DSB) p-type silicon wafer junctions. The GB potential energy barrier in thermal equilibrium was reduced by 70meV after hydrogenation. It was found that the clean sample had a density of GB states of ~6×10^{12} cm^{-2}·eV^{-1} in the range of E$_v$+0.54~0.64eV. Hydrogenation reduced the density of GB states to ~9×10^{11} cm^{-2}·eV^{-1} in the range of E$_v$+0.56~0.61eV. Fe contamination increased the density of boundary states by at least three times greater than 2×10^{13} cm^{-2}·eV^{-1}, and the zero-bias barrier height by 70meV over the clean sample. The subsequent hydrogenation of the Fe decorated GB lowered the capacitance back to that of the clean sample.

I. INTRODUCTION

Multi-crystalline silicon (mc-Si) solar cell wafers benefit from reducing the electrical activity of such as dislocations and grain boundaries (GBs). A common solution is to employ hydrogen passivation during the cell fabrication process. It has been known that a plasma of monatomic hydrogen provides a significant reduction in both the density of states and the GB potential energy barrier [1]. Electron beam induced current (EBIC) analyses has shown that for GBs in less contaminated regions of mc-Si, the effect of hydrogen passivation depends on both GB character and impurity contamination, while for highly contaminated regions, the hydrogen passivation was less significant and was not affected by GB character [2]. Although it has been observed that hydrogenation decreases GB recombination activity, it is not fully understood how hydrogenation affects each component of the electrical characteristics, such as the density of GB states and GB potential energy barrier for both clean and impurity decorated GBs. These issues will be studied in this paper. Mc-Si wafers have the complex defect structure with dislocations, GBs (subgrain-boundaries), twin boundaries, and micro-defects which are inhomogeneously distributed. Besides, impurities due to the metallurgical grade silicon feedstock and crucible walls can in-diffuse and be incorporated with structural defects. These facts lead to difficulties in obtaining a unique experimental signal from the individual defect of interest. The major obstacle is that experimental characterization of GB electrical properties is very variable without a uniform defect array positioned at a well controlled depth. For these reasons, in this study, hybrid orientation technology (HOT) DSB wafers [3] were selected as a "model" (110)/(100) silicon grain boundary.

II. EXPERIMENTAL

DSB wafers are composed of a p-type (110) Si top layer bonded to a p-type (100) Si substrate wafer. A (110) layer was transferred to the (100) substrate by hydrophilic wafer bonding and cleavage. The thin residual oxide layer at the bonding interface was dissolved by a high temperature annealing process. Cross-sectional TEM revealed no interfacial oxide layer or oxide precipitates, and secondary ion mass spectroscopy and ellipsometry measurements indicated no detectable oxygen at the bonding interface. In this paper, two kinds of the bonded wafers were prepared depending on the top layer thickness. One has 200nm (110) top layer which was cleaved and chemical-mechanical polished, while the other sample had the (110) top layer epi-thickened to 2.3μm. The bonding interface studied here can be categorized as a general large-angle GB according to the concept of coincident site lattice, which is the type of boundary most effectively reducing the carrier lifetime in mc-Si. Hydrogen was introduced by boiling in water [4]. Since at higher temperature the sample is more prone to impurity contamination, the low boiling point of water has an advantage of less contamination over other techniques. Iron contamination was performed by dipping the sample in an iron-spiked nitric acid solution, and subsequent two-step annealing process at

900°C for 1h., followed at 700°C for 1h. in an argon. For the electrical characterizations, 1mm diameter gold and 2mm diameter aluminum contacts were evaporated on the (110) top layer. Ohmic contact was made on the sample backside by rubbing gallium-indium eutectic. Current-voltage (I-V), capacitance-voltage (C-V, 1MHz), and capacitance transient measurements were carried out on a Bio-Rad DL8000 deep level transient spectroscopy system.

III. RESULTS AND DISCUSSION

1. 200nm sample: J-V/C-V study

Figure 1 shows the energy band diagram of gold/DSB junctions before and after an applied bias. Density of GB states can be investigated through J-V characteristics. Majority carrier transport across a GB can be described by a double-depletion-layer/thermionic-field emission model [5].

$$J = R^* T^2 \exp\left(-\frac{\Phi + qV_L}{KT}\right)\left(1 - \exp\left(-\frac{qV}{KT}\right)\right),$$

where J is the current density, R^* the Richardson constant, $(\Phi + qV_L)$ the potential energy barrier on the left-hand side of the GB, K Boltzmann constant, and V external bias. It was found from the measured J-V data that the barrier $(\Phi + qV_L)$ is decreased very little with an increase in applied bias. This indicates that the device structure behaves like a conventional Schottky diode, and the positive GB charge is balanced mainly by the bias generated negative space charge $(q \cdot N_A^-)$ on the right side of the GB. Hence, the charge density of the GB is obtained using the charge neutrality formula shown below.

$$q \cdot N_{GB} = Q_M + q \cdot N_A^- \cdot d_{GB} + q \cdot N_A^- \cdot d_R,$$

where N_{GB} number of charges per unit area in the GB, Q_M the negative charge in metal, N_A^- boron doping concentration, d_{GB} the GB depth, d_R the depletion width on the right side of the GB. With the charge density of the GB and the bias-dependent level of the electron filled trap state obtained from $(\Phi + qV_L)$ using J-V data, a plot of N_{GB} as a function of trap energy level was made for both clean and hydrogenated samples, see Fig. 2. The slope of the plot $dN_{GB}/(\Phi + qV_L)$ represents the density of GB states. For the clean sample, the density of GB states was ~6×10^{12} cm^{-2}·eV^{-1} in the energy level range of E$_v$+0.54~0.64eV. It was reported previously that the density of GB states of clean HOT bonded wafers is ~6.6×10^{12} cm^{-2}·eV^{-1} [6]. For the hydrogenated sample, the density of GB states was found to be the minimum ~9×10^{11} cm^{-2}·eV^{-1} in the range of E$_v$+0.56~0.61eV which is about 7 times less than that of the clean sample. The density of hydrogenated GB states was reduced until the energy level of 0.52eV from the valance band edge. The reduction of the density of GB states for hydrogenated sample is in favor of the suppressed recombination activity of the GB. Fig. 3 shows C-V characteristics before and after hydrogenation. The capacitance signal reflects the charge density of the GB which is a function of the density of GB states, the charge neutral level position and the position of the highest electron filled trap state. The charge density of the GB was decreased after hydrogenation. It should be noted that electrically active boron can be passivated by injected hydrogen. The lower doping level of the bonded wafers can decrease the capacitance under the assumption that the electronic structure of the GB is not changed after hydrogenation. Our measured C-V characteristics revealed the higher capacitance after hydrogenation. It indicates that change in the electronic structure of the GB due to hydrogen treatment must be responsible for the increased capacitance of the hydrogenated sample. The GB potential energy barrier (qV_R) at zero bias before and after hydrogenation, which affects optically generated minority carriers collection efficiency at the GB, can be evaluated from C-V characteristics. The higher value of capacitance after hydrogenation indicates the decreased depletion width in the GB barrier regions. This means that the potential energy barrier of the GB becomes lower after hydrogen treatment. The GB potential energy barrier in the thermal equilibrium was reduced by 70meV from 0.46eV (before hydrogenation) to 0.39eV (after hydrogen treatment).

2. 200nm sample: capacitance transient study

The capacitance transient method (C-t) gives us an insight on the distribution of the GB states by analyzing the data of the charge density of the GB and GB charge decay rate (hole emission rate in this study) acquired from C-t plot. The amount of charge in the GB can be measured capacitatively while non-equilibrium conditions caused by the pulse bias for brief periods revert to the steady-state. Using Poisson's equation and the concept of the charge neutrality, the GB hole density (N_{GB}) at the reverse bias (V_R) can be calculated from the capacitance (C) [6] by

$$V_R + V_{bi} = \frac{(d_{GB} + d_R)^2 \cdot q \cdot N_A}{2 \cdot \varepsilon_{Si}} - \frac{N_{GB} \cdot q \cdot d_{GB}}{\varepsilon_{Si}}, \quad d_{GB} + d_R = \frac{\varepsilon_{Si} \cdot A}{C},$$

where $d_{GB} + d_R$ the total depletion width, q is the electron charge, N_A the doping concentration, ε_{Si} the dielectric constant of silicon, d_{GB} is the GB depth, and V_{bi} the built-in potential which is approximately 0.23eV. GB barriers were exposed to 20V for brief periods to empty the GB energy states, and then monitored the rise of reverse capacitance due to hole emission (the decay of positive GB charge) as a function of time in thermal equilibrium. The relation between the charge density at the GB (N_{GB}) and the measured capacitance (C) under zero bias can be simplified from the above equation.

$$N_{GB} = \frac{1}{d_{GB}} \left(\frac{\varepsilon_{Si}^2 \cdot A^2 \cdot N_A}{2C^2} - \frac{\varepsilon_{Si} \cdot V_{bi}}{q} \right)$$

Charge decay rate of the GB versus the charge density of the GB plots before and after hydrogenation were compared in Fig. 4. The energy level position affects the emission rate exponentially. The higher hole emission rate for the hydrogenated sample indicates that the trap filling position is closer to the valance band edge. The curvature of the plot is inversely proportional to the density of states. Hydrogenated sample with the higher curvature indicates the decreased density of the states compared with that of the clean sample.

3. 2μm sample: C-V study

Figure 5 shows the C-V characteristics of clean, iron decorated, and Fe-decorated plus hydrogenated GB. It was found that iron contamination increases both the density of boundary states by at least three times (at least greater than 2×10^{13} cm^{-2}·eV^{-1}) and the zero-bias barrier height by 70 meV compared with the clean sample [6]. The subsequent hydrogenation of Fe decorated GB led the capacitance revert to that of the clean sample. It is suggested that hydrogenation of iron contaminated GB produces the passivation effect.

IV. CONCLUSIONS

The impact of hydrogen passivation of clean and Fe decorated (110)/(110) GB was investigated using a GB model structure and electrical characterizations. Hydrogenation reduced the density of clean GB states and trap levels were broad distributed compared with the clean sample. GB potential energy barrier was the largest for the Fe contaminated sample, and the smallest for hydrogenated GB. This result indicates that a larger barrier for the Fe contamination (a smaller barrier for the hydrogenation) enables more (less) effective minority carrier collection affecting the recombination activity of GB.

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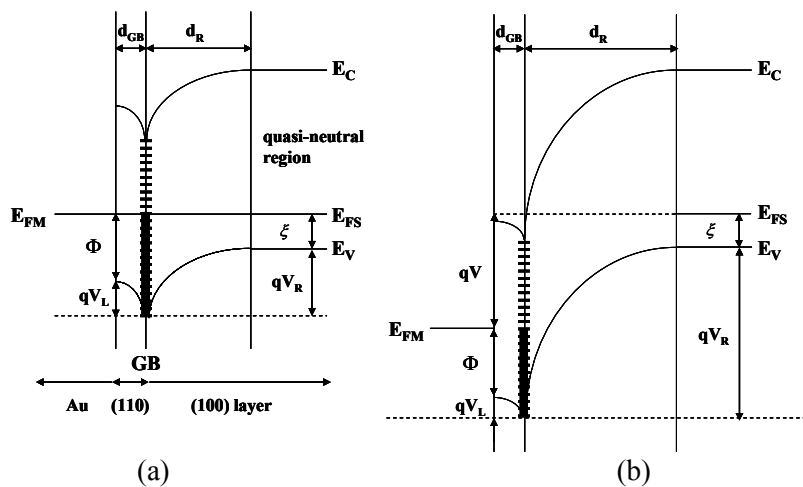
(a)   (b)

Fig. 1 Energy band diagram of gold/DSB junctions (a) at zero bias and (b) under an applied bias, V.
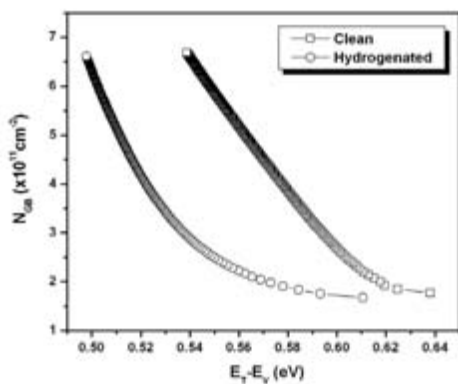

Fig. 2 GB charge density as a function of trap energy level for clean and hydrogenated GB.
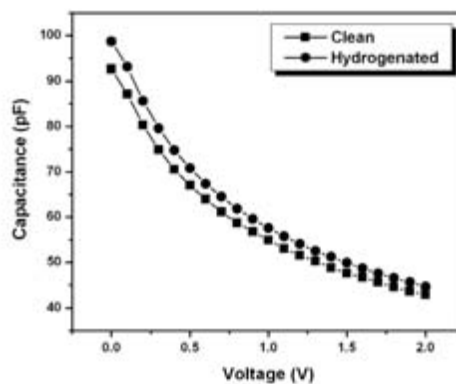

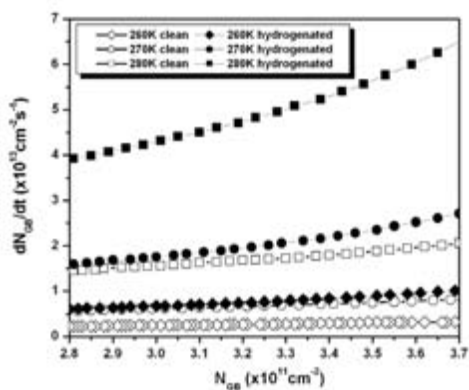Fig. 3 C-V characteristics before and after hydrogenation.

Fig. 4 Charge decay rate vs. GB charge density at different temperatures for clean and hydrogenated GB.
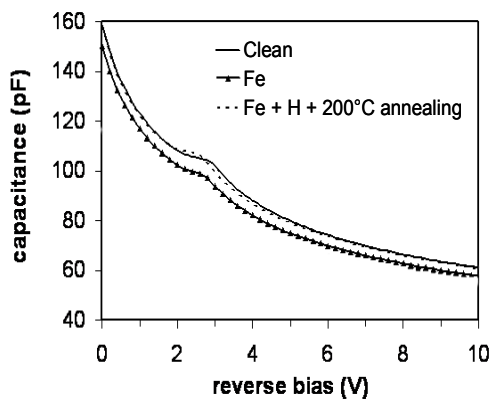

Fig. 5 C-V characteristics for clean, Fe decorated, and Fe-decorated plus hydrogenated GB.

Intragrain defects in polycrystalline silicon thin-film solar cells on glass by aluminum-induced crystallization and subsequent epitaxy

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Abstract

The origin of intragrain defects in polycrystalline silicon films grown by ion-assisted deposition (IAD) on aluminum-induced crystallization seed layers on glass is investigated. The microstructure of these polycrystalline Si films is bimodal, with near defect-free regions of <001> orientation along the growth direction and highly defective regions containing smaller grains of <111> orientation. In the defective regions, the dominant structural defects are twins in the seed layer and stacking faults in the IAD-grown epitaxial layer, both lying on {111} planes. The stacking faults originate at the seed layer surface due to surface imperfections, indicating that the quality of the seed layer surface plays an important role for the quality of the epitaxial Si film. We find a clear correlation between the structural crystal quality and defect-related radiative transitions at sub-bandgap wavelengths. Two dominant defect levels ($\sim$0.20 eV and $\sim$0.29 eV below the conduction band edge) are observed and identified as impurity-related.

1. Introduction

The overwhelming majority (>90%) of solar cells are made of silicon. However, due to the current worldwide shortage of silicon, considerable research efforts are being directed to thin film silicon worldwide. Inexpensive, device-grade, and large-grained polycrystalline silicon (pc-Si, grain size > 1 μm) on foreign substrates (glass in particular) has seen increasing research interest in thin-film solar cells due to its significant industrial appeal [1-3]. One approach to realize pc-Si thin-film diodes is to prepare a thin crystalline seed layer on glass by aluminum-induced crystallization (AIC), followed by epitaxial thickening by ion-assisted deposition (IAD) [4]. The AIC process is a promising seeding technique because it produces large-grained ($\geq$ 20 μm), heavily doped pc-Si films on glass [5,6]. Subsequent epitaxial thickening by non-ultra-high vacuum IAD is very attractive because the growth of device-grade Si epitaxial layers on both (100) Si wafers and AIC-seeded glass at low temperatures ($\sim$600°C) has been demonstrated [7,8]. However, the polycrystalline nature of the seed layer and its surface roughness make epitaxial growth much more difficult, and heavily defective grains are often present in the epitaxial layer [9,10]. Furthermore, the open-circuit voltage (V_{oc}), which is an indicator of the

film's structural quality, is found to be quasi independent of grain size [2]. Therefore, the intragrain defects can be a major limiting factor for the electrical quality of pc-Si layers [11]. In this work, our goal is to study the origin of intragrain defects in pc-Si films grown by IAD on AIC seed layers at low temperature.

2. Experimental details

To make a solar cell, a thin AIC polycrystalline Si seed layer is formed at 400-500°C on a silicon nitride (~80 nm)-coated, 3-mm-thick glass substrate (Borofloat 33 from Schott AG). This seed layer is 50-100 nm thick, has an average grain size of the order of 10 μm, and is p-type due to the presence of aluminum (~2 × 10^{19} cm^{-3}). Using this thin layer as a crystal template, an n-type (~8 × 10^{16} cm^{-3}, P) layer (~1.8 μm) is epitaxially grown on top at ~600°C by IAD, thus forming the p-n junction and the absorber layer of the solar cell. A heavily doped 80-nm n-type layer (~5 × 10^{19} cm^{-3}, P) is finally grown as a back-surface field and contact layer. Upon completion of the IAD process, the solar cells receive a rapid thermal anneal (RTA) treatment and a hydrogenation treatment for defect passivation. Finally, the cells are metallized. Further details on the cell fabrication process can be found elsewhere [1].

To establish an accurate correlation between orientation, structure, composition, and electronic levels in the epitaxial films, we selected specific areas to perform all measurements. First, orientation maps are generated by electron backscatter diffraction (EBSD) (Hitachi S-4300N) at 20 kV and a working distance of 15 mm over a film patterned with a microgrid. Cathodoluminescence (CL) (JEOL 5800 SEM) maps of electronically active defects are then acquired and compared with the orientation maps. Specifically selected sections crossing <001>- and <111>-oriented regions are prepared using a focused ion beam (FIB) workstation (FEI-Nova 200 Dual Beam) at normal operating parameters and then investigated by cross-sectional transmission electron microscopy (XTEM) (FEI-F20) at 200 kV. The distribution of various impurities (O, C, N, and Al) is determined by energy-filtered transmission electron microscopy (EFTEM) at 200 kV and 0.5 eV/channel.

3. Results and discussion

Figs. 1(a) and 1(b) show EBSD and energy-resolved photon intensity maps of the same area of the solar cell. Those grains showing a clear diffraction pattern (and which are therefore indexable) are highly <001>-oriented along the growth direction. In other regions the diffraction pattern is degraded, resulting in non-indexable locations (dark areas in Fig. 1(a)). These degraded regions are shown below to be very defective and to contain smaller grains with <111> orientation. When compared with the EBSD results, the photon energy mapping (Fig. 1(b)) indicates that both the photon intensity and the photon energy depend on the orientation and quality of the diffraction pattern; that is, the higher the quality, the higher the photon intensity, and the lower the quality, the more the energy of the spectrum is red-shifted. Therefore, there is a certain correlation between orientation and defects/impurities in the epitaxial layer.

Using the FIB workstation, XTEM specimens are prepared on selected areas cutting through both a defective region and a neighboring defect-free region (A and B in Figs. 1(a) and 2(a)). The good region B, containing just one grain, is of excellent crystalline quality. The interface between the epitaxial layer and the seed layer is almost invisible, and the growth direction is determined to be <001> (inset of Fig. 2(a)). In contrast, a high defect density can be seen on the

left side of the grain boundary (Fig. 2(a)). The growth interface is clearly visible in region A, indicating that at the start of epitaxy, the hydrogen termination on the seed layer surface had already been slightly deteriorated, leading to some contamination (most probably involving N, O, and C). The defective region is actually polycrystalline, although the <110> diffraction pattern is dominant in this projection direction, as seen from the selected-area diffraction (SAD) pattern in Fig. 2(a) (a 20-µm aperture size is used). In fact, the seed layer is found to contain smaller grains of 1–6 µm, and the small grains are found to be <111>-oriented along the growth direction (Fig. 2(b)). It is also clearly shown that Si grows epitaxially on the seed layer, but not on the islands that have different orientations from the seed layer (Fig. 2(b), see also Ref. [12]). The predominant extended defects in the faulted region are determined to be stacking faults on {111} planes and can be seen to originate at the seed layer surface steps (i.e., the islands) or the grain boundaries of the seed layer where localized etching of the underlying SiN layer has occurred during the solar cell fabrication process. This etching of the SiN layer should be avoided because the adjacent seed layer surface regions may be contaminated by outgassing of impurities from the glass substrate, as indicated by the clear interface and dislocations close to the voids even in the good region where some SiN was etched away (Fig. 4(b)). Twins in the seed layer (also on the {111} planes) are usually found in the defective region, but not in the good region (Fig. 2). It is interesting to note that, in the case of high-temperature epitaxial thickening of AIC seed layers, epitaxial stacking faults are seen on the {111} planes, even for grains well-oriented along the <001> direction [11]. It therefore follows that the defective regions are related to (i) the grain orientation in this low-temperature growth regime (~600°C) (as suggested by Wagner et al. [13]), (ii) AIC seed layer surface imperfections, and (iii), possibly, thermal mismatch between the (SiN-coated) glass substrate and the Si film during RTA treatment at high temperature (900°C).

To obtain insight into the electrical quality of the investigated samples, CL spectra were recorded for the photon energy range 0.75-1.40 eV. Fig. 3 shows the emission spectra obtained from positions "A" and "B" as indicated in Fig. 1(a), at a sample temperature of 17.9 K using an electron beam with an acceleration voltage V_{ac} of 10 kV and a beam current I_b of 5 nA. At this temperature, crystalline silicon has a bandgap energy of ~1.17 eV. Two broad peaks at ~0.88 and ~ 0.97 eV can be seen in spectra "A" and "B", respectively, which indicates a broad defect (or impurity) distribution. As mentioned above, stacking faults are the predominant structural defects in the epitaxial layer, while dislocations are rarely observed. So it is not surprising that we do not observe the so-called D lines commonly associated with dislocations in crystalline Si [14,15]. Although the D1 line (~0.81 eV) and D2 line (~0.87 eV) are thought to be related to stacking faults [16,17], only the D2 line is close to the peak at ~0.88 eV at the defective region where the predominant defects are stacking faults. Therefore, stacking faults are not the main mechanism that causes the energy shift (1.17 - 0.88 = 0.29 eV and 1.17 - 0.97 = 0.20 eV) shown in spectra "A" and "B". Given that the base region of the investigated samples is n-type, it seems clear that these two defect levels are near the conduction band edge. These two energy levels have been associated with impurities and their complexes [18-21].

The existence of impurities in large quantities is corroborated by EFTEM. Because the most common contaminants in ion-assisted deposition are O, C, and N [7], we run mappings of these three elements and of Al which is vital for the AIC process. Here, only O maps are shown (Fig. 4). O incorporation, especially at locations with high stacking fault density, is high (> 5×10^{19} cm^{-3}), despite the high growth rate (250 nm/min). No O incorporation is detected in the good region (Fig. 4(b)). Similar results are obtained for N and C. The different incorporation of these

impurities can therefore account for the different energy shift shown in Fig. 3. However, it is difficult to identify the impurity levels, because the spectral peaks are smeared in energy due to the nature of the investigated material, as shown in Fig. 3. Fig. 4 also shows that a thin aluminum oxide layer exists on the SiN layer in both regions. So far, it is not known how this oxide layer is formed and where the O comes from [11,22].

4. Conclusions

In summary, the origin of the intragrain defects in pc-Si films grown by IAD on AIC seed layers has been investigated. We find a bimodal microstructure, with <001>-oriented regions of high crystalline quality and defective regions containing smaller grains which are <111>-oriented. The interface is clearly seen in TEM images of the defective regions, whereas it is almost invisible in the good regions. In the defective regions, the dominant defects are twins in the seed layer and stacking faults in the epitaxial layer, which are both on {111} planes. Stacking faults originate at imperfections at the seed layer surface, indicating that the seed layer surface quality, which is found to depend on crystal orientation, plays an important role in determining the subsequent epitaxial layer quality. There is much more O (and also C and N) in the defective regions compared to the good regions, as confirmed by EFTEM. We found a good correlation between crystal orientation, crystal quality, and the presence of deep-level defects. Radiative recombination is dominated by impurity-related defect levels (~0.20 and ~0.29 eV below the conduction band edge in the good and defective regions, respectively), suggesting that some impurities are electronically active and play a significant role in limiting device performance.

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Figure captions

Fig. 1. (a) EBSD map (plan view). The solid line connecting regions "A" and "B" represents the position where an XTEM specimen is prepared by FIB. (b) Photon energy map of the same sample area. RGB colors are used for labeling the crystal orientation and photon energies.

Fig. 2. (a) Bright-field XTEM image. The two insets are the SAD pattern of the defective region and a HRTEM image of the good region. (b) Z-contrast image of the defective region. The two insets are the atomic-resolution Z-contrast images of the interface and one twin in the seed layer. Both stacking faults (SFs) and twins are on {111} planes (see dashed lines). The islands have different orientation compared to the underlying seed layer grain.

Fig. 3. CL spectra at 17.9 K from regions "A" and "B" in Fig. 1(a). A Gaussian function is applied to fit each spectrum (smooth solid line). The photon energies corresponding to the centre of the emission peaks are also indicated (dashed lines).

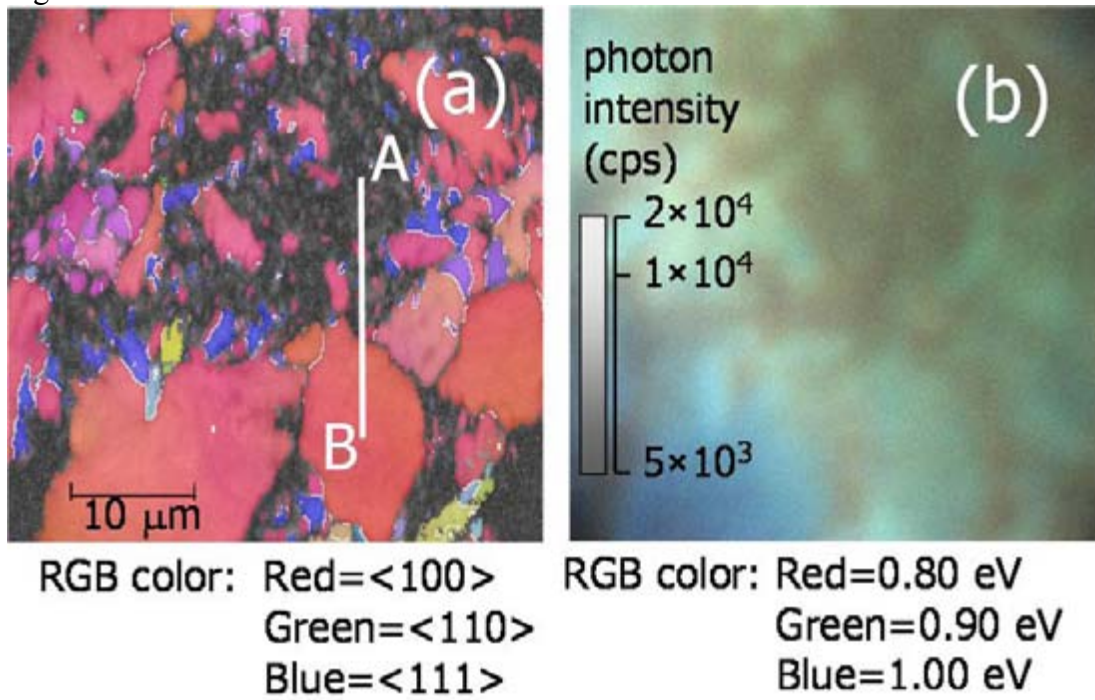Fig. 4. Oxygen maps of (a) the defective region and (b) the good region.

Fig. 1

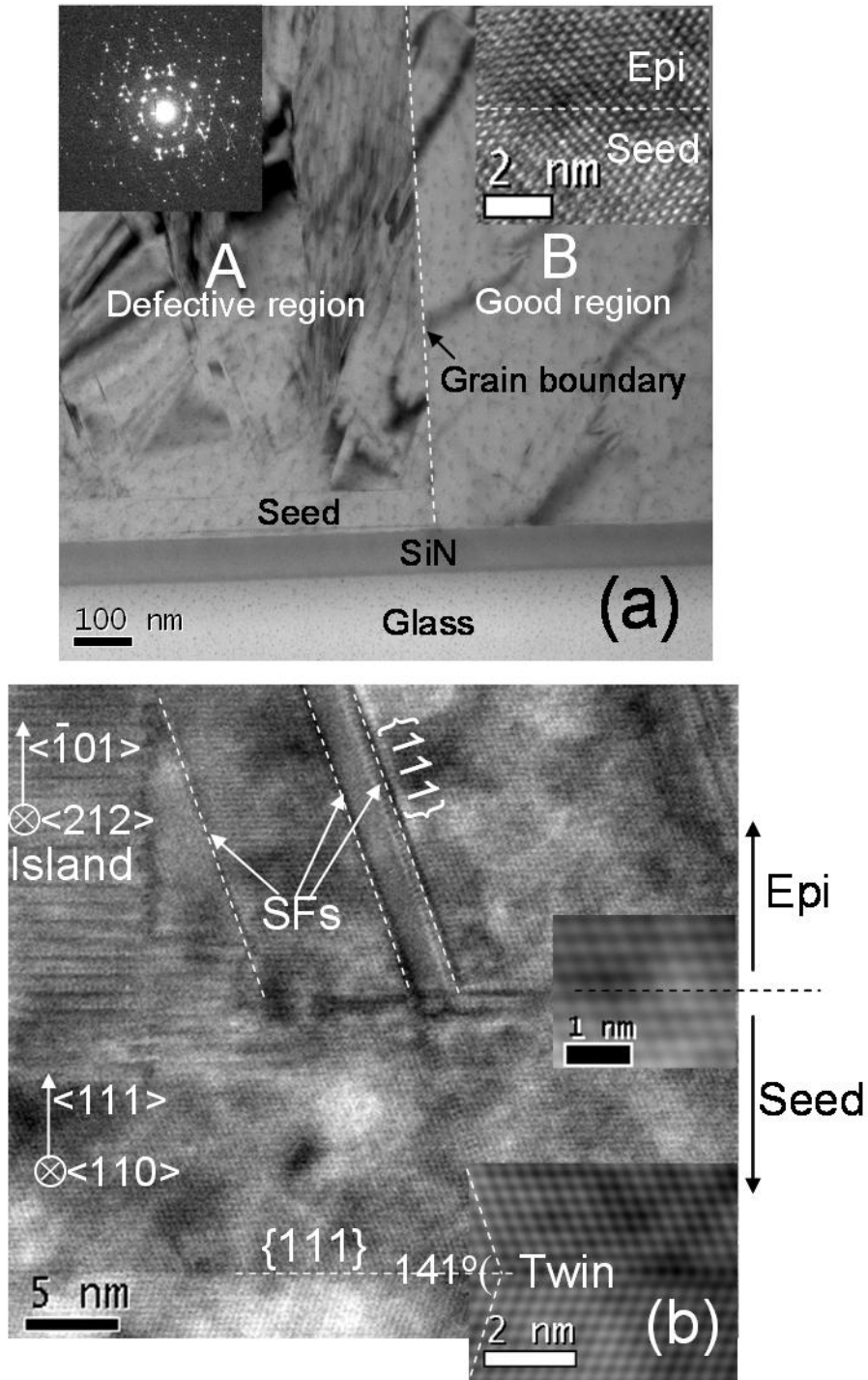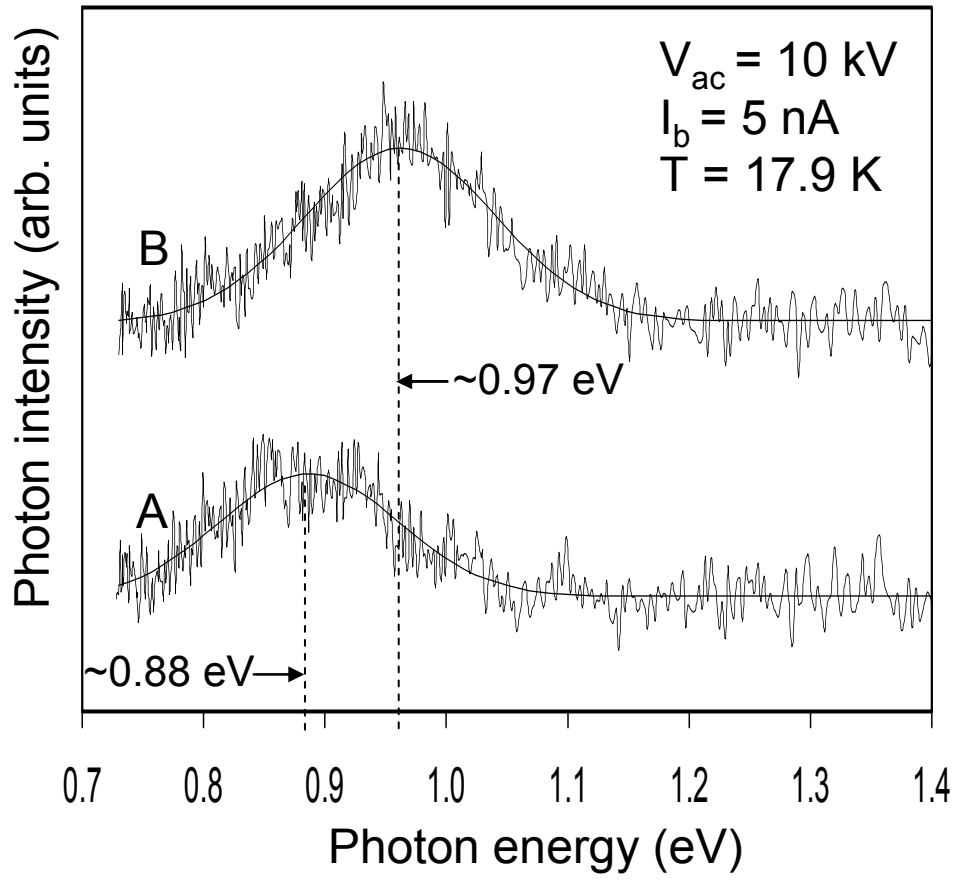RGB color: Red=<100>
Green=<110>
Blue=<111>

RGB color: Red=0.80 eV
Green=0.90 eV
Blue=1.00 eV

Fig. 2
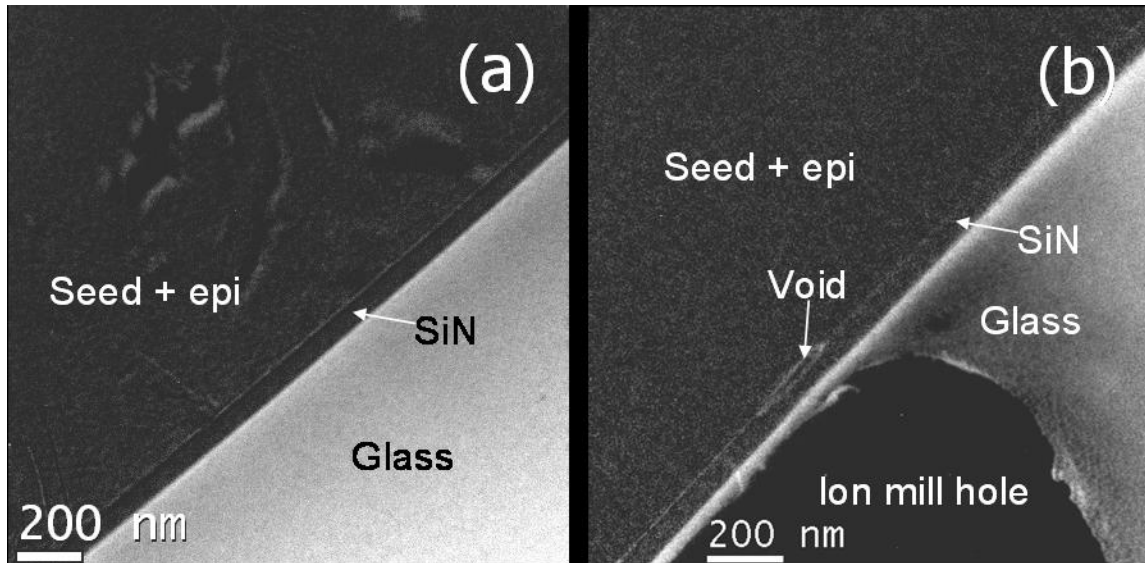

(a)

(b)

173

Fig. 3

Fig. 4

Development of low cost plated contact solar cells (PCSC) on high sheet resistance emitters

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Abstract

In this paper we report on the preliminary study of plated contact solar cells (PCSC). Efficiencies above 17% have been achieved with plated contacts on high sheet resistance emitters. PCSC is a low cost solar cell manufacturing method which utilizes a screen printable phosphoric acid based etching paste to open windows for fingers and busbars in the silicon nitride anti-reflection coating. This method also utilizes an alkaline commercial electroless nickel plating bath followed by light induced silver plating to achieve front side metallization. However, nickel silicide barrier layer must be formed to avoid electromigration of silver metal into silicon. The desired silicide is the mono layer, which has to be formed at a temperature below 750°C. We have found the minimum nickel silicide sheet resistance to be 3.3 $\Omega/\square$ when annealed at 650°C.

Introduction

For crystalline solar cells to compete with conventional grid electricity the cost of electricity produced must be on the order of $0.10/kWhr. Increasing solar cell efficiency is the key to bringing cost down. To increase the efficiency and lower the cost of solar cell a method for making contact to high sheet resistance emitters (~100 $\Omega/\square$) should be developed. High sheet resistance emitters are advantageous because they have higher short circuit current and open circuit voltage compared to low sheet resistance emitters which are hampered by auger recombination due to the heavy doping. Low sheet resistance emitters favor ohmic contact formation but have an electrically dead layer on the front of the cell giving it a poor blue response. However, forming a high quality contact to high sheet resistance emitters with screen printing is challenging because contact resistance is proportional to $(N_D)^{-1/2}$ [1]. Also, the firing process of screen printed paste drives the contact down into the wafer towards the emitter junction, where the doping concentration is lower and may lead to high contact resistance. To avoid contact formation beneath the surface of the solar cell, a low-cost method utilizing electroless nickel followed by light induced plating of silver is being developed at Georgia Tech. This metallization scheme is advantageous for several reasons; firstly it enables contact formation to the surface where doping concentration is the highest. Secondly, low resistivity nickel silicide is easily formed by anneal as a barrier against electromigration of silver or copper in silicon [2]. Thirdly, there is the possibility of realizing very fine and tall fingers to reduce shadowing and increase fill factor. Finally, the plated contact solar cells (pcsc) follows a simple and low cost process where the SiN is opened by screen printed etching paste followed by drying at medium temperature before rinsing in de-ionized water. In this paper we will present the preliminary results on the plated contact solar cells.

Cell Fabrication

In this study 300 μm thick textured boron doped 1-1.5 Ω-cm float zone wafers were used along with an alkaline commercial nickel plating bath. After the wafers were textured and cleaned they were diffused in a $POCl_3$ tube furnace for n^+ emitter formation, the resulting sheet resistance was 75-80 Ω/sq. This was followed by low frequency (50 kHz) PECVD silicon nitride deposition of 750 Å at 450^oC for an anti-reflective coating. Next, Merck SolarEtch™ was printed on the SiNx followed by hot plate dry to open windows in the SiN_x for the fingers and busbar. The Etch procedure is shown figure1.

| screen print etching paste | → | Dry etching paste on hot plate | → | DI water rinse to clear the fingers |

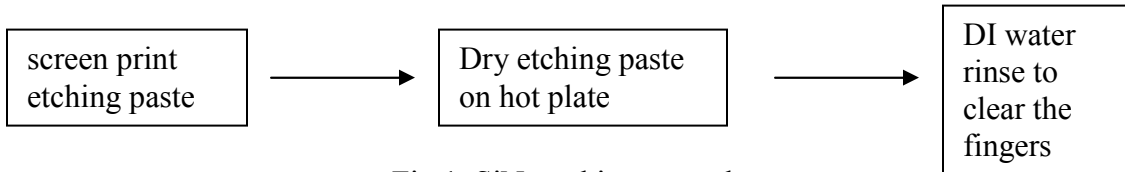Fig.1. SiN_x etching procedure

This was followed by the screen-printing of a commercial Aluminum paste and dry before firing in a belt furnace for back contact/BSF formation. Finally, we plated nickel on the front windows followed by light induced silver plating to thicken the fingers and reduce finger resistance. The cells were then isolated in $4cm^2$ before light current voltage measurements.

Characterization of finger opening through the silicon nitride with etching paste

For successful plating of nickel metal to a desired phosphorus surface concentration, the continuity and uniformity of the finger opening and surface finish are critical. The openings must be completely etched of the silicon nitride and the residue from the etching paste because electroless nickel plating requires a hydrophobic silicon surface. If the openings are not completely clean the plated nickel layer will not adhere. We observed, drying the paste immediately after it is printed provides the best results with the narrowest fingers. Figures 2a and 2b show the two cases with poor and good finger openings.
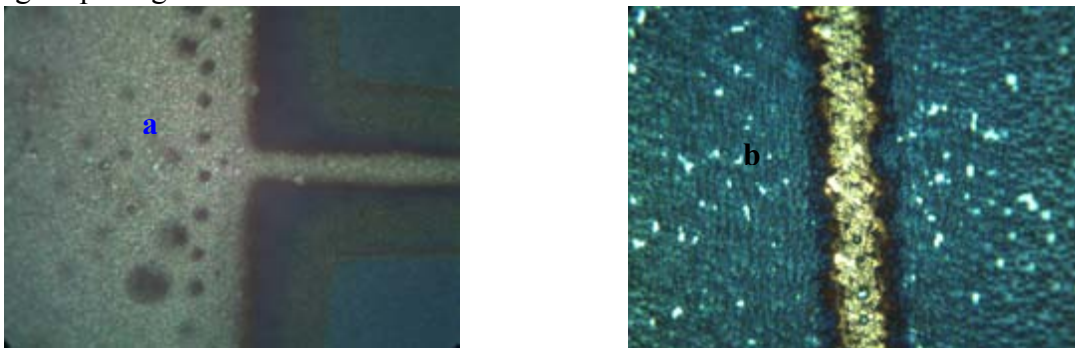
Figs. 2a and 2b: Example of a poorly and properly etched fingers

Electroless nickel plating and nickel silicide (NiSi) formation

As noted in the previous section, the silicon surface must be hydrophobic to ensure the plating and adhesion of the nickel metal. The poorly opened finger as shown in

Fig. 2a will result in plated and pealed nickel metal while Fig. 2b will lead to well plated contact.   Fig. 3 depicts a well plated contact such as resulted in the formation of the NiSi study shown in Fig. 4.
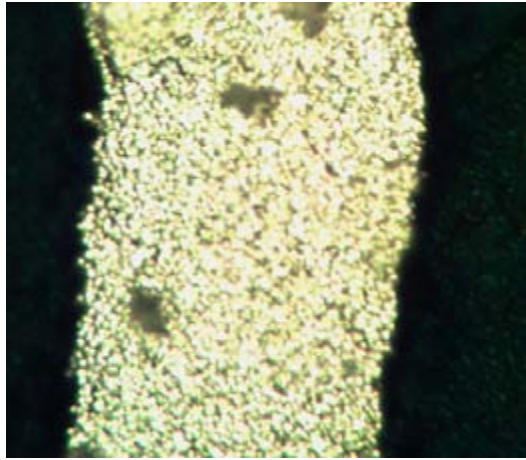

Fig. 3: Well plated Ni/Ag contact

There are three types of nickel silicide, $NiSi_2$, NiSi and Ni_2Si according to the anneal temperature. Ni_2Si forms at lower temperature than NiSi and $NiSi_2$. However, NiSi is preferred to the other two silicides because it has the lowest sheet resistance and therefore the lowest contact resistance to silicon. $NiSi_2$ is particularly undesirable because it consumes more silicon than NiSi or Ni_2Si since it is formed at higher temperature. More so, the contact is driven towards the junction, which can easily shunt shallow emitters as observed with screen-printed fired contacts. Therefore, in this work we use the rapid thermal processing system to characterize the nickel silicide formation based on the anneal temperature.

To find the optimal conditions for nickel silicide formation on n-type <111> silicon, twenty four samples were diffused, plated and then annealed over a range of temperatures from 250-800°C. The sheet resistances of the plated nickel layers were 10-15Ω/□. The sheet resistances of the nickel silicide layers were measured before and after a selective etch that removes nickel but leaves NiSi. The results are shown in Figure 4. There were considerable differences in the measured sheet resistance before and after etching for anneal temperatures below 450°C. This indicates an incomplete conversion of nickel into nickel silicide. However, the sheet resistances were approximately the same before and after etching for anneal temperatures above 450°C, which indicates the nickel metal was completely converted to nickel silicide. Figure 4 demonstrates minimum sheet resistance of 3.3 Ω/□ for the nickel silicide at 650 °C. This suggests the NiSi phase since it is formed at temperature below 750°C [3] which favors the formation of $NiSi_2$.
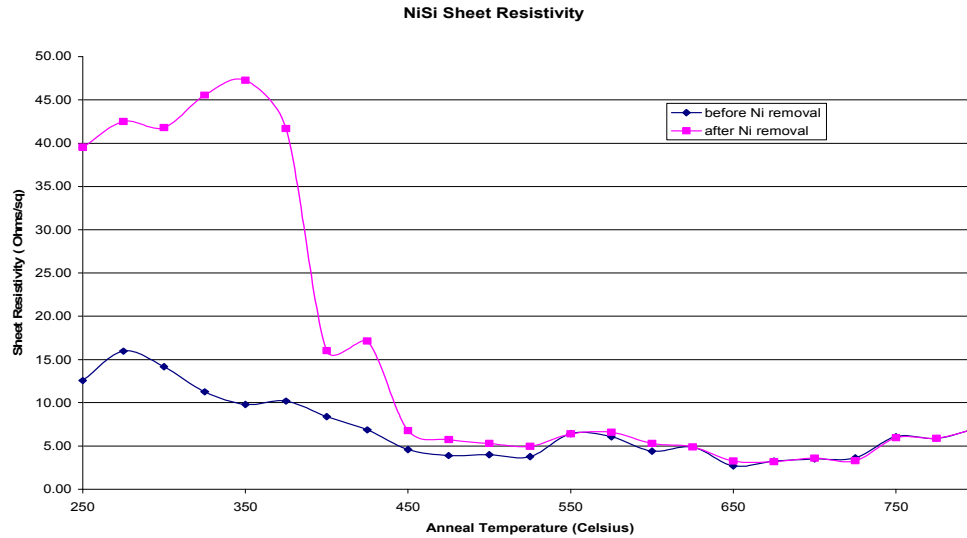
Fig.4. Ni/NiSi layer sheet resistance as a function of anneal temperature before and after a Ni Etch

Cell Results

Table 1: Electrical parameters of PCSC

V_{oc} (mV)	J_{sc}(mA/cm^2)	Fill Factor	Eff	Rshunt ohm-cm^2	Rseries ohm-cm^2	n-factor
635	37.3	71.0	16.8	9301	1.32	1.57
633	37.6	73.3	17.5	2818	0.76	1.53
636	37.9	72.7	17.5	6235	0.84	1.56
627	37.5	71.6	16.8	6676	1.23	1.44
624	37. 7	73.4	17.2	3475	0.91	1.41
628	37.7	73.0	17.3	4020	0.83	1.51
634	37.1	71.1	16.7	6949	1.38	1.49

The preliminary cell results are summarized in Table 1. As expected the short circuit currents are high as well as the open circuit voltage. However, the fill factors were low because the ideality factors are high. High ideality factor indicates recombination in the depletion region of the junction, which may lead to high reverse saturation currents (I_{o2}). The series resistance was somewhat misleading because such low values normally results in high fill factor. Despite these problems because both V_{oc} and J_{sc} are high, efficiency as high as 17.5% was achieved.

Conclusion

Plated contacts solar cells (PCSC) could be the next generation solar cell technology because of the low-cost manufacturability and higher efficiency potentials. It is possible to make high quality contacts to only the emitter region with high phosphorus concentration without compromising the shallow junction. Thus high sheet resistance

emitters with shallow junctions can be contacted to take advantage of the high open circuit voltage and short circuit currents potentials. Therefore, the cell efficiency can be improved to enhance the power generation and cost reduction of photovoltaic electricity. However, there are some challenges facing this technology that need further understanding and development. Such as the proper window opening without residue; narrow and hydrophobic emitter surface after etching, characterization of the nickel metal and anneal to establish the silicide phase and the characterization of PCSC to understand the source of high ideality factor.

Our preliminary nickel anneal temperature study revealed a minimum sheet resistance of $3.3\Omega/\square$ nickel silicide at 650°C on n-type textured silicon. This low sheet resistance at medium temperature suggests the NiSi phase, which is most desirable for good contacts. However, the PCSC we have shown here did not benefit from the optimized nickel anneal, which led to low fill factors. Despite this deficiency, we have demonstrated efficiencies in excess of 17% for PCSC. Future work will involve high sheet resistance emitters employing the optimized NiSi formation to raise the fill factor.

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[3] J. Foggiato, W. S. Yoo, M. Ouaknine, T. Murakami and T. Fukada, *Materials Science and Engineering B,* ***114-115****, 2004, p.56-60.*

A NOTE ON EDGE PASSIVATION MECHANISMS OF
N/P MESA DIODES THROUGH MODELING

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Abstract

The edge conditions of small-sample n-p junction diode and a mesa diode used for characterizing crystalline silicon substrates were modeled with a commercial finite element software package. The results of our calculations show that an increase in the positive surface charge along the vertical edge of the small diode and the mesa diode causes the edges to become depleted and then inverted as the charge on the edge is increased. This results in a higher forward biased dark current at low voltages and is a result of resistive shunting from the junction to the back contact along the passivating edge. As the edge becomes inverted, carrier recombination around the edge of the device increases, which results in more dark current. When a back surface field is incorporated into the model of the small-sample diode, the opposite effect occurs. The influence of a passivating edge on the illuminated characteristics of the small-sample diode was also simulated. Increasing the surface charge decreases the open circuit voltage and fill factor if a back surface field is not included. In simulations where the back surface field was incorporated, the short circuit current, open circuit voltage, and fill factor all improve with the largest fixed edge charges. Dark and illuminated simulations of the mesa diode are more complex because of the affects of two additional passivating surfaces due to its geometry. However, the results of the dark and illuminated simulations of the mesa diode without a back surface field are similar to the behavior seen in the small-sample diode.

Introduction

Mesa diode arrays are a highly effective way to make spatially resolved current vs. voltage measurements of crystalline silicon solar cells under dark and illuminated conditions. They have been successfully used in the past for determining the effect of dislocation density on the dark-current characteristics, and the effect of a backside hydrogen implant on the open-circuit voltage [1,2]. It is known how to provide a well passivated edge to make mesa diode arrays [1]. However, the limitations and requirements of the edge conditions have not been quantified. The following will present the results of computer simulations of a small-sample n-p junction diode, including a discussion of our results to work performed by another group [3], and a set of dark and illuminated simulations for a mesa diode based on its actual size and geometry.

Summary of Computer Model

To determine the effect that edge conditions have on the operation of an n-p junction diode, we formulated a computer model using commercial finite-element software, COMSOL Multiphysics. This software package solves a wide range of partial differential equations using the finite-element method. We used it to find a self-consistent solution to the continuity equations for electrons and holes coupled via Poisson's equation. The electron and hole currents were modeled using the drift-diffusion equations. The independent variables were the electric potential, electron concentration, and hole concentration, which are different than what are typically used. Namely, the imrefs for electrons and holes are used instead of solving directly for electron and hole concentrations. However, using the weak form of the finite-element method, we can calculate highly precise fluxes at the boundaries and we did this to obtain the current density vs. voltage curves. Also, the model was formulated in axially symmetric two-dimensional (2-D) space. COMSOL Multiphysics casts the system of partial differential equations in cylindrical coordinates and states that the solution is invariant in the radial direction. This reduces the problem from three dimensions to two. We performed initial simulations on a small diode to gain insight into the operation of the diode, particularly its behavior near the junction adjacent to a passivating surface. Furthermore, performing simulations on a smaller device used less computer time and resources. Therefore, after simulations on a smaller device performed predictably, we performed simulations of the mesa diode because they were much more intensive computationally.

Results of Small-Diode Simulations

The first set of simulations was performed on a simple n-p junction diode having a radius of two microns and a depth of five microns. The top and bottom segments were modeled as metal contacts. The left segment was the line of axial symmetry. Lastly, the right segment was modeled as a passivation layer with recombination centers and a fixed positive charge. The junction was modeled as an abrupt junction 0.5 micron below the top of the diode. Bulk recombination was modeled using a simplified Shockley-Read-Hall equation assuming all recombination centers were located at the middle of the silicon bandgap at room temperature. Figure 1 shows the dark current density vs. voltage plots when the surface charge along the right-hand segment was changed from $5x10^{10}$ C/cm^2 to $5x10^{11}$ C/cm^2. The dark current density increases with increasing charge along the edge of the device. At a surface charge of $1.5x10^{11}$ C/cm^2, small bumps appear at about 0.3 volt forward bias and they move toward lower voltages as the surface charge increases until $2x10^{11}$ C/cm^2. These bumps in current density vs. voltage curve correspond to the applied forward bias that results in the maximum surface and bulk recombination rates. This maximum occurs because the hole and electron concentration are nearly equivalent. However, as the surface charge is further increased, the dark current also increases. This is the opposite of what would be expected. As the surface charge is increased from $3x10^{11}$ to $5x10^{11}$ C/cm^2, the current density vs. voltage curves move upward, with the greatest increases at lower applied forward biases. This is typically the behavior of an electric shunt. Detailed analysis shows that the recombination rate increases in the region next to the surface charge and it extends all the way to the back contact as the edge surface charge increases.
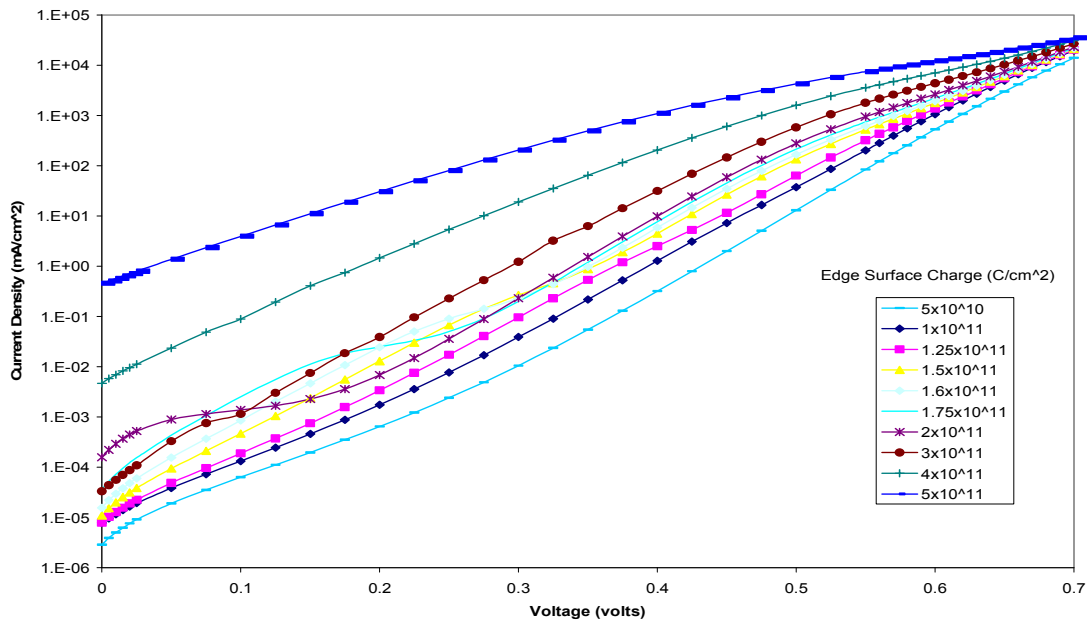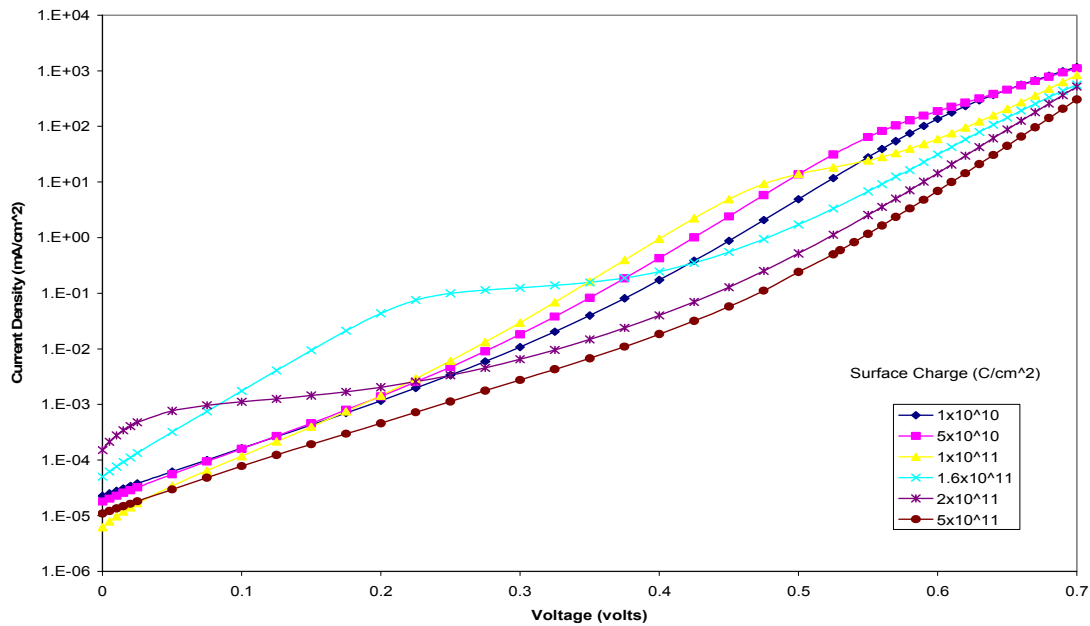

Figure 1. Small-diode simulation (dark)

In a similar study, Kuhn et al. [3] state that if the depletion or inversion region next to the fixed edge charge is continuous from the junction to the back contact, then shunting will occur. They did not have a shunting problem in the device that they modeled because a back-surface field was included. The simulations that produced the results shown in Fig. 1 were run again, but with a back-surface field that extended 0.25 micron above the bottom of the device. The results of our simulations for the small diode including the back-surface field are shown in Fig. 2. They are in good agreement with the results of simulations performed by Kuhn et. al [3]. The bumps in the current density vs. voltage curve are more pronounced indicating that the surface recombination is a more important mechanism than shunting. Also, as the surface charge increases to its maximum value the lowest dark current is achieved, and this is was one would expect. Therefore, adding the back surface field significantly reduces resistive shunting in the small diode simulated.

Figure 2. Small diode with back-surface field (dark)

As further confirmation, the diode was simulated under illuminated conditions. The generation curve was obtained by using PVOPTICS, an optical simulation software package developed at the National Renewable Energy Laboratory. It was used to determine the number of electron-hole pairs that were generated as a function of distance below the top of the device. The illuminated current density vs. voltage curves for the diode with and without a back-surface field are shown in Figs. 3 and 4, respectively. In the case with no back-surface field, the open-circuit voltage (V_{oc}) and fill factor (FF) decrease as the surface charge is increased. With a back-surface field, the V_{oc} and FF initially decrease with increasing surface charge, and then increase as the charge is further increased, reaching the best values for short-circuit current density (J_{sc}), V_{oc}, and FF. This is because shunting has been minimized and the additional positive charge pins electrons near the edge, thereby reducing the recombination rate in this area.
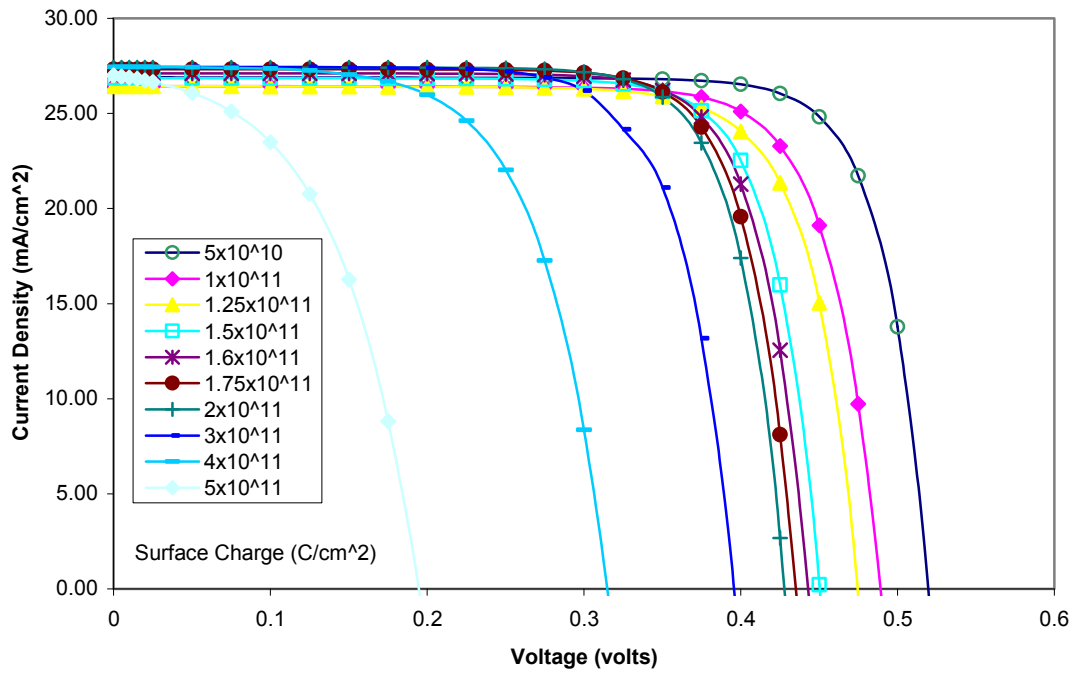
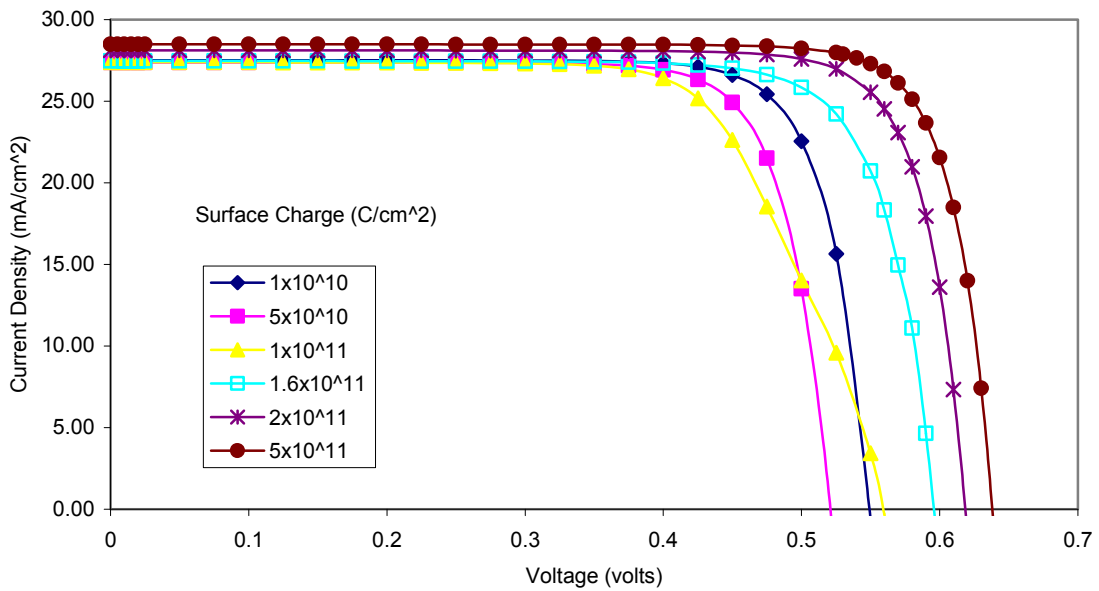**Figure 3. Small diode (illuminated)**

Figure 4. Small diode with back-surface field (illuminated)

Results of Mesa Diode Simulations

The next step was to model the mesa diode that is used for solar cell characterization. Figure 5 shows a cross section of the device. In this set of simulations, the top and step segments were modeled as

passivating surfaces with a fixed charge of $1x10^{11}$ C/cm^2, while the vertical edge of the mesa was modeled as a passivating surface whose surface charge was changed from $1x10^{11}$ to $5x10^{11}$ C/cm^2.
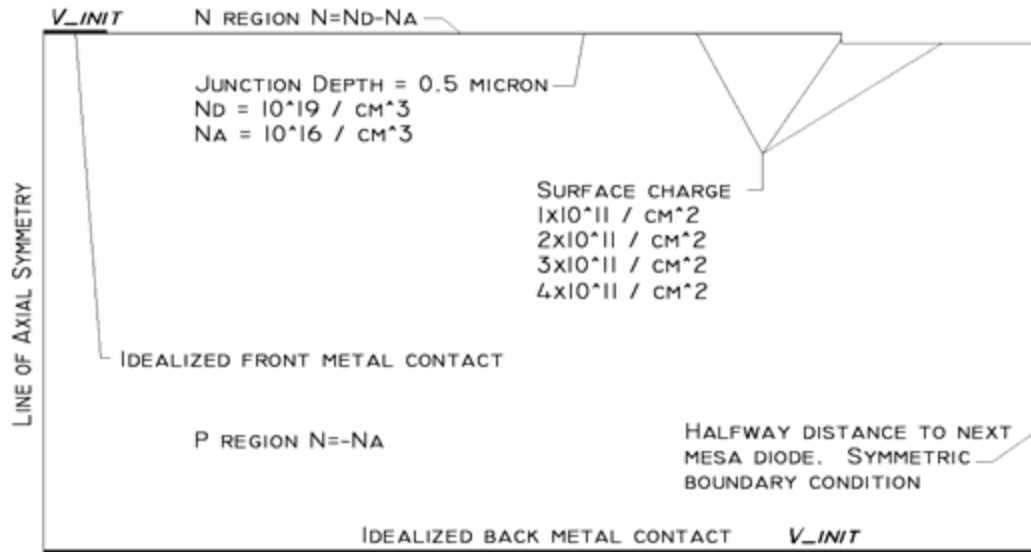

Figure 5. Cross section of modeled mesa diode

The dark and illuminated plots from the simulations are shown in Figure 6 and Figure 7, respectively. In the dark simulations, the current density increases with increasing surface charge, decreases at a surface charge of $4x10^{11}$ C/cm^2, then increases at a surface charge of $5x10^{11}$ C/cm^2. The initial increase in dark current is predominantly due to additional recombination near the mesa's edge. This is similar to behavior of the current density vs. voltage curves of the small diode without a back surface field. Also, as the surface charge is increased to $5x10^{11}$ C/cm^2, the dark current density vs. voltage increases, similar to the small diode without a back surface field. The greatest increase occurs at low voltages and is due to resistive shunting.
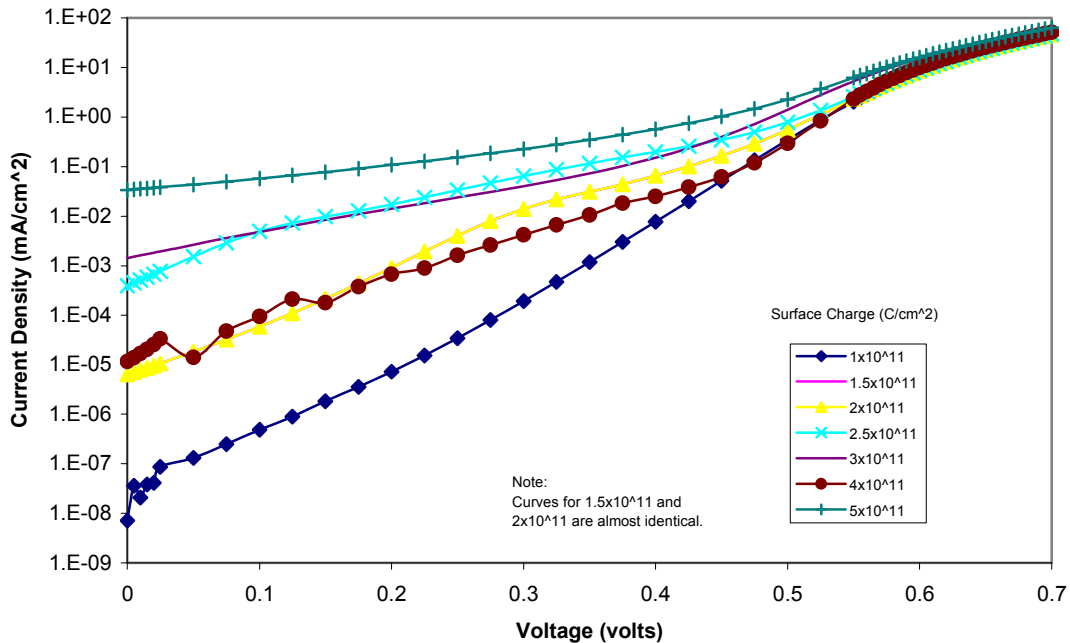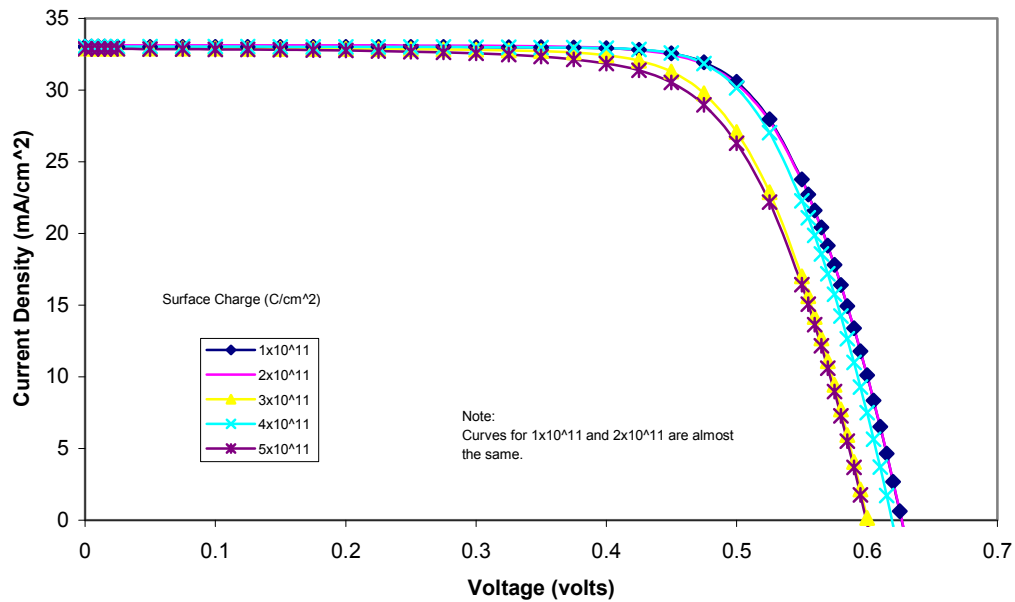

Figure 6. Mesa diode (dark)

Figure 7. Mesa diode (illuminated)

Figure 8 shows the bulk recombination rate for the entire mesa diode. It clearly shows a region of maximum bulk recombination occurs at the edge of the mesa diode and extends all the way to the back contact. This is similar to the behavior of the small diode without a back-surface field at high edge surface charges.
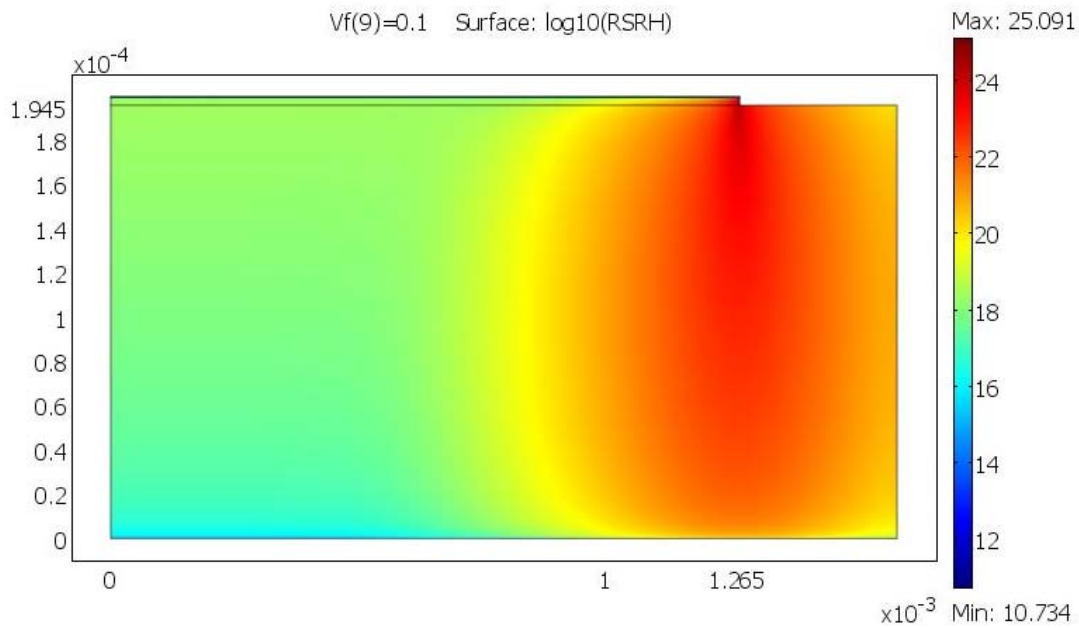

Figure 8. Logarithmic bulk recombination rate at 0.1 volt (forward bias) and 5×10^{11} C/cm^2 edge charge

Conclusions

Simulations a small n-p junction device shows that increasing the surface charge next to the junction can significantly degrade the overall performance of the device unless a back-surface field is included. In a mesa diode, which is significantly larger than the small diode modeled in this study, increasing the edge surface charge can lead to significant recombination near the edge and a region directly below it; this consequently results in shunting at higher edge surface charges. We expect that including a back-surface field in the model of the mesa diode will reduce this effect in a similar way as it does for the small diode. The results of these simulations will be presented at a later date.

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Mechanical Strength of Mono- and Multicrystalline Silicon Wafers

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Abstract

Thin silicon wafers are used for the majority of solar cells produced today. The strength behavior of such wafers has to be understood to avoid wafer breakage during manufacturing. In this work, mono- and multicrystalline wafers are characterized. Differences in strength are found to be mainly caused by the different defects due to the wafering process. The strength also depends on the orientation of the sawing marks. Roughness measurements can be correlated to the strength results.

Introduction

The silicon substrates in crystalline photovoltaics dominate the strength of the final solar cell. Substrates are available as monocrystalline or multicrystalline silicon wafers. In general the strength shows a large scattering of fracture stress values because silicon is a brittle material at room temperature. The strength strongly depends on the defects in the material, i.e. the process steps influence the fracture behavior of the wafer. Breakage of silicon wafer and solar cells is a key problem in solar cell and module manufacturing. Thus the fracture behavior is investigated in order to determine the strength and to understand the failure mechanism [1-4]. In this investigation the mono- and multicrystalline wafers are characterized using the 4-point bending test, which loads the wafer surface as well as the wafer edges.

Samples and Experiments

For this investigation (156x156)mm² wafers out of 2 blocks were characterized. One block was crystallized as monocrystalline material by the Czochralski process. The other block was manufactured as multicrystalline block by the Bridgman process. Both blocks were cut into wafers with a thickness of 200µm (± 30µm). The process parameters were similar for both types of material.
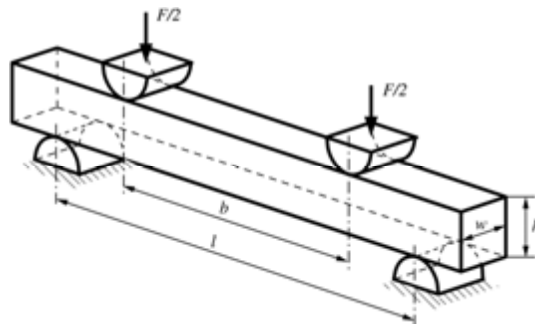

Fig. 1: Principle of the 4-point bending test

In order to characterize the wafer including the surface and the edges 4-point bending tests (see Fig. 1) were performed. The 4-point bending test is an appropriate method to characterize the strength of wafers [5]. The bending setup according to Fig. 1 with 10mm rollers had an outer

span of l=110mm and an inner span of b=55mm. The load was measured with a 500N load cell on a universal testing machine ZWICK 1445. The deflection was measured by the position of the crosshead. In the experiment the wafers were loaded with a velocity of 100μm/s until fracture occurred. For statistically reliable results, between 100 and 160 samples were tested for each batch. Due to large thickness variations every wafer was weighed before testing and an average thickness was calculated. In this investigation wafers were tested along and across the sawing marks to determine dependence on loading direction. The sawing marks due to the wire sawing process are visible as straight lines across the wafer. If they are parallel to the rollers in the 4-point bending test, the wafer is tested along the sawing marks. If the lines are perpendicular to the rollers the load is applied across the sawing marks. In Tab. 1 the batches of wafer for the different experiments are summarized.

Tab.1: Batches for strength measurements in 4-point bending test

No.	Sample Type	Loading vs. Sawing direction	Number of Samples
1	Monocrystalline silicon wafer	across	160
2	Monocrystalline silicon wafer	along	160
3	Multicrystalline silicon wafer	across	100
4	Multicrystalline silicon wafer	along	100

The experiments give the fracture force and deflection as well as the force-deflection charts. Instead of the fracture force the fracture stress, which consider differences in geometries of sample and setup, should be used to characterize the strength behavior. For every sample the fracture stress σ was calculated with equations of the linear elastic beam theory,

$$\sigma = \frac{3}{2}\frac{F}{wh^2}(l-b) \qquad (1),$$

with the total load F and the geometrical parameters of sample and setup as shown in Fig.1. Although the wafers show large deflection in the experiments, the error from using the linear approximation of Eq. (1) is rather small, as indicated by Finite Element Analysis.

The fracture stresses were statistically evaluated with the Weibull distribution. This type of statistical distribution represents the weakest link model and is commonly used for brittle materials like silicon. The two-parameter form of the Weibull distribution can be written as

$$P = 1 - \exp\left(\frac{\sigma}{\sigma_\theta}\right)^m \qquad (2)$$

The parameter σ_θ represents the characteristic fracture stress at which 63.2% of all samples fail. The Weibull modulus m is the parameter of variation, with a small value indicating large scattering and vice versa.

The roughness of the wafers was measured by profilometry with a Dektak 3030. For mono- and multicrystalline wafers 5 samples were measured respectively. Every sample was scanned along 5 mm lines, twice along and twice across the sawing direction. The results of the roughness measurements are presented by the parameter R_a, which is the arithmetic average value of the deviation from the mean center line.

Results

The results of the 4-point bending tests are shown as Weibull probability plots in Fig. 2 for mono- and multicrystalline wafers. The Weibull parameters are summarized in Tab. 2. The monocrystalline wafers show high characteristic stress values and rather small scattering. There is no significant difference in strength behavior for the different orientations of sawing marks. The multicrystalline wafers have smaller characteristic stress values and slightly smaller scattering meaning higher Weibull moduli. The orientation of the wafer shows a significant difference here. If the sawing marks are oriented along the rollers in the 4-point bending test, the characteristic fracture stress is significantly smaller compared to the stress when the sawing marks are oriented across the rollers. The roughness values in Tab. 2 are nearly the same for monocrystalline wafers for both directions along and across the sawing marks. They are smaller than for the multicrystalline wafers, which show also differences between the orientations. The roughness is higher across the sawing marks than along.

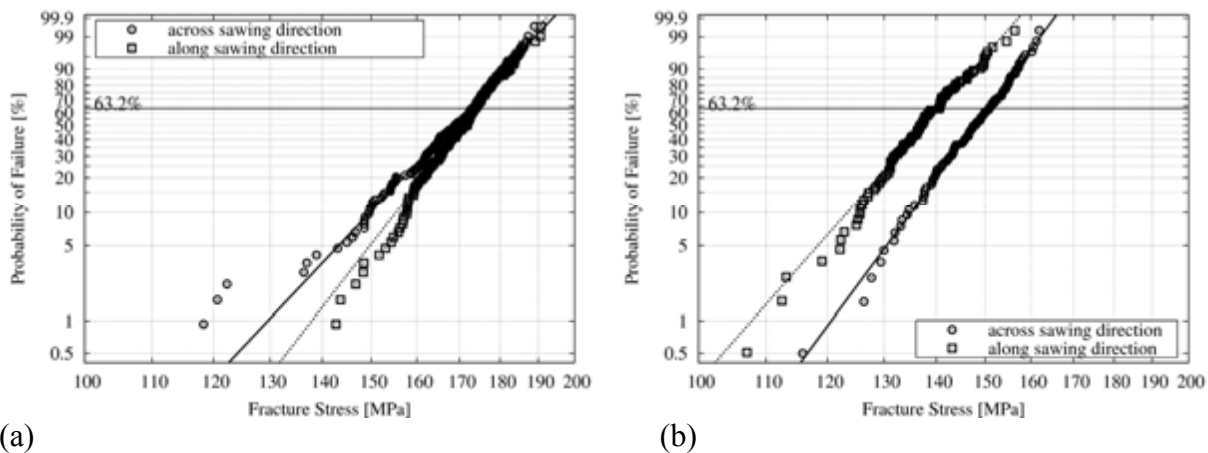(a)   (b)

Fig. 2: Weibull probability plots for different batches, which were tested along and across the sawing direction; (a) monocrystalline wafers and (b) multicrystalline wafers

Tab. 2: Summarized results of strength and roughness measurements for all tested batches with 90% confidence bounds for the Weibull parameter.

	Monocrystalline Wafers		Multicrystalline Wafers	
	across	along	across	along
Characteristic Fracture Stress [MPa]	172.2 (170.7 ... 173.6)	174.2 (173.0 ... 175.4)	150.7 (149.4 … 151.9)	140.6 (139.2 … 142.1)
Weibull Modulus [-]	16.2 (14.5 … 17.8)	19.7 (17.6 … 21.6)	20.7 (17.9 … 23.3)	17.3 (14.9 … 19.4)
Roughness R_a [µm]	0.39 ± 0.03	0.41 ± 0.07	0.76 ± 0.14	0.58 ± 0.07

Discussion

The results of strength measurements of mono- and multicrystalline wafers show differences between the types of wafers as well as the orientation in loading. The roughness can be correlated to this behavior. While monocrystalline wafers show higher strength, the roughness is much smaller compared to multicrystalline wafers. The roughness of wafers can qualify the strength of

the wafer as described in [6]. Although the roughness cannot quantify the difference in strength, it helps to understand the different strength behavior. The orientation of the sawing marks influences the strength behavior of the multicrystalline wafers significantly. Due to larger saw damage the roughness is increased resulting in lower fracture stress and strong orientation dependence. For monocrystalline wafers the roughness is smaller, which indicates less saw damage. This leads to higher fracture stress and smaller influence of the sawing mark orientation.

The results indicate that the strength of mono- and multicrystalline wafer is more dominated by the wire saw process than the crystal structure of the wafers. Although multicrystalline wafers have intrinsic stress due to the manufacturing process and multiple defects, which can cause fracture, the strength is smaller but still in the range of the monocrystalline wafers. Furthermore it should be noted that the 4-point bending test characterizes nearly the whole wafer including the surface and the edges. Therefore the strength behavior should also be investigated with other test methods like the ball-on-ring test to exclude the effect of the edges. Results of both test methods can give a more comprehensive view of the strength behavior of mono- and multicrystalline silicon photovoltaic wafers.

Conclusions

Monocrystalline and multicrystalline silicon photovoltaic wafer are brittle substrates whose strength behavior is strongly influenced by the manufacturing process. It was shown that the strength of the wafer mainly depends on the saw damage and less on crystal structure, intrinsic material defects, or intrinsic stress. The strength of wafer with large saw damage and sawing marks depends also on the orientation of the marks.

Acknowledgement

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Challenges and Potential Solutions at Making High-Performance Cells from Low-grade Si Feedstock

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Matthias Heuer, Anis Jouini, Alain Blosse,
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(Paper not available)

A Technique for Rapid Cross-Sectioning of Si Solar Cells with Highly Planar, Damage-Free, Edge

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Abstract

We describe a technique for producing highly planar, damage-free, cross-sections of Si solar cells. This technique uses a wax mounting procedure, which allows formation of a predetermined shape of wax to support the sample. Damage-free cross-sections are produced by using only chemical-mechanical polishing with optimized pressure. Cross-sections are suitable for carrying out high-resolution analyses of various interfaces of solar cells.

Mechanism of Hillock Formation during Chemical-Mechanical Polishing of Multicrystalline Silicon Wafers

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Abstract

Chemical-mechanical polishing of multicrystalline Si wafers can produce an intriguing defect, which we have termed "hillocks." We have investigated the conditions under which hillocks can appear and determined the polishing conditions that can prevent their formation. This paper describes a mechanism of hillock formation, and explains all the experimental observations that relate to the shape of hillocks and the characteristics of grains in which they appear.

Migration of Hydrogen in Silicon from PECVD SiN$_x$ Films

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Abstract

Hydrogen (H) released during the annealing of hydrogenated amorphous silicon nitride (SiN$_x$:H) films diffuses through the crystalline silicon and passivates the defects. This study shows that the stable H isotope deuterium (D), which is released during the annealing of deuterated amorphous silicon nitride (SiN$_x$:D) films, diffuses through the crystalline silicon and is subsequently captured by a thin, highly defective amorphous layer of silicon (a-Si) sputtered on the rear surface. The penetrated deuterium (hydrogen) concentration was measured by secondary ion mass spectrometry (SIMS) to monitor the flux of D diffusing through a defect-free single-crystalline silicon wafer. The penetrated D content in the trapping layer increases with the annealing time and temperature. The flux of D injected into the silicon from the SiN$_x$ layer decreases as annealing time increases. The measured flux was correlated with lifetime measurements on defective Si to show that higher flux of H during the short RTP anneal is crucial for enhanced hydrogenation of the defects in Si.

1. Introduction

The H concentration in Si is very low and usually below the detection limit [1-3]; therefore, the positive effects of H released from hydrogenated SiN$_x$ (SiN$_x$:H) film during high-temperature annealing (hydrogenation) have been observed and reported mostly via indirect measurements such as the increase in minority carrier lifetime [4] and improved current-voltage and spectral response of solar cells [5,6]. Not long ago it was conjectured that the H lost from the SiN$_x$:H film after annealing was released into the atmosphere and not into the Si [7]. However, infrared absorption measurements of Pt-H complexes in Si have recently demonstrated a large diffusion depth of H and placed a lower limit on the total amount of H diffusing into the crystalline Si (c-Si) samples [1]. In this study we peformed secondary ion mass spectrometry (SIMS) measurements of D that was released from the deuterated SiN$_x$ (SiN$_x$:D) film and "penetrated" through a defect-free c-Si wafer during rapid thermal annealing (RTA) at 750 and 800 °C for different times. This enabled us to determine the average flux of H diffusion through thick c-Si samples and to correlate it with the lifetime enhancement of defective Si samples.

2. Experimental

80 nm thick SiN$_x$:D was deposited on the front side of 215 µm thick float zone (FZ) wafers, with a resistivity of 0.35 Ω·cm using deuterated silane (SiD$_4$) and deuterated ammonia (ND$_3$) as precursors in a low-frequency plasma-enhanced chemical vapor

deposition (PECVD) reactor at 400 °C. rf sputtering was used to deposit 1.5-2.5 μm defective amorphous Si (a-Si) films on the rear side of the wafer in an argon environment at a substrate temperature of 200 °C. Samples coated with SiN_x:D on one side and a-Si on the other side were annealed in a Rapid Thermal Processing (RTP) system at 750 and 800 °C for 1, 5, 60, and 300 s, with fast ramp-up and ramp-down rates, similar to the contact firing profiles used during solar cell fabrication. SIMS measurements of D profiles were performed within the sputtered Si films with a Cameca IMS5f using a cesium primary ion beam.

Migration of hydrogen in the silicon bulk

Figure 1 shows the structure used to trap D and the D concentration profiles in the sputtered Si layer on the rear side of the FZ samples annealed at 750 °C. The peak D concentration in the sputtered Si film for 1, 5, 60, and 300 s annealings were found to be 3.84×10^{18}, 4.43×10^{18}, 5.23×10^{18}, and 7.87×10^{18} cm^{-3}, respectively. Figure 1 also shows the D content in the sputtered Si layer for a sample that had no SiN_x on the front and was coannealed with the 300 s sample. No D was detected in this sample, which establishes that the source of D detected in sputtered Si is the SiN_x:D film on the front side and that D gets there via diffusion through the c-Si wafer. The concentration of the trapped D increases in the sputtered Si layer as the annealing time increases, but the increase is limited by the supply of D from the SiN_x:D film. The D concentration inside the sputtered Si layer shows a typical diffusion profile with a tail away from the c-Si/ sputtered Si interface decreasing toward the free surface. This indicates the diffusion of D through the c-Si and into the sputtered Si, rather than diffusion from the ambient. As expected, in the absence of traps, the D concentration rapidly falls below the detection limit inside the FZ Si.
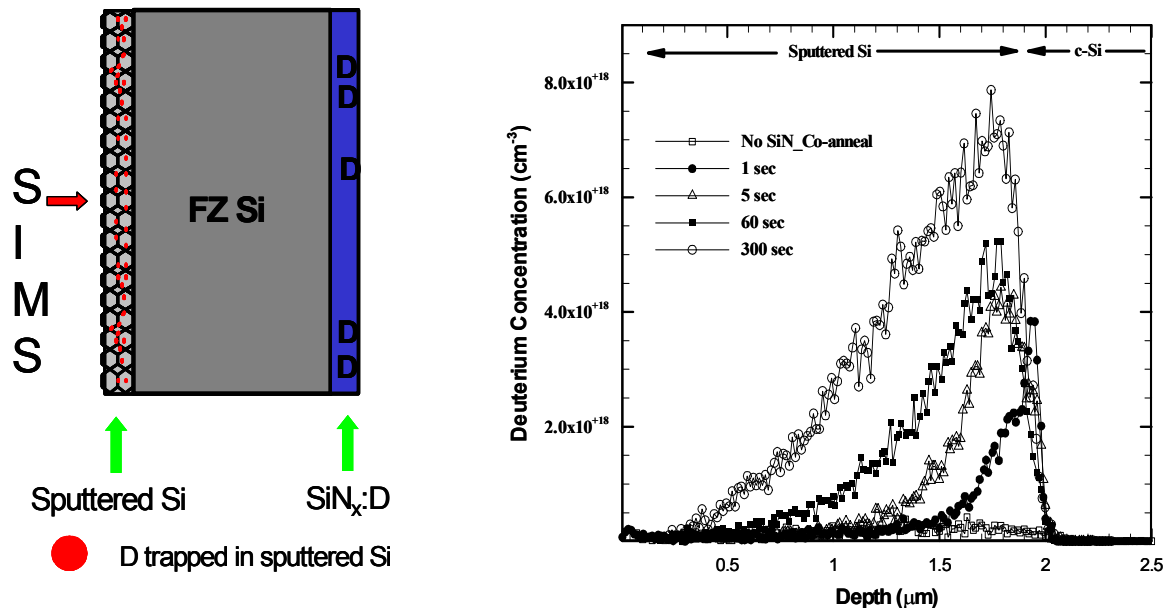

Figure 1: Penetrated deuterium concentration in the sputter Si layer on the back of the wafers, released from the front SiN_x:D film, for times of 1, 5, 60 and 300 s at 750 °C in RTP.

Figure 2 shows the D concentration in the sputtered layers for a higher annealing temperature of 800 °C and for times of 1, 5, 60, and 300 s. As opposed to the 300 s annealing at 750 °C, the D starts to escape from the rear surface for 800 °C sample which was annealed for 300 s. As expected, much higher concentrations of D is measured at the higher annealing temperature of 800 °C compared to 750 °C.
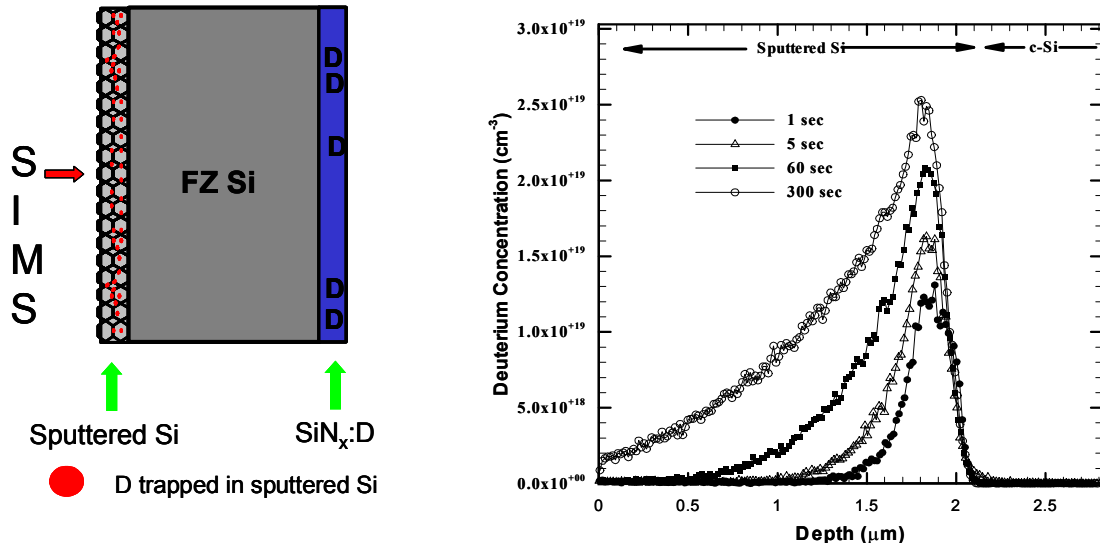

Figure 2: Penetrated deuterium concentration in the sputter Si layer on the back of the wafers, released from the front SiN_x:D film, for times of 1, 5, 60 and 300 s at 800 °C in RTP.

Average flux of deuterium injected in silicon from SiN_x

Further analysis was done on the penetrated D concentrations for annealing temperature of 750 °C. Figure 3 shows the average "areal density" of D (integrated area under the concentration curves) in the sputtered Si layers for the 750 °C anneal. Notice that the areal density increases, but its slope decreases with the increase in annealing time. This suggests a rapid decrease in the rate of release of D from the SiN_x:D film. This is consistent with some observations in literature, where it has been suggested that the total H content and also the Si-H and the N-H bond densities in the SiN_x:H film initially decrease at a higher rate and then slows down for longer annealing times [7,8]. Thus, the merit of measuring the penetrated or diffused H through the defect-free Si in this study is that it provides a measure of H that would be available for defect passivation if SiN_x:H were deposited on top of a defective Si substrate. This is a much more useful quantity than measuring the loss of H from the SiN_x film, which would also involve H escaping from the front surface to the ambient. From the areal density of the trapped D, the average flux (areal density divided by annealing time, in $cm^{-2} \cdot s^{-1}$) of D diffusing through the Si has been estimated and plotted in Fig. 3.

Hydrogen passivation of defective silicon bulk

After establishing the incorporation of H into the Si bulk, the retention of H at the defects was also studied. As-grown String Ribbon wafers, which are very sensitive to hydrogenation, were gettered with $POCl_3$. Lifetime measurements were performed after
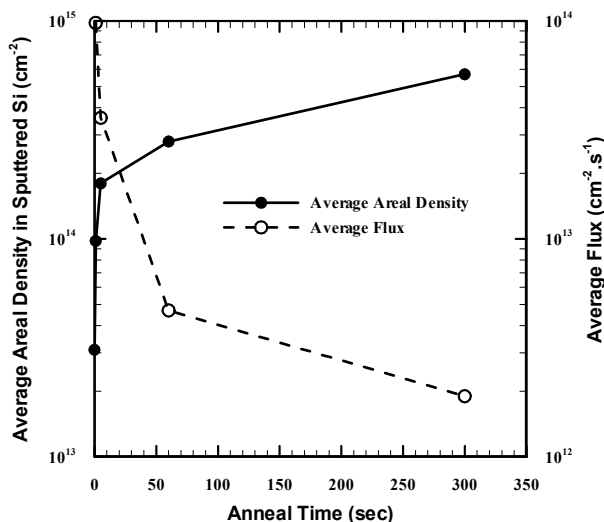
Figure 3: Average areal density of D in the sputter Si film for different annealing times and the average flux of D injected in the Si is also shown.

etching off the emitter and then a 80 nm thick low-frequency SiN_x:H film was deposited on these samples for hydrogenation study. To study the effect of annealing time only, the cool-down rate was kept constant for all annealing times. Bulk lifetime was then measured after 1, 5, 60 and 300 secs anneals, with similar cool down profiles for all times. Figure 4 shows the correlation between the measured lifetime and the average D flux (Fig. 3) for different annealing times.

The average flux values for the shorter annealing times are substantially higher relative to the longer annealing times. It is important to recognize that a higher flux of H during a shorter annealing enhances defect passivation in the Si bulk. For longer annealing times the average flux of H decreases, which in turn would decrease the ratio of the hydrogenated to the dehydrogenated defects. Therefore, a smaller fraction of defects will be in the passivated state just before the start of the cooldown cycle, resulting in inferior defect passivation even though the total amount of released H from SiN_x:H increases. This is because hydrogenation and dehydrogenation are both taking place at the same time and the dehydrogenation rate is fixed, hence the net hydrogenation is dictated by the average flux rather than the total amount of H passing through the Si. If however no dehydrogenation is taking place, then lifetime for longer annealing times would be better. Hence, 1 s firing produces maximum flux and highest lifetime. For longer annealing times, the flux of H decreases and consequently H passivation and bulk lifetime is reduced.

4. Conclusions

D released from the PECVD SiN_x:D film on top of a Si substrate penetrates through the entire Si wafer. The single-crystal Si wafers are highly transparent to D diffusion. Therefore, a significant amount of the released D is captured by the sputtered Si layer on the rear side of the sample at annealing temperatures of 750 and 800 °C and for annealing time as short as 1 s. The flux values for various annealing times were correlated with the lifetime enhancement of defective String ribbon Si wafers. It was

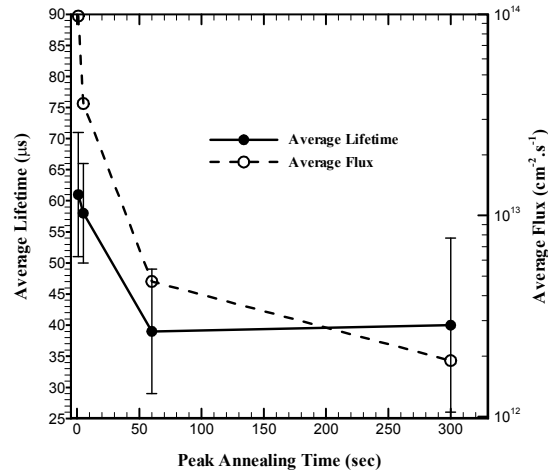found that a higher flux for shorter annealing times leads to an enhanced defect passivation in low-cost Si.

Figure 4: Average lifetime and average flux values for peak annealing times of 1, 5, 60 and 300 s.

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