Optimization Design and Simulation for a Band-Pass-Filter with IPD Technology for RF Front-end Application

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***Abstract*—A band-pass-filter (BPF) based on silicon substrate was designed and simulated. Different software was applied to design and simulate the character of the filter. A three-order filter was designed dedicating to range 2.4 GHz-2.5 GHz use. The ideal topology circuit was designed with passive inductors and capacitors. Moreover, the integrated passive devices (IPDs) were modeled and simulated with thin film process. To enhance the performance of the IPD, some typical factors were considered to optimize the physical model. The IC design tool and electromagnetic simulation software were used and compared to analysis the character of the filter, which demonstrated that the BPF can be applied to RF front-end system.**

Keywords—2.5D interposer; Integrated passive devices (IPD), Band-pass-Filter, inductor andcapacitor

I. INTRODUCTION

In a wireless communication system, there are many kinds of passive modules, such as LCs, filters, baluns and duplexers. These passive components cover 60%-70% of the area in the board. These passive components can be made in various substrate and process, such as ceramic, lamination, silicon and glass [1]. There is clear indication that the overall size-reduction relies heavily on the reduction of these passive components. Conventional discrete passive components are the most widely used for wireless products, which are typically made using ceramic technology for ceramic's good electrical and thermal characteristics [2][3]. However, integrated passives devices (IPDs) based on semiconductor processes offer the advantage of excellent parameter control, and allow simplified and compact module design IPD processes can be used to make high density capacitors high Q inductors and large value resistors [4].

IPD technology based on Silicon wafer process has been in great interest in the past decade. The process of thin film IPD is well familiar to the semiconductor industry. Since the silicon interposer which through the though silicon via (TSV) and the redistribution wiring (RDL) layers of the silicon has been proposed and applied to the typical electronic products packaging, and due to its unique technology materials and processing technology[5][6]. It is widely used and recognized in the industry. However, it is not enough for only TSV and RDL in the interposer, especially applied on radio frequency (RF) integrated system. There are many passive devices integrated in RF circuits, like capacitor, resistor and inductor. The fabrication of high factor (Q) inductor and high density capacitor are the important task to be solved imperatively for silicon interposer. Fig.1 shows the smart interposer which integrated TSV and integrated passive devices (IPDs), which can be widely used for high density RF systems[7][8].

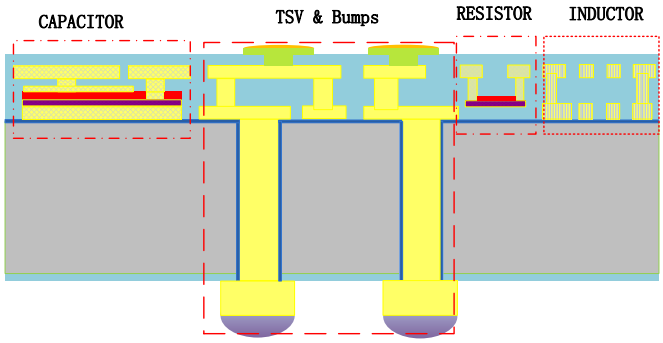


Fig. 1. The structure of smart interposer integrated TSV and IPD

In this paper, we designed the IPD in the 8 inch silicon wafer. BPF from 2.4 GHz to 2.5 GHz (10dB return loss bandwidth) is designed using IPD technology on a silicon substrate for RF front-end applications. The filter shows 2 dB insertion loss from 2.4 GHz to 2.5 GHz. The size of the filter is 2mm×2mm×0.5mm including bump height. The high resistivity silicon wafer (2KΩ.cm) is used because it can obtain high Q inductor (35 at 2 GHz) on silicon wafers. To obtain the character above, we modeling and optimization the elements of a three order Chebyshev filter. In last part of the paper, it simulated the whole circuit with layout which illustrates the filter can meet the application.

II. MODELING AND OPTIMAZATION FOR ELEMENT

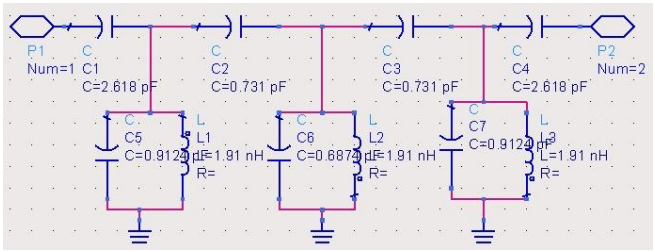
To meet the requirement on wireless communications system, the 2.4 GHz band passive module (such as filter, balun and duplexer, etc.) are widely applied on RF front-end of the electrical products. BPF is a kind of important passive device which used in the ZigBee, Bluetooth and WiFi .The target of the design of the filter is shows as follows: (1). Bandwidth(BW):400-2500 MHz; (2). f_0=2.5 GHz; (3). Low

insertion loss < 3 dB; (4). High rejection @ 1 GHz > 35 dB; (5). Return loss> 14 dB

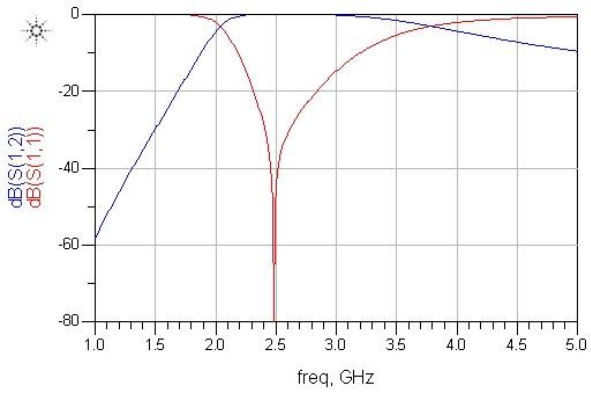
A. The Ideal Schematical Model

In order to design a passive BPF, we should choose a proper type of filter. There are many kinds of filters that Butterworth filter and Chebyshev filter are the most commonly used in the circuit. Butterworth filter in the pass band has a smooth inside and outside the amplitude-frequency characteristics, but there is a longer transition period which is likely to cause distortion. Compared with the Butterworth filter, Chebyshev filter transition band is narrow, but the internal amplitude-frequency characteristic is very unstable. Cause the target filter need a high rejection, we choose the latter one.

The next one is to determine the order of the filter. The order is smaller, the amplitude ripple is bigger. However, the order is bigger, the circuit is more complex and difficult to optimize. After calculate and trade-off consideration, we used three-order BPF which is shown in Fig.2（a）. It shows that there seven capacitors and three inductors in the circuit. Each element of the passive component is ideal model. The inductance of the inductor is 1.91nH，and the capacitance is also shown in the picture. Fig.2（b）is the result of the s parameters for the circuit in Fig.2（a）, which illustrates the high rejection can reach -50dB. The other features of the filter can meet the demand of the design.



(a) The circuit topology for the 3-order BPF



(b) S parameters of the ideal circuit topology

Fig. 2. The circuit model of the filter with simulation results

B. 3D Model Simulation for Inductors

In the ideal circuit model, it determined the value of the inductor is 1.91nF. There era parasitical resistance, inductance and capacitance for a inductor based on silicon. The impedance is increase with the frequency, which is the reason for the big loss under high frequency. To get a high Q inductor with precise inductance need to consider the shape for a spiral inductor. Spiral inductance and geometry are closely related, their accuracy can be obtained by solving Maxwell's equations. For the quadrilateral, hexagon and eight octagonal spiral inductor, \can be calculated from the following formula(1):

$$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + k_2 \rho} \tag{1}$$

Where, K1、K2 are constants for different turns, which are shown in the Table.1, μ 0 represents magnetic conductivity，n represents turns，d_{avg} represents an average value for inner diameter and external diameter, ρ represents filling rate of turns，which formula is(2)：

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{2}$$

TABLE I. THE VALUE OF K1 AND K2 WITH DIFFERENT SHAPES

Shape of the inductor	Quadrilateral	Hexagon	Octagon
K_1	2.34	2.33	2.35
K_2	2.75	3.82	3.55

Cause octagonal inductor can get a high Q and easily to fabricate， we choose octagonal inductor to modeling and simulation. Fig.3 shows a typical image of the layout for a octagonal spiral inductor. In the image, it can see that the diameter 2R, line width W, line separation S and turns form the mainly structure parameters.

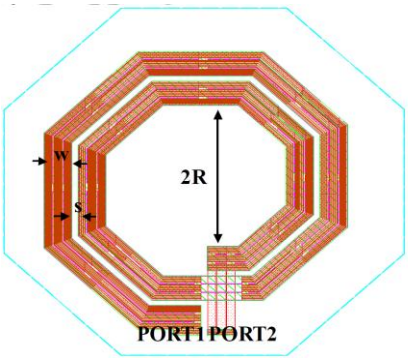
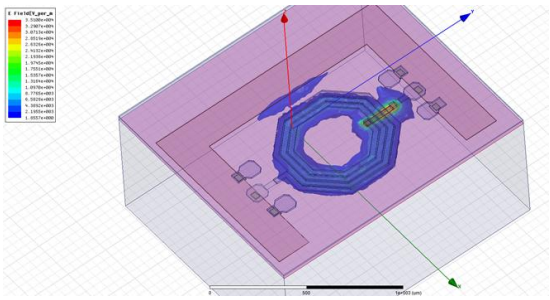


Fig. 3. The layout for a spiral inductor

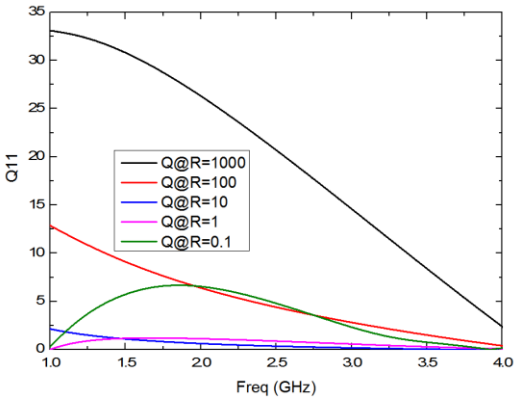
TABLE II. PARAMETERS OF THE MATERIAL

Material Name	Relative Permittivity	Bulk Conductivity (S/m)
IPD-Al	1	34800000
IPD-Cu	1	57000000
IPD-PI	3.16	0
IPD-silicon	11.9	0.1-1000

We used the 3D electromagnetics simulation software HFSS to set up the model of inductor.TABLE2 given the material name and characteristic parameters with them, which used in the software. It chooses aluminum as metal pad, plated copper to form thick spiral, and cured resin PI to insulation. The silicon substrate is changed by bulk conductivity from 0.1-1000 s/m. Fig.4(a) shows the model of the inductor with the distribution of surface field. It illustrates the position of maximum surface electric field is the connection of two metal layers. The ground of the inductor also induced the leakage current. Fig.4(b) is the simulation of the results between the Q and the bulk resistivity from 1 GHz to 4 GHz. Apparently, the Q is higher with the bulk resistivity is increasing. When the bulk resistivity is above than 1000 Ω .cm, the Q can reach 20 at 2.5 GHz. Fig.4(c) is the



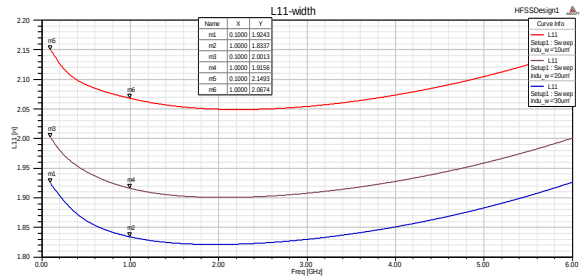
(a) Simulation models for 3D structure



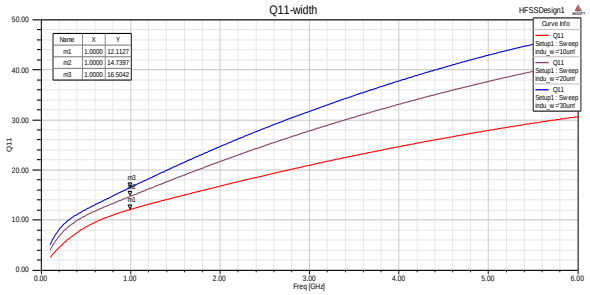
(b) Simulation results for Q change with bulk conductivity

Fig. 4. Simulation model and simulation results of 3D structure

Line width is also considered to model the inductance and Q of the inductor besides the bulk resistivity. It fixed the radius at 0.1 mm, line thick at 0.3 mm, the turn at 2 and changed the line width from 10 um to 30 um. Fig.5(a) shows simulation results for relation among the inductance, Q and line width. It illustrated the line width is smaller, the inductance is decrease. For example, when the W=10um, L=2.0674nH; W=20um, L=1.9156nH; W=30um, L=1.8337nH. (@f=1GHz). The Q is getting higher as line width increases, which is shown in the Fig.5(b). The bigger the line width，the higher the Q value. Cross section of metal is getting bigger as the line width increases, thereby resistance decreases and the Q value increases. Increase of line width also affects integration and increases parasitic capacitance, so as to affect operation frequency and increase coupling between inductance and substrate, which decrease the Q value.



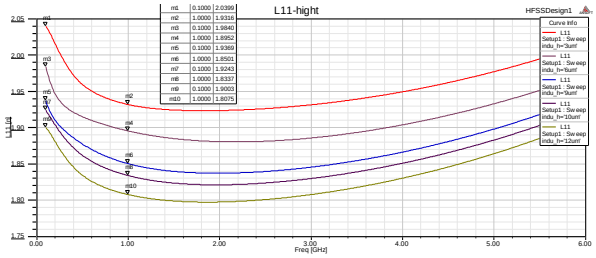
(a) Inductance changed with different line width



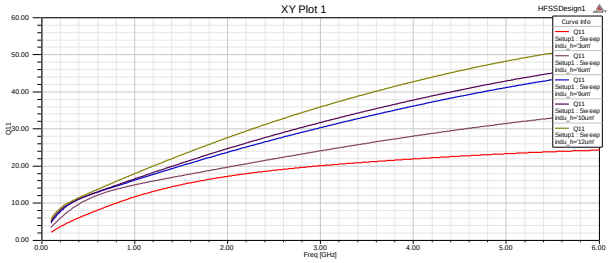
(b) The Q factor changed with different line width

Fig. 5. The inductance and Q changed with the line width

Diameter of inductance 2R is 0.1mm, external diameter is 0.3mm, line width is 30um, and line width is changed with 3-12um to do simulation calculation. Referring to Fig.5(a), corresponding inductance increasing as line width increases, and in a case that the line width is 9 um, change of the inductance is smallest. Referring to Fig.5(b), the Q value is increasing as the line width increases since increase of the line width leads to decrease for resistance of turns which causes decrease for loss of turns.



(a) Inductance changed with different line thicknes



(b) The Q factor changed with different line thickness

Fig. 6. The inductance and Q changed with the line thickness

C. 3D Model Simulation for Capacitors

The capacitor based on silicon is also simulated in HFSS. Fig.7 shows cross-section of the 3D model of the capacitor. It used the MIM capacitor with the a thin dielectric layer. In the model, it utilized Si_3N_4 as the dielectric here and aluminum as pad metal to finish the simulation. There are some simulation results show as follows:

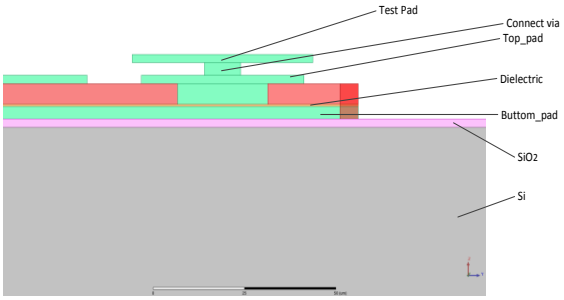


Fig. 7. Cross section of the 3D model of a capacitor in HFSS

Ⅰ）Scalable the bulk resistivity：0.1-1000 siemens/m

In Fig.8, it can be seen from the simulation result, change of substrate conductivity has little effect on capacitance and quality factor Q value, since main factors for affecting capacitance performance, which has little connection of substrate, are loss for metal and dielectric, and parasitic inductance in inner part of inductance and capacitance for input and output ports.

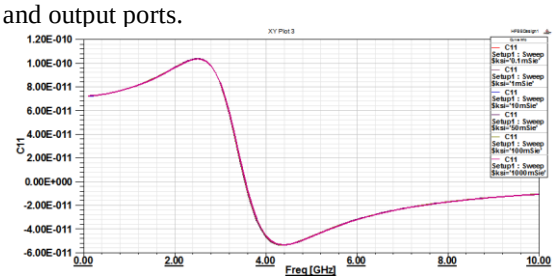


Fig. 8. The capacitance changed with the bulk resistivity

Ⅱ） The thickness of SiO2 layer：0.2 um-10 um

In Fig.9, change of thickness for an oxide layer has little effect on capacitance and quality factor Q value, since the oxide layer, which is located between a bottom metal layer and substrate, does not have serious parasitic effect for the capacitance, and main factors for affecting capacitance performance are loss for metal and dielectric, and parasitic inductance in inner part of inductance and capacitance for input and output ports.

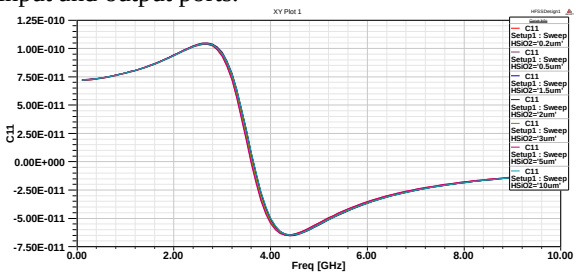


Fig. 9. The capacitance changed with the thickness of insulation layer

Ⅲ）The thickness of top metal layer:0.2 um-10 um

In Fig.10, Capacitance is increasing as thickness of bottom metal layer increases, since the edge scattering effect is enhance, which takes a parasitical capacitance. So the total capacitance is increasing. However, the edge scattering effect also causes the loss of the capacitor, which makes the Q is smaller.

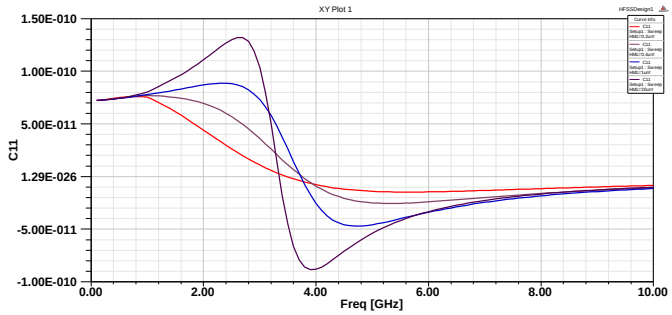
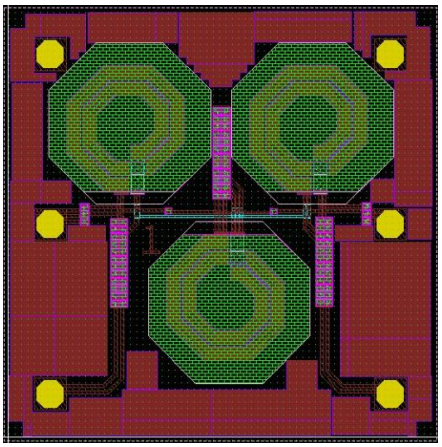


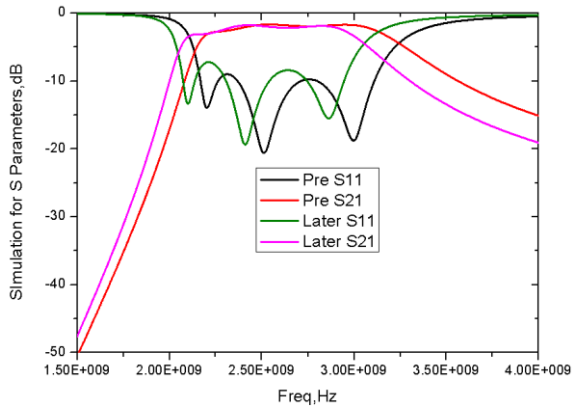
Fig. 10. The capacitance changed with the thickness of metal layer

III. LAYOUT AND SIMULATION FOR FILTER

After design and simulation for elements, it get the layout of the filter in Fig.11(a) by chip design tool. In the layout, we employed the inductor with W=60um, Line space=15nH; 2R=120um, N=2, L=1.8337nH. The thickness of the metal pad for capacitor is 3um, and thickness of dielectric layer is 100 nm. In order to ensure the big capacitance of the capacitor, it used several arrays to connect by parallel. This filter is fabricated based on 8 inch high resistivity silicon with 2000 Ω.cm. Fig.11(b) is the result for the S parameters by both circuits' simulation (pre) and layout parasitical simulation (later), which the insertion loss is -1.7dB at 2.5GHz. This result is also simulated by the chip simulation tool.



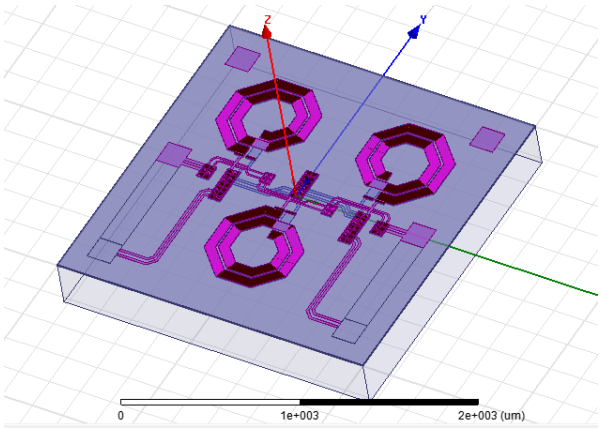
(a) The pictures of the Band-Pass-filter with test pads



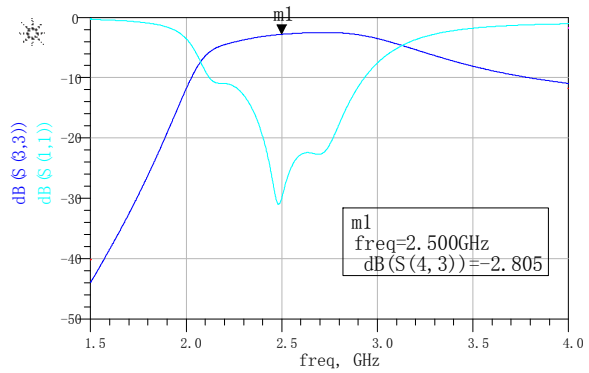
(b) Simulation results for S parameters

Fig. 11. The layout of the filter with simulation results

In Figure 12(a), it shows 3D structures for the three steps coupled filter in full-wave simulator. Figure 12(b) is the simulation results, which shows the insertion loss is -2.85dB at 2.5GHz. The loss is bigger than the calculated results by chip simulation tool. 3D simulation is closer to the real situation, which some loss didn't consider by the chip design tool. There are three kinds of reasons to cause this loss: loss of the interconnection, the parasitic of the capacitors and the semiconductor substrate loss.



(a) Simulation models for 3D structure



(b) Simulation results for S parameters

Fig. 12. The 3D model of the filter with simulation results

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