PRO-DASP

Power Reduction for Digital Audio Signal Processing

Using Transformations to Implement Hardware-Macros for a Low Power Design Methodology

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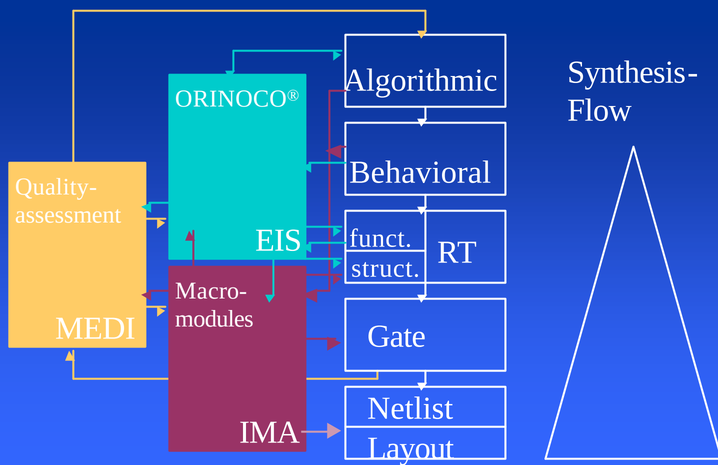
Structure

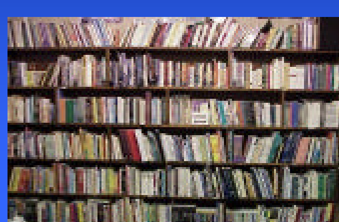
1. Macro-Module Library for Audio-Processing
2. Power-Reduction Strategy
3. Design-Flow
4. Module-Hierarchy
5. Examples (Module and Algorithm)
6. Conclusion

Cooperation



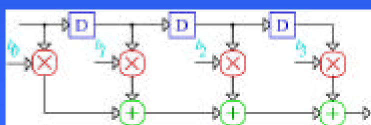
Basic Idea

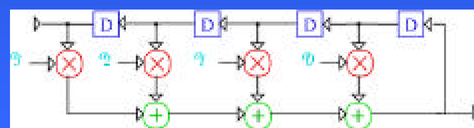
A library of Macro-Modules for low-power audio digital signal processing



Audio Signal Processing

- Filters are the Central Concept of Signal Processing
- Two main mathematical principles: FIR & IIR





Library

Audio algorithms can be partitioned to a set of filters

=> Library approach is sensible

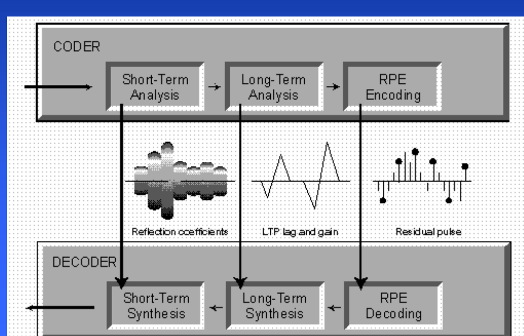
Macro-Library

Design-goals:

1. Technology independence
   => Low-level (automatic) optimization possible
   => Extensive applicability (technology, size)
2. High level of optimization
3. Easy useability
   => Development of a software-framework

Audio Filter Example: GSM-Compression 1

GSM 06.10 audio compressor model for human speech



Source: J.Degener: Putting the GSM 06.10 RPE-LTP algorithm to work

GSM Compression 2

- Two filters: 1. Short term prediction
  2. Long term prediction
- Exploits correlation in speech to reduce data-rate
- Implemented in every cellular phone
- 3G: advanced compression scheme

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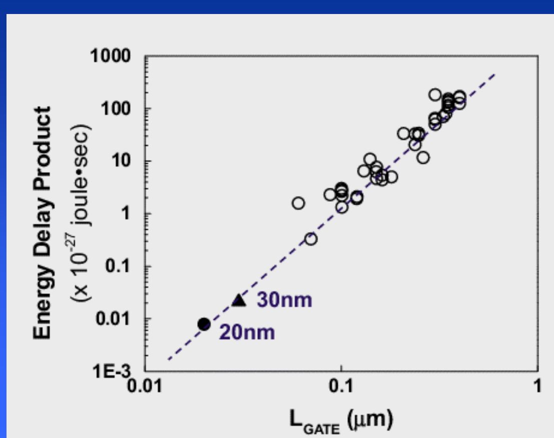
Power-Reduction Strategy 1

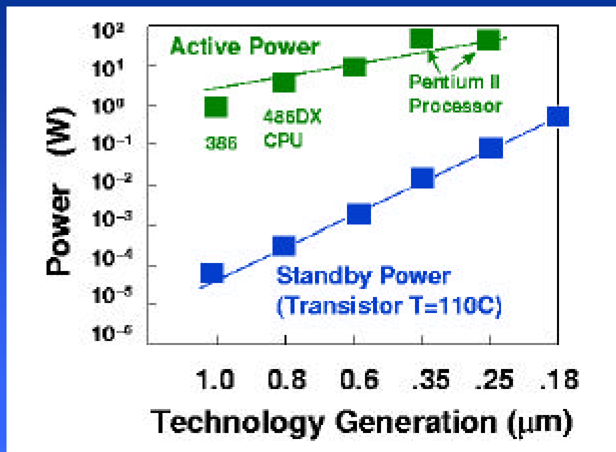
- Two trends related to Moore‘s Law:
  - Reduction of energy-delay product
  - Standby-power is becoming more important

Power-Reduction Strategy 2



Source: IEDM 2001; Enhanced 130nm Generation Logic Technology...

Power-Reduction Strategy 3



Source: Intel Techn. Jour. 3/98: Transistor Challenges for the 21. Centurzy

Power-Reduction Strategy 4

Reason:

As Supply Voltages become smaller, the relative Gate-Overdrive has to be reduced as the delay depends on the gate-overdrive

=> For modern technologies, Vdd-Reduction is limited due to relatively high gate-delay for smaller Voltages

Power-Reduction Strategy 5

Consequence for PRO-DASP:

Reduction of switched capacitance by exploiting locality (modularisation, library approach)

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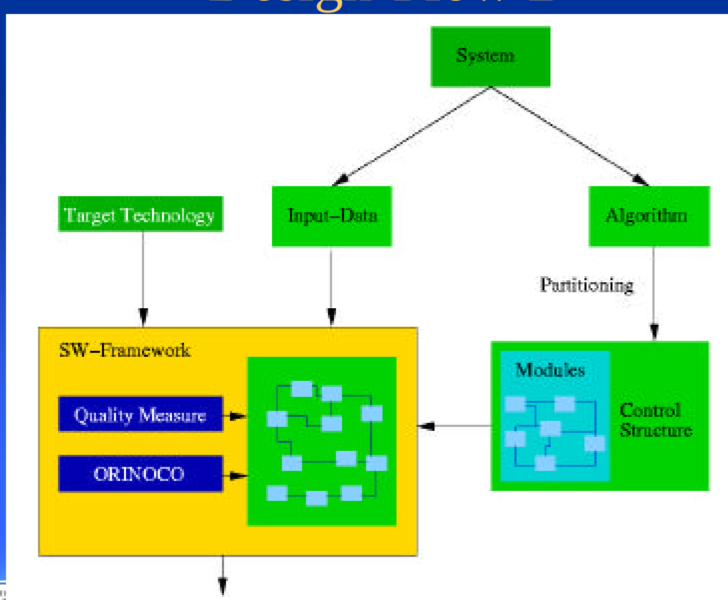
Design-Flow 1

- Partitioning of algorithm to modules
- Heuristical/probabilistical refinement
- Quality assurance via MEDI testbench
- Further optimization through ORINOCO
- Optimization through compiler/back-end tools

Design-Flow 2



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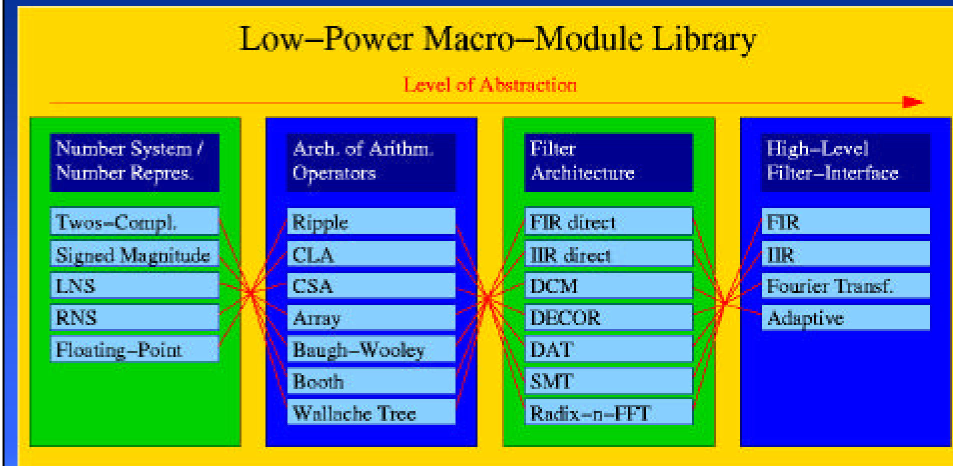
Module-Hierarchy 1

- Two-level approach:
  - Low-level modules for number systems and number representation
  - High-level modules for actual filter architecture
- „Glue-layers“

Module-Hierarchy 2



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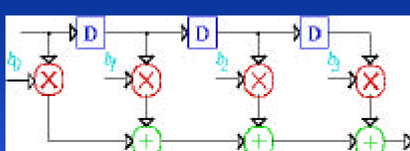
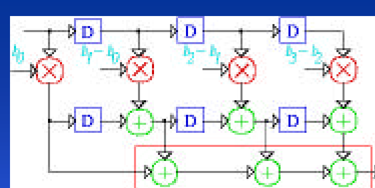
Example-Module: DECOR 1

- DECoRrelation transform: exploitation redundancy of coefficients to reduce strength of multiplication by only multiplying differences of coefficients (cf. DCM)
- Mathmatically a multiplication of the Z-transfer-function with unity

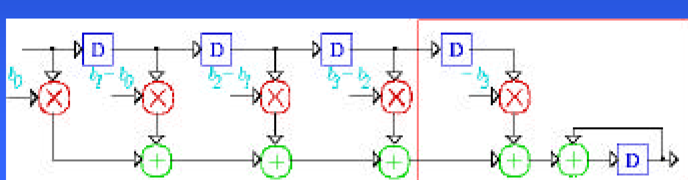
Example-Module: DECOR 2



Direct-FIR



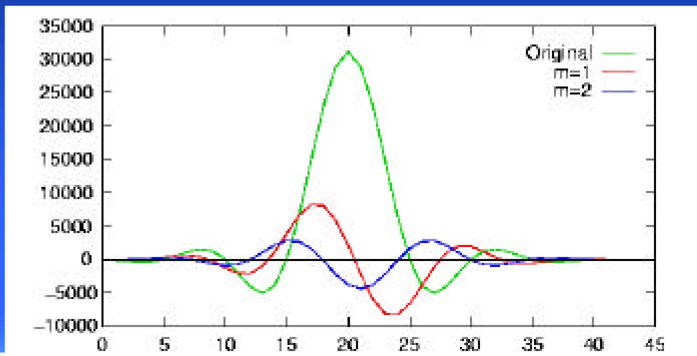
DCM-FIR



DECOR-FIR

Example-Module: DECOR 3

$$Y(z) \equiv H(z)\frac{(1+az^{-b})^m}{(1+az^{-b})^m}X(z)$$

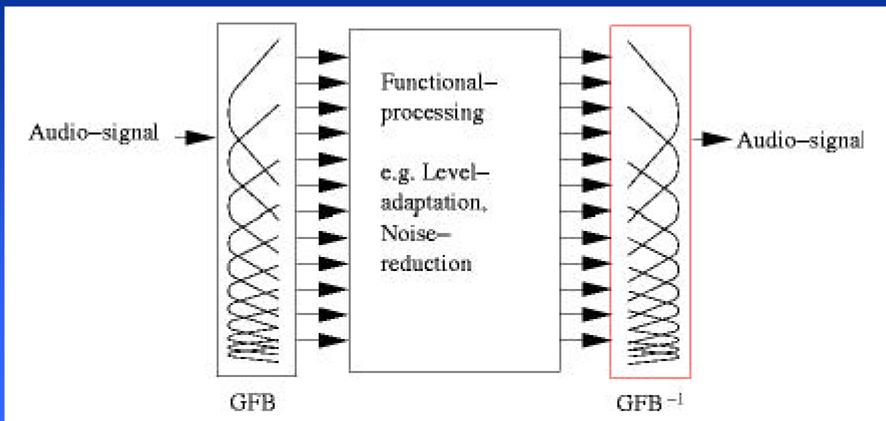


a=1,
b=-1

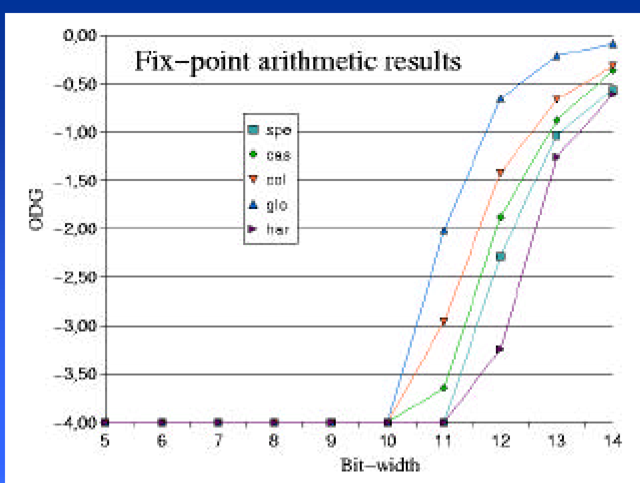
Example Algorithm: Resynthesis 1

- Gammatone-resynthesis is used as pre and post-Processing for audio algorithms
- Set of band-pass filters, frequency selection is approximation of basilar membrane filtering of inner ear

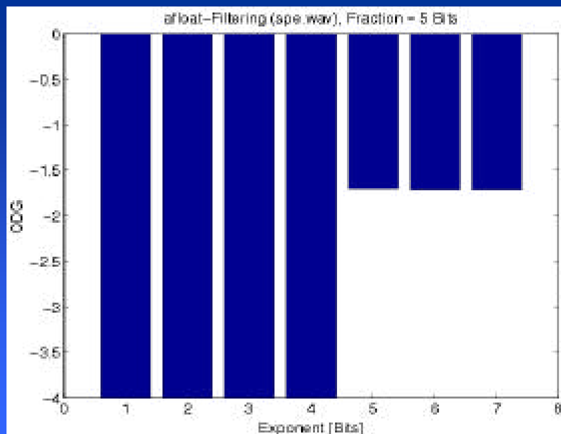
Example Algorithm: Resynthesis 2



Resynthesis Results Fix-Point

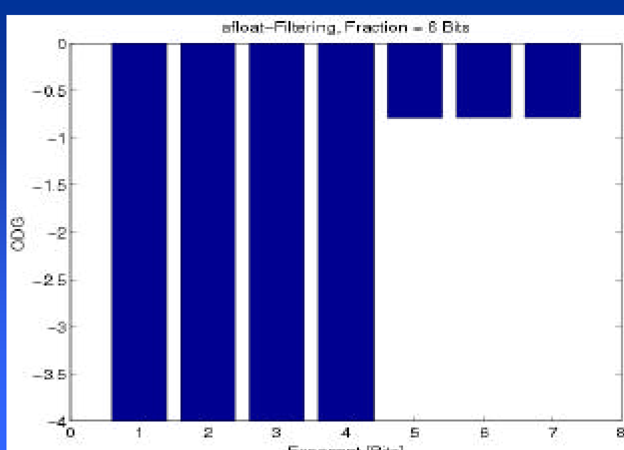


Resynthesis Results Floating Point 1



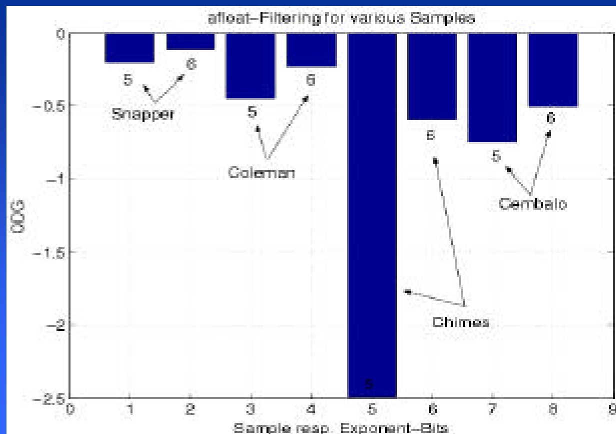
VIVA-Kolloquium 2002

Resynthesis Results Floating Point 2



VIVA-Kolloquium 2002

Resynthesis Results Floating Point 3



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Conclusion

- Modularization is a sensible approach
  - Energy savings for modern technologies
  - Audio algorithms are easily partitioned to modules
  - Modules can be optimized by external tools

Conclusion

- Modules are embedded into a SW-frame
  - Application of probablistic/heuristic methods for selection and optimization of modules
  - Exploration of a multi-dimensional solution space possible

Conclusion

- Independent of target technology through focusing on algorithmic level (in contrast to existing high-level tools like HYPER-LP)

Outlook

- Integration of probabilistic/heuristic methods for module selection
- Automatic generation of VHDL hardware description in SW-FW
- VLSI chip-design for example algorithm