Effect of Solar Array Capacitance on the Performance of Switching Shunt Voltage Regulator

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Abstract—Due to high power demand photovoltaic regulators are being switched at high frequency. The solar cell capacitance increases the ripple voltage of the switching regulators at higher switching frequencies. Increased ripple due to array capacitance is calculated and its effect in limiting the maximum design switching frequency is studied. An experimental switching regulator is designed and used to confirm the theoretical considerations. This study has identified a method of solar cell capacitance measurement that is relevant to the design of a switching voltage regulator.

Index Terms—Array capacitance, pulse-width modulator (PWM), shunt switching power conditioner.

I. INTRODUCTION

PHOTOVOLTAIC conversion of solar energy is one of the most promising ways of meeting the increasing energy demand. The technology of photovoltaics has evolved and is vying to become an economical alternative to other power sources in certain niche applications such as remote terminals. In space applications, this is the only source of power, barring nuclear alternatives. The need for small size and low weight has necessitated the use of high-speed switching voltage regulators. Although the solar cell is a dc source when used with switching regulators, the dynamic or ac parameters of a solar cell array, particularly its capacitance, need to be considered. It is known that the solar cell capacitance is nonlinear and a function of the operating voltage and temperature [1], [2]. The variation of capacitance of a silicon solar cell as a function of cell voltage is shown in Fig. 1 along with its current-voltage and power-voltage characteristics. The solar cell capacitance near open circuit voltage is quite large (around 25 times) compared to that of the near short circuit. A solar cell array is operated around its maximum power point, where solar cell capacitance is considerable ($0.05 \ \mu\text{F/Cm}^2$ for silicon solar cell—see Fig. 1), which rapidly increases toward open circuit voltage. Hence, the influence of solar cell capacitance on the performance of power regulators should be considered in designing a solar photovoltaic power conditioning system. The capacitance of solar cell arrays has been considered [3]–[6] for the design of shunt power regulators. Their emphasis was on the stability of regulator or input filtering. The effect of

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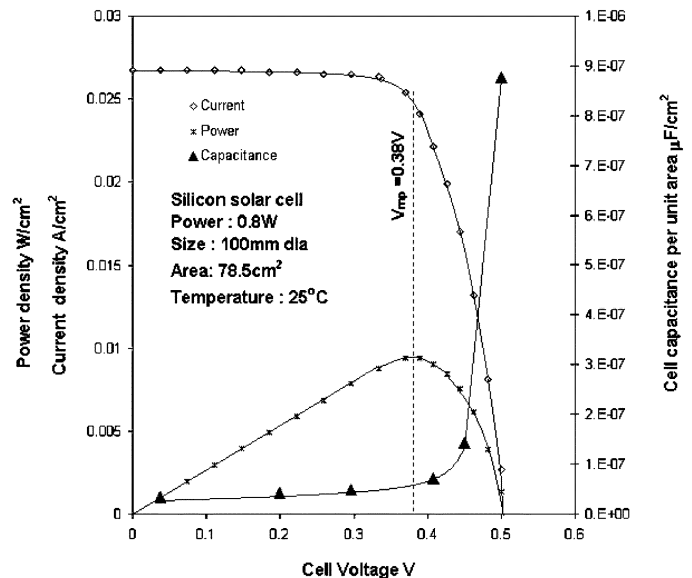
Fig. 1. Variation in cell capacitance, current, and power as function of cell voltage.
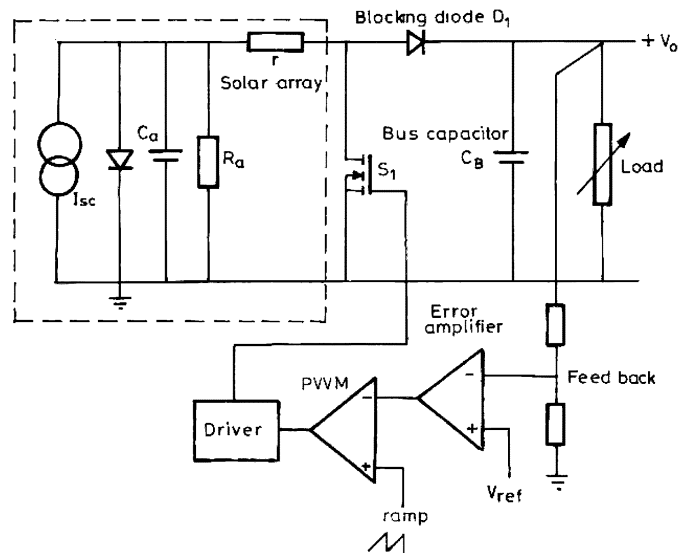

Fig. 2. Schematic diagram of fixed frequency PWM shunt switching voltage regulator.

solar array capacitance on the output power ripple or the limitation it puts on the switching frequency has not been addressed.

II. STEADY-STATE ANALYSIS

To illustrate the effect of solar cell capacitance on the design and operation of power conditioning circuits, a typical fixed frequency shunt voltage regulator is considered, as shown in Fig. 2.
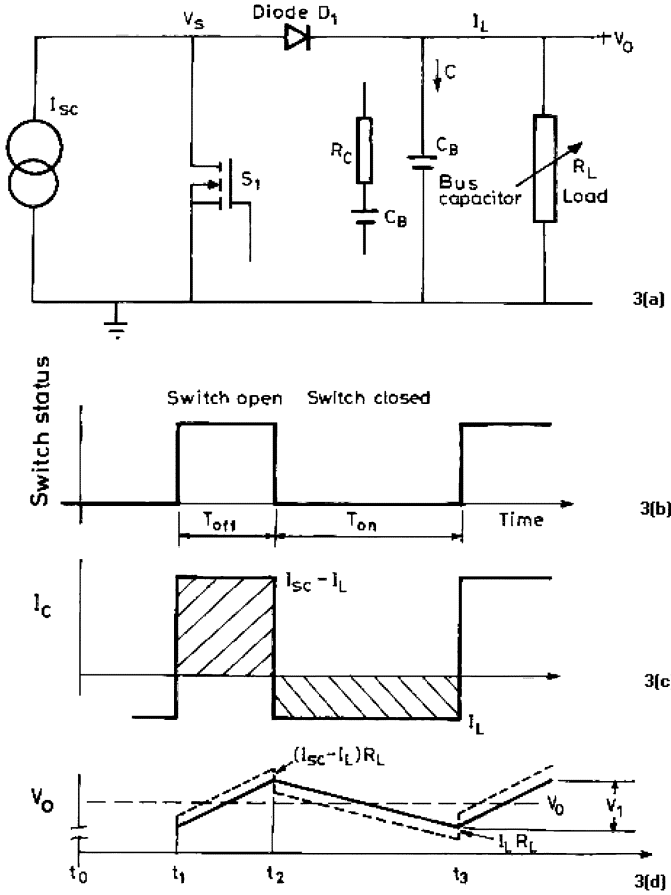
Fig. 3. (a) Equivalent circuit of shunt regulator, (b) switch status, (c) current through bus capacitor, and (d) output voltage ripple.

Certain basic blocks of the pulse-width modulator (PWM) controller circuit are shown in Fig. 2, which consists of an error amplifier, a PWM signal generator, and a shunt switch driver. The average voltage of the shunt regulator is compared with the reference voltage (V_{ref}) and an error signal is generated, which is compared with a fixed frequency ramp to generate a PWM signal. The duty cycle of the PWM output is such as to regulate the average output voltage (V_o) and the bus capacitor, load current, and solar array characteristics determine the ripple on the average voltage. The equivalent circuit of a solar array has been modeled as a current source with a diode, a capacitance (C_a), and dynamic shunt resistance (R_a), all in parallel and a series resistance (r). When the switch (S_1) is "OFF," the solar array takes some time to rise to the output voltage (V_o) delaying the supply of current to the output and bus capacitor. The increase in ripple due to this delay and the limitations this puts on the maximum switching frequency of operation are considered here, which have until now been ignored.

In actual photovoltaic power regulators, several circuits of the type shown in Fig. 2 are paralleled to get the required power. However, only one of these will have PWM capability [7]. The other circuits are either ON or OFF depending on the power to be supplied. Only the difference between the power needed and the power supplied by an integral number of array circuits is delivered by the PWM controlled power conditioner. Hence, only

the PWM switching part of the voltage regulator has been considered.

Fig. 3 shows the fixed frequency shunt voltage regulator described earlier with its current and voltage waveforms. Also shown is the equivalent circuit of the bus capacitor (unconnected C_B, R_C) by its side in Fig. 3(a). If the solar array capacitance and the equivalent series resistance of the bus capacitor are not considered, the output voltage ripple caused by the switching of S1 is given by [3]

$$V_1 = \frac{I_L D}{C_B f_s} = \frac{I_{SC} D(1-D)}{C_B f_s} \tag{1}$$

where

I_L load current (normally I_L is equal to maximum power point current I_{mp});
I_{SC} solar array short circuit current;
C_B bus capacitance;
f_S switching frequency;
D duty cycle.

The expected waveforms of current (I_c) through the bus capacitor and output voltage (V_o) when solar array is switched ON and OFF are shown in Fig. 3(c) and (d). If equivalent series resistance (R_C) of the bus capacitor is taken into account, the output voltage ripple is given by

$$V_1 = I_{SC} R_C + \frac{I_{SC} D(1-D)}{C_B f_S} \tag{2}$$

where R_C is the equivalent series resistance (ESR) of bus capacitor.

However, the fixed ripple due to equivalent series resistance of the bus capacitor is neglected in further analysis as it is small at lower frequency of operation and can simply be added to the ripple voltage caused by other factors at the end.

As the solar cell array capacitance is large and increases exponentially with operating voltage, it is essential to consider the solar cell array capacitance in the design of switching voltage regulators. However, the solar array series resistance (r) and the ON resistance of switch S1 have been neglected as very small in the following analysis.

Considering the effect of solar array capacitance (which causes slow raise of array voltage) into account the output voltage ripple at the bus is given by

$$V_R = \frac{I_{sc}(1-D)D}{C_B f_s} \tag{3}$$

where $D^{|}$ is the effective duty cycle $= (D + (C_a V_o / I_{sc}) f_s)$.

It is observed that the output voltage ripple increases with increase of array capacitance (C_a) for a given duty cycle (D) of the switch. The switching waveforms, which accounts for array capacitance, are shown in Fig. 4. When the switch is opened at time t_3, the time taken by the array voltage $(t_4 - t_3)$ to increase to voltage V_o is determined by the array capacitance and its short circuit current; diode drop is neglected

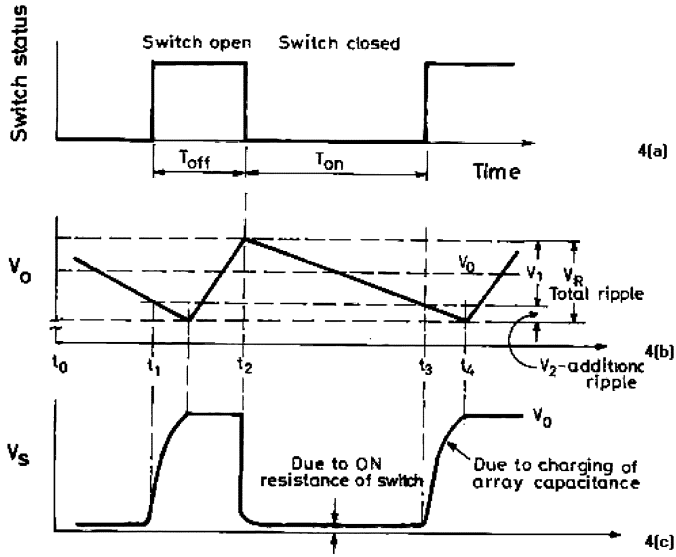$$T_a = t_4 - t_3 = \frac{C_a V_o}{I_{SC}}. \tag{4}$$

Fig. 4. (a) Shunt switch status, (b) voltage across shunt switch, and (c) output voltage ripple with extra ripple due to array capacitance.

The bus capacitance supports the load during this period and the extra output voltage ripple due to this slow rise of array voltage is given by

$$V_2 = \frac{C_a I_L V_o}{C_B I_{SC}} \qquad (5)$$

where

I_L load current;

V_1 output ripple without considering solar array capacitance;

V_R output ripple taking into account solar array capacitance;

V_2 that part of output ripple (extra ripple) caused by solar array capacitance.

The variation of extra ripple (V_2) caused by array capacitance expressed as the percentage of output voltage $((V_2/V_o) * 100)$ as a function of the operating point for a typical solar array is shown in Fig. 5. Observe that the extra ripple (V_2) increases rapidly as the operating point shifts toward the open circuit voltage (V_{oc}) of the array.

The discussion is valid, not only for a fixed frequency shunt-switching regulator, but also to a variable frequency fixed ripple shunt-switching regulator. The governing equations are also the same as that for the fixed frequency shunt switching regulators.

III. EXPERIMENTATION AND RESULTS

To confirm the above analysis, a fixed frequency PWM shunt switching voltage regulator, explained earlier in Fig. 2, is built and tested with an array of 27 solar cells in series, each cell with an area of 78.5 cm^2. The measured capacitance (C_a) of this solar cell array at different bias voltages (around V_{mp}) is shown in Fig. 6. The array operating voltage chosen is 10.5 V, which is close to "V_{mp}" (10.3 V) giving an output voltage of 9.8 V (due to diode forward voltage drop). The array capacitance at 10.5 V is 0.166 μF. The array is illuminated by a set of halogen lamps located to give uniform illumination on solar cells. The fixed frequency switching voltage regulator is operated at different
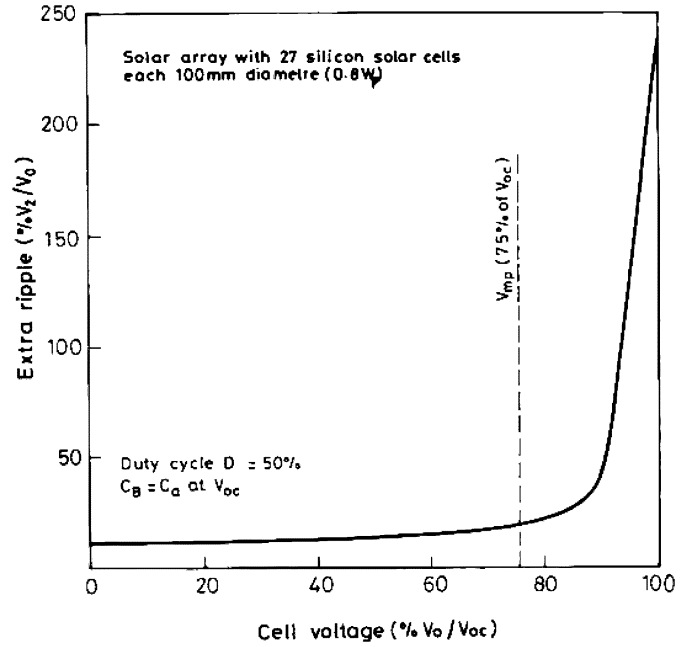

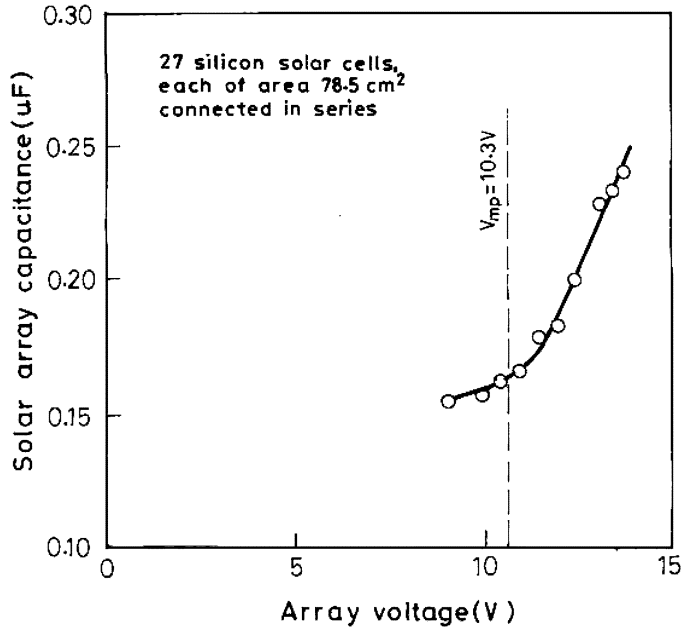Fig. 5. Variation in additional ripple "V_2" due to array operating point.

Fig. 6. Variation in array capacitance with array bias voltage.

load currents (0.1 A to 0.6 A in steps of 0.1 A) and switching frequencies from 20 to 80 kHz. The output voltage ripple and voltage waveform at the shunt switch are monitored using a digital storage oscilloscope (Tektronix: TDS 2012).

A snapshot of the output voltage ripple and expanded view of the ripple in output voltage, showing additional ripple (V_2) caused by array capacitance, are shown in Fig. 7(a) and (b), respectively. It is observed from Fig. 7(b) that the solar array takes around 2.5 μs to rise from zero to 10.5 V (refer waveform-1) resulting in an extra ripple of 27.2 mV (refer waveform-2) at 60% load (0.6 A). Extra ripple voltage (V_2) measured for load current varying from 10% (0.1 A) to 60% (0.6 A) of I_{sc} is compared with calculated values in Fig. 8, which shows a very close

Fig. 8. Variation of extra ripple with load current.
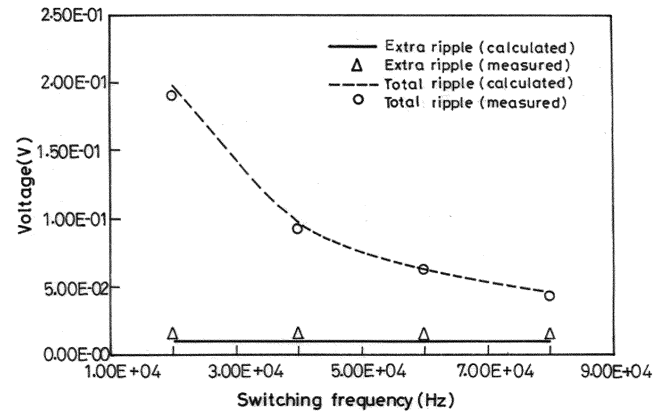
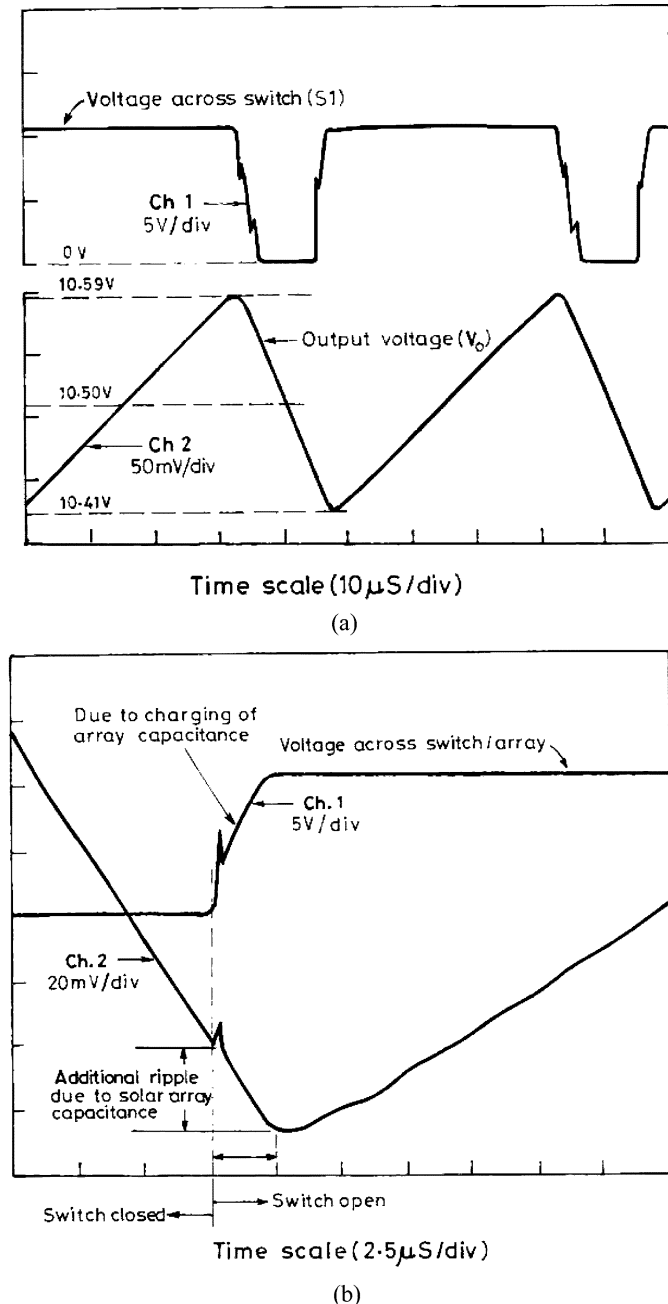Fig. 9. Variation of extra ripple and total ripple with switching frequency.

Fig. 7. At a load current of 0.6 A and a switching frequency 20 kHz: (a) measured total ripple and (b) measured extra ripple.

match. The total ripple voltage (V_R) and extra ripple voltage (V_2) are also measured as a function of switching frequency for a given bus capacitance, which is shown in Fig. 9. It is observed that the total ripple voltage decreases with increase in switching frequency but additional ripple voltage (V_2) is constant, as expected, for a given bus capacitance "C_B."

A. Measurement of Array Capacitance

The value of solar cell capacitance depends on the method of measurement. Therefore, it is essential to clarify how solar cell array capacitance is to be measured or calculated for use in regulator design. One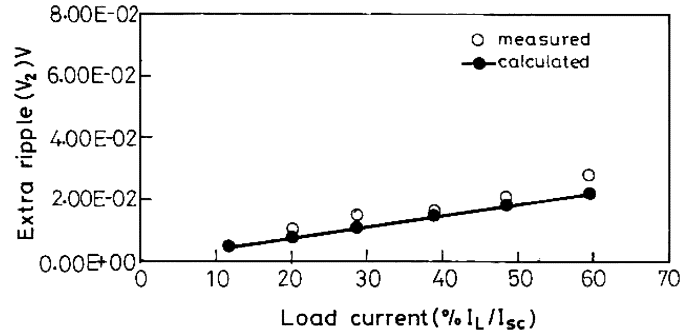 of the popular methods of measuring solar cell capacitance is by the small signal method [8]. A small (~ 10 mV) sinusoidal voltage signal is applied to a solar cell, by superposing on the dc bias voltage (its operating point) and the resultant ac current is measured in phase and magnitude. The dynamic capacitance (C_p) and dynamic resistance (R_p) of the solar cell array are calculated from the real and imaginary components of its impedance. This capacitance is a local (differential) value about the operating point defined as

$$C_p = \frac{dQ}{dv}. \tag{6}$$

When the switch S1 in switching regulator is opened, the voltage across the solar cell array increases from zero to voltage V_o and the time taken to charge solar array to V_o is given by the charge equivalent capacitance (C_q) because the charging time (rise time) depends on the total quantity of charge (Q_o) to be supplied. The charge equivalent capacitance is given by [9]

$$C_q = \frac{Q_o}{V_o} = \frac{1}{V_o} \int_o^{V_o} C_P dv. \tag{7}$$

C_q is calculated by finding the area under C_p verses V curve, which varies with the operating point. C_q is also measured directly in time domain [9] by measuring the total charge accumulated in the cell at the operating point. The capacitance of relevance for calculating the ripple in the voltage regulator is C_q.

Another definition of capacitance is also used for calculating the energy stored in the solar cell capacitance and this capacitance is defined as energy equivalent capacitance (C_e)

$$C_e = \frac{1}{(V_o)^2} \int_o^{V_o} V_o C_P dv. \qquad (8)$$

This capacitance (C_e) is used to calculate the energy stored in the solar cell capacitance. Generally, a voltage regulator is designed to work close to maximum power point (V_{mp}, I_{mp}) of the solar cell array. Hence, the most relevant operating point at which capacitance has to be measured is V_{mp}. The solar array works at varying temperatures, between $-20\,°C$ to $+60\,°C$ in terrestrial, and $-100\,°C$ to $+100\,°C$ in space applications. The solar cell capacitance at V_{mp} increases with temperature [10]. Hence, it is necessary to consider the solar array charge equivalent capacitance (C_q) at V_{mp} and at expected maximum operating temperature, to design a reliable switching shunt voltage regulator. At all other temperatures the regulator will be operating at and below V_{mp} and C_q will be lower. For an array, the charge equivalent capacitance "C_a" is calculated from C_q of the cell.

IV. DESIGN CONSIDERATIONS

For a given operating frequency (f_s), the output voltage ripple (V_R) is given by (3). If the operating frequency (f_s) is low the effective duty cycle $(D^|)$ is nearly equal to switch duty cycle (D) and the ripple voltage is given by (1). The ripple voltage (V_R) is maximum when the duty cycle is 0.5. The bus capacitance (C_B) can be selected to get an acceptable predetermined ripple as

$$C_B \geq \frac{0.25 I_{sc}}{f_s V_R}. \qquad (9)$$

However, as the operating frequency increases, solar array rise time (T_a) becomes a larger part of the switch ON/OFF time. When this happens the effective duty cycle $(D^| = T_{ON}^|/T)$ decreases. If the load current I_L is held constant, the feedback voltage regulator decreases the ON time of the switch (S1) to keep the output voltage constant as the operating frequency increases. However, a limiting frequency $(f_{s(\max)})$ is reached when the switch (S1) switches ON for a extremely short period and the effective ON period is practically equal to T_a, the rise time of the array voltage. At this frequency, load current (I_L) is given by

$$I_L = \frac{I_{sc} T_{off}^|}{T} = \frac{I_{sc}(T - T_a))}{T} = I_{sc}\left(1 - \frac{T_a}{T}\right). \qquad (10)$$

Substituting for T_a from (4) and replacing $I_L = V_o/R_L$, and switching frequency (f_s) is

$$f_{s(\max)} = \left[\frac{I_{sc}}{C_a V_o} - \frac{1}{R_L C_a}\right]. \qquad (11)$$

At this frequency the output ripple voltage is

$$V_R = \frac{C_a V_o I_L}{I_{sc} C_B}. \qquad (12)$$

If the operating frequency is increased above $f_{s(\max)}$ the $T_{on}^|$ cannot be further decreased and the circuits can no longer regulate the output voltage. Observe that $f_{s(\max)}$ is inversely related to array capacitance and beyond the maximum operating voltage (V_{mp}) of the array its capacitance increases exponentially. Hence, it is necessary to select the operating point such that it does not cross V_{mp} at the maximum operating temperature.

For the circuit used in this investigation the maximum frequency for an operation at 0.6 A (60% duty cycle) is 289 kHz. Thus, the upper limit to switching frequency is set by the array.

It may be noted that in the limit the switch will be OFF continuously at that condition rise time for the array voltage, and has no meaning.

V. CONCLUSION

The variation of solar cell capacitance is very large over its operating points. It has a dominant effect on the performance of shunt switching regulators around and beyond the maximum power point. The output voltage ripple in a switching regulator increases considerably due to solar cell array capacitance and the maximum frequency of operation $f_{s(\max)}$ is limited by array capacitance. Special consideration must be given to the selection of a shunt switch as the array capacitance causes peak currents limited only by the parasitic impedances of the circuit. For general design applications, it is adequate to consider array capacitance at the maximum power point and at the room temperature. The capacitance to be considered for the design of a shunt switching voltage regulator is the charge equivalent capacitor (C_q) and not the cell dynamic capacitance "C_p."
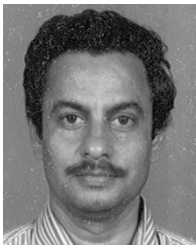
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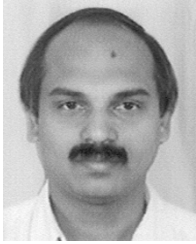
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