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Review of CMOS image sensors

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Abstract

The role of CMOS Image Sensors since their birth around the 1960s, has been changing a lot. Unlike the past, current CMOS Image Sensors are becoming competitive with regard to Charged Couple Device (CCD) technology. They offer many advantages with respect to CCD, such as lower power consumption, lower voltage operation, on-chip functionality and lower cost. Nevertheless, they are still too noisy and less sensitive than CCDs.

Noise and sensitivity are the key-factors to compete with industrial and scientific CCDs. It must be pointed out also that there are several kinds of CMOS Image sensors, each of them to satisfy the huge demand in different areas, such as Digital photography, industrial vision, medical and space applications, electrostatic sensing, automotive, instrumentation and 3D vision systems.

In the wake of that, a lot of research has been carried out, focusing on problems to be solved such as sensitivity, noise, power consumption, voltage operation, speed imaging and dynamic range. In this paper, CMOS Image Sensors are reviewed, providing information on the latest advances achieved, their applications, the new challenges and their limitations. In conclusion, the State-of-the-art of CMOS Image Sensors.

Keywords: CMOS image sensors; APS

1. Introduction

1.1. Introduction

Currently, there are many different Imaging Systems suitable for different purposes, de pending upon their final application. Digital Cameras, Camcorders, Webcams, Security cameras or IR-cameras are well-known Imaging Systems. Moreover, as the purposes are different, the technologies used differ from each other. This situation has been possible thanks to the fact that Imaging Technologies, mainly the ones concerning CMOS imagers, have been improving their performance, their functional capability and their flexibility during last years.

CMOS image sensors have received much attention over the last decade, because their performance is very promising compared to CCDs. New horizons can be opened, like ultra low power or camera-on-chip systems. Owing to this situation and the latest developments within this field, this paper reviews CMOS image sensors since 1997 in order to continue and update the review reported by E. Fossum [1].

In order to understand why CMOS image sensors have emerged as a strong alternative to CCDs, it is important, first, to highlight the *Advantages and Disadvantages* of CMOS image sensors.

1.2. Advantages and disadvantages

The main *Advantages* of CMOS imagers are:

1. *Low power consumption*. Estimates of CMOS power consumption range from one-third to more than 100 times less than that of CCDs [2]. Besides, they work at low voltage. CMOS imagers only need one supply voltage, instead of CCDs, which need 3 or 4.
2. *Lower cost* compared to CCD's technology.
3. *On chip functionality* and compatibility with standard CMOS technology. CMOS imagers allow monolithical integration of readout and signal processing electronics. In 2001, a study for Cross Contamination between CMOS Image Sensor and IC product showed no

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problems [3]. A sensor can integrate various signal and image processing blocks such as amplifiers, ADCs, circuits for colour processing and data compression, etc. on the same chip.
4. *Miniaturisation*, although important limitations exist, the level of integration is rather high [4].
5. *Random access* of image data.
6. Selective read-out mechanism [4,5]
7. *High-speed imaging*. The flexibility and the possibility to acquire images in a very short period of time [6].
8. *To avoid blooming and smearing effects*, which are typical problems of CDD technology [6].

As outlined before, despite these advantages, there are still significant *Disadvantages* of CMOS image sensors compared to CCD technology. Therefore, these problems need to be solved so that CMOS image sensors can compete in any area. These disadvantages are:

1. *Sensitivity*: The basic quality criterion for pixel *sensitivity* is the product of its *Fill Factor* and its *Quantum Efficiency* (FFxQE) where *Fill Factor* is the ratio of light-sensitive area to the pixel's total size, and *Quantum efficiency* is the ratio of photon-generated electrons that the pixel captures to the photons incident on the pixel area. It must be pointed out that Active Pixel Sensors (APS) have reduced sensitivity to incident light, due to a limited Fill Factor, hence, less quantum efficiency.
2. *Noise*: CMOS Image sensors suffer from different noise sources which set the fundamental limits of their performance, especially under low illumination.
3. *Dynamic range* (*DR*): Dynamic Range, which is the ratio of the saturation signal to the rms noise floor of the sensor, is limited by the *photosensitive-area size, integration time and noise floor*.
4. Less image quality than CCD.

In order to overcome the *disadvantages* outlined before and, also, to improve the current advantages as well, the research on CMOS image sensors, since 1997, has been mostly focused on the following areas:

- Low noise
- High dynamic range
- High sensitivity and High fill factor
- Low power consumption
- Low voltage operation
- High speed imaging

In spite of the high number of applications of the imaging systems, all of them have almost always the same *basic functions*: (1) Optical gathering of photons (lens), (2) Wavelength discrimination of photons (filter), (3) Detector for photons to electrons conversion (photodiode), (4) A method to readout the detector (CCD), (5) Timing, control, and drive electronics for the sensors, (6) Signal processing electronics such as for Correlated Double Sampling (CDS) or for color processing, (7) Analog-to-digital conversion, (8) Interface electronics.

1.3. Historical background

1.3.1. Before 1997

CMOS image sensors could not compete in the past with CCD technology, although the first solid-state imagers presented in the 60 s and early 70 s used MOS diodes as light sensitive elements and during the 60 s several works were performed in the solid-state image sensor's field, using NMOS, PMOS and bipolar processes. [1] For instance, photodiode image sensors with MOS scanning circuits were known from mid 60 s. However, they were not embraced commercially because of poor performance and large pixel size (for that time) relative to that of the CCDs. In fact, even though CMOS image sensors appeared in 1967, CCDs have prevailed since their invention in 1970 [7]. Full-analog CCDs have dominated the vision applications owing to their superior dynamic range, lower fixed-pattern noise (FPN), smaller pixels and higher sensitivity to light [2].

In the early 1990s, CMOS image sensors re-emerged as an alternative to CCDs thanks to the advantages pointed out before. Passive pixel CMOS arrays were the first generation. Major improvements in signal-to-noise ratio for photo-diodes and charge-injection devices (CIDs) could be made by adding an amplifier per column or per row. Therefore, sensors that implement a buffer, which acts as simple source follower, per pixel have been known as active-pixel sensors (APS) and represent the second generation of CMOS imagers [8]. CMOS APS (Active Pixel Sensors) promised to provide: lower noise readout, improved scalability to large array formats and higher speed readout compared to PPS.

1.3.2. After 1997

Recently, the research has been focusing, mainly, on the improvement of the APS, because APS are the pixel circuit that have shown better performance and flexibility.

In order to strongly compete with CCD technology, the aim of researchers has been to obtain higher performance imaging systems based on CMOS technology. Therefore, there have been several reports on improving the fill-factor (FF) with low power consumption, low voltage operation, low noise, high speed imaging and high dynamic range. Moreover, little research has been done on other topics such as pixel shape optimization [9], pixels on SOI substrate [10], high resolution [11], APS with variable resolution [12,13], self-correcting [14,15] and for low light [16–18], etc.

On the other hand, *new applications* have emerged due to the CMOS imager development. Automotive applications, imaging for cellular or static phones, computer video, space, medical, digital photography and 3D applications have been improved. So many applications areas caused that CMOS

technology made a breakthrough on two fronts in 2000: sensors for computers and cell phones on the low end, and ultra high speed, large format imaging on the high-end [19]. Moreover, new technologies and architectures appeared due to scale effects. For instance, Thin Film on ASIC (TFA) technology [20–24] and Complementary Active Pixel Sensors (CAPS) [25–31]. Finally, some *studies* have been carried out to study the radiation effects and how radiation induced dark current in APS [32–39] and the effect of hot carriers [40]. In addition, it is well known that heavy metals such as Cu, Ni, Fe or Zn, which appear in some CMOS image sensor processes, can cause defects in silicon and influence gate oxide quality in VLSI circuits. So the cross-contamination between CMOS image sensor and IC technologies has been studied as well [3].

1.4. CCD technology limitations

CCD technology has prevailed since its invention in 1970, because it provided better solutions to the typical problems, such as FPN and it had a higher fill factor, smaller pixel size, larger format, etc. than CMOS, which could not compete with CCD performance. Then, the research has been mainly focused on CCD technology. Nevertheless, CCD technology has some *limitations*: For instance, in a CCD-based system, the *basic function* often consumes several watts (1–5 W) and is, therefore, a major drain for the battery. Furthermore, unlike CMOS image sensors, CCD cannot be monolithically integrated with analog readout and digital control electronics [1]. New applications have appeared as well. For instance, in the automotive field, the image sensor has to fulfill the specifications concerning the temperature range, the range of illumination, and the power dissipation. CCD image sensors cannot guarantee their functionality over the whole temperature range required, or to cover all lighting conditions during daytime. They cannot operate beyond quite restrictive ranges of illumination and temperature. For instance, a non illuminated CCD is completely full of electrons after roughly 1 min at room temperature and the dark current doubles approximately every 7 K. This means that noise drastically increases with the temperature of the chip.

Also there is a need to acquire images in a very short time for high speed applications, therefore short integration time is required. This leads to image sensors equipped with synchronous shutters in order to avoid blur [6]. Other CCD typical problems are: Blooming and smearing [6]. CCDs are high capacitance devices, so they suffer from high power dissipation. CCDs need many different voltage levels, they are sensitive to radiation and their readout rate is limited.

1.5. CMOS Image sensors (APS) as an alternative to overcome CCDs limitations

CMOS imagers began to be a strong alternative since early 90 s (see Fig. 1). Their most important feature was that they would satisfy the demand for low-power, miniaturised and cost-effective imaging systems. Moreover, CMOS image sensors offered the possibility to monolithically integrate a significant amount of VLSI electronics on-chip and reduce component and packaging costs [1].

However, passive pixel CMOS arrays were the first generation. CMOS Active Pixel Sensors (APS) have offered better performance though. Up to now, a lot of research and studies has been done on this topic and CMOS APS technology has demonstrated noise, quantum efficiency, and dynamic range performance comparable to CCDs [41]. However, CCDs still offer a better image quality, especially for digital still applications. Therefore, CCDs are still superior to CMOS image sensors as far as signal-to-noise and dynamic range is concerned. This means that CCDs are still the first choice for high quality still photography.

In spite of the huge work that has been carried out in this area, more research on reducing the noise and increasing the sensitivity of the CMOS imagers is needed in order to compete with industrial and scientific CCDs. For instance, if the noise issues (mainly reset noise and dark current shot noise) can be solved with CMOS imagers, they might be able to challenge CCDs in digital still applications [5].

Thanks to the fact that there were niches to cover such as high-speed, motion analysis or detection, etc. [42], CMOS APS technology has been growing up and, currently, there are different kinds of pixel circuits depending on their purpose. For instance, logarithmic APS, capacitive transimpedance amplifier (CTIA) APS [43], APS with shutter [44] or complementary active pixel sensors CAPS [31]. Currently, there is no CMOS image sensor that can provide the global quality of a CCD in terms of noise, sensitivity, dynamic range and so on. This means that it is possible to

CCD	CMOS
Lower noise	Low power consumption
Smaller pixel size	Single power supply
Lower dark current	High Integration capability
100% Fill Factor	Lower cost
Higher sensitivity	Single master clock
Electronic shutter without artifacts	Random access

Fig. 1. Summary of the main advantages of CCD and CMOS image sensors.

reach or improve one or two of their characteristics with a specific architecture, but not all together.

1.6. New applications-new challenges

The improvement of CMOS image sensors has opened up new application areas [45], owing to the lower cost of CMOS image sensors. They can compete with CCDs in applications such as IR-vision (systems for automobile drivers under fog and night driving conditions, security cameras, baby monitors that can 'see' in the dark, etc.)

Besides these, imaging or vision systems for X-ray, space, medical, 3D, consumer electronics, automotive or low-light applications are required, and most of them need *highly integrated imaging systems*, so CMOS image sensors are well situated to jump into the market.

Moreover, imaging or vision systems have to offer, in order to be ideal, good imaging performance with low noise, no lag, no smear, good blooming control, random access, simple clocks and fast readout rates.

1.7. CMOS Image sensors limitations and device scaling considerations

1.7.1. Industry trend

The technology has advanced from a 2 μm CMOS in 1993 to 0.25 μm in 1996 [4] and less than 0.1 μm will also be possible. So, considering scaling effects has been necessary in order to know where and which are the limits of CMOS imagers.

Some *Scaling Considerations* were studied in 1996[46] and in 1997[4]. The question was whether the image sensing performance of CMOS imagers would get better or worse as the technology would be scaled. The question arose because if CMOS imagers would scale down as fast as industry standard CMOS technologies, CMOS imagers would achieve a smaller pixel size than CCDs during the following years [4]. Anyway, it seemed to be clear that 'standard ' CMOS technology, which provided good imaging performance at 2–1 μm without any process change, would need some modifications in its fabrication process and innovations on the pixel architecture in order to enable CMOS imagers to perform good quality imaging when using the 0.25 μm generation technology and beyond [1]. In fact, CMOS imagers could not be scaled down using standard CMOS technology because scaling effects increase leakage current and reduce dynamic range. That is to say that performance was getting worse. Thus, technological changes in CMOS technology are needed in order to reach the imaging performance of CCDs with a CMOS imager.

In 2000 [20] a scaling perspectives study was done and, certainly, new technological processes appeared, such as PPD [20] and TFA imagers [20–24] (See Fig. 2). Later, CAPS appeared as well [25–31]. TFA imagers are immune to negative scaling impacts on sensitivity. Even more, they

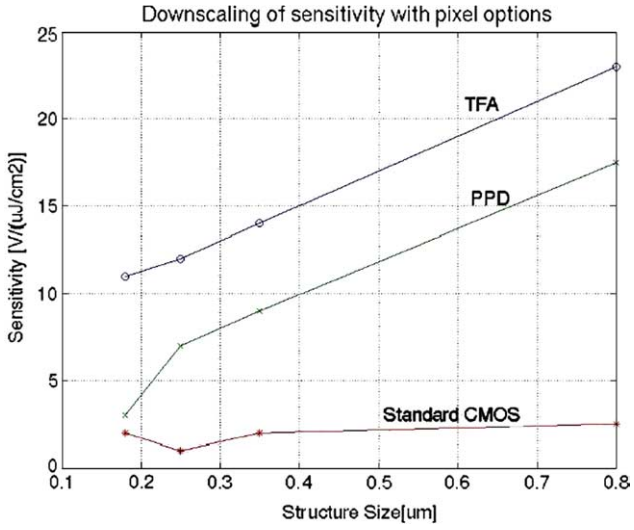

Fig. 2. Downscaling of sensitivity with pixel options.

offer high sensitivity and high dynamic range. Nevertheless this technology is not suitable down to 0.1 μm.

Thus, it has been demonstrated the limitation of conventional APS, because conventional pixel architecture (APS) cannot work properly with a 0.1 μm technology or below because the low power of these technologies implies a decrease in the saturation level and in the light sensitivity that it is not acceptable. Nevertheless, an alternative architecture called CAPS (Complementary APS) came on scene [25–31]. They are a possible way to design a highly integrated, high performance CMOS image sensor in the deep sub-quarter micron technology, because CAPS architecture has a very attractive low-voltage operation capability. For instance 1.0 V [25,26,29,30] Moreover, the possibility to reach low power and low voltage consumption depends on the capability to scale down the current technology.

2. CMOS image sensors

CMOS image sensors are mixed-signal circuits containing pixels, analog signal processors, analog-to-digital converters, bias generators, timing generators, digital logic and memory.

2.1. Overall architecture

There are several CMOS imager topologies depending on their purpose. Nevertheless, CMOS imagers architecture can be divided into four main blocks, as Fig. 3 shows.

1. Pixel Array
2. Analog Signal Processors
3. Row and Column Selector
4. Timing and Control

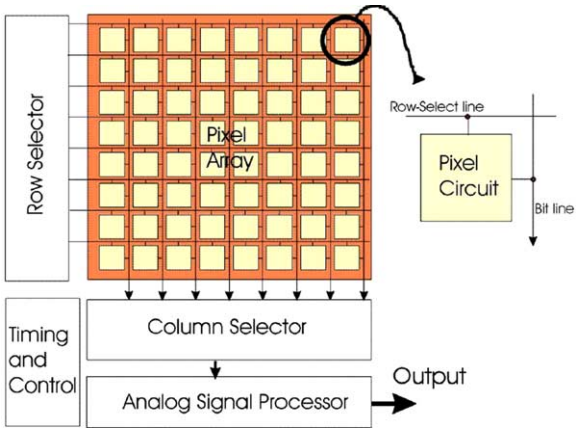

Fig. 3. CMOS image sensor floorplan.

2.2. Pixel circuits

2.2.1. Traditional imagers or photodetectors

1. Photodiodes: Semiconductor devices responsive to high energy particles and photons. They operate by absorption of photons or charged particles and the collected electrons which decrease the voltage across the photodiode in a proportional basis to the incident power. Currently, photodiode CMOS pixels are the most popular ones.
2. Photogates (PG) or CID (Charge-injection device): Semiconductor devices that also collect the photon-generated electrons, but only when the photogate is biased to a high potential.
3. CCD (Charge-coupled device): Device architecture based on series and parallel connection of capacitors, which are made using a dedicated semiconductor process.

2.2.2. Pixel circuits

Pixel circuits are mainly divided into active pixels (APS) and passive pixels (PPS). APS are sensors that implement a buffer per pixel. This buffer is as simple as adding a source-follower. Currently, APS are the predominant devices, although in some cases PPS are also used.

2.2.2.1. Passive pixels (PPS). They were the first CMOS imagers. They are based on photodiodes without internal amplification. In these devices each pixel consists of a photodetector (e.g. photodiode), and a transistor in order to connect it to a readout structure (See Fig. 4). Then, after adressing the pixel by opening the row-select transistor (RS), the pixel is reset along the bit line and RS. In spite of the small pixel size capability and a large fill factor, they suffer from low sensitivity and high noise [20] due to the large column's capacitance with respect to the pixel's one.

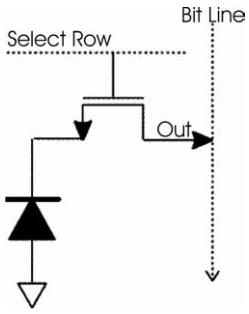

Fig. 4. A photodiode-type PPS schematic.

2.2.2.2. Active pixels (APS). APS are sensors that implement a buffer per pixel. This buffer is a simple source-follower. It is well known that the insertion of a buffer/amplifier into the pixel improves the performance of the pixel. Power dissipation is minimal and, generally, less than CCD's, because each amplifier is only activated during readout. Nevertheless, it must be noted APS technology has some disadvantages: Conventional APS suffer from a high level of *fixed pattern noise* (*FPN*) due to wafer process variations that cause differences in the transistor thresholds and gain characteristics. A solution is to use a *Correlated Double Sampling* (*CDS*) circuit, which can almost eliminate the threshold variations that cause offsets in the video background.

2.2.2.3. Photodiode (PD) type APS. The photodiode-type (PD) APS is considered as standard and it was described by Noble in 1968 [1,20] (See Fig. 5a). It consists of three-transistor: a reset transistor, for resetting the photodiode voltage; and a source follower with select transistor, for buffering the photodiode voltage onto a vertical-column bus. The PD APS is suitable for most mid low-performance applications.

2.2.2.4. Photogate(PG) type APS. It was introduced later than PD APS, in 1993 [1,20] and it employs the principle of operation of CCDs concerning integration transport and readout inside each pixel. Its transfer of charge and correlated double sampling permits a low noise operation. Thus, it is suitable for high performance and low light applications. A typical schematic is shown in Fig. 5c.

2.2.2.5. Logarithmic APS. Non-linear output of the sensor can be desirable. This fact permits an increase on the intra-scene dynamic range. Logarithmic APS are suitable for High Dynamic Range applications, although they suffer from large FPN. Owing to this fact, currently, they are not as used as before. It must be pointed out that they are used a lot in silicon retinas. A typical schematic is shown in the Fig. 5b.

2.2.2.6. CTIA APS pixels. As highlighted before, conventional APS suffer a high level of FPN. Thus, reducing FPN has been a challenge for quite a while and some solutions

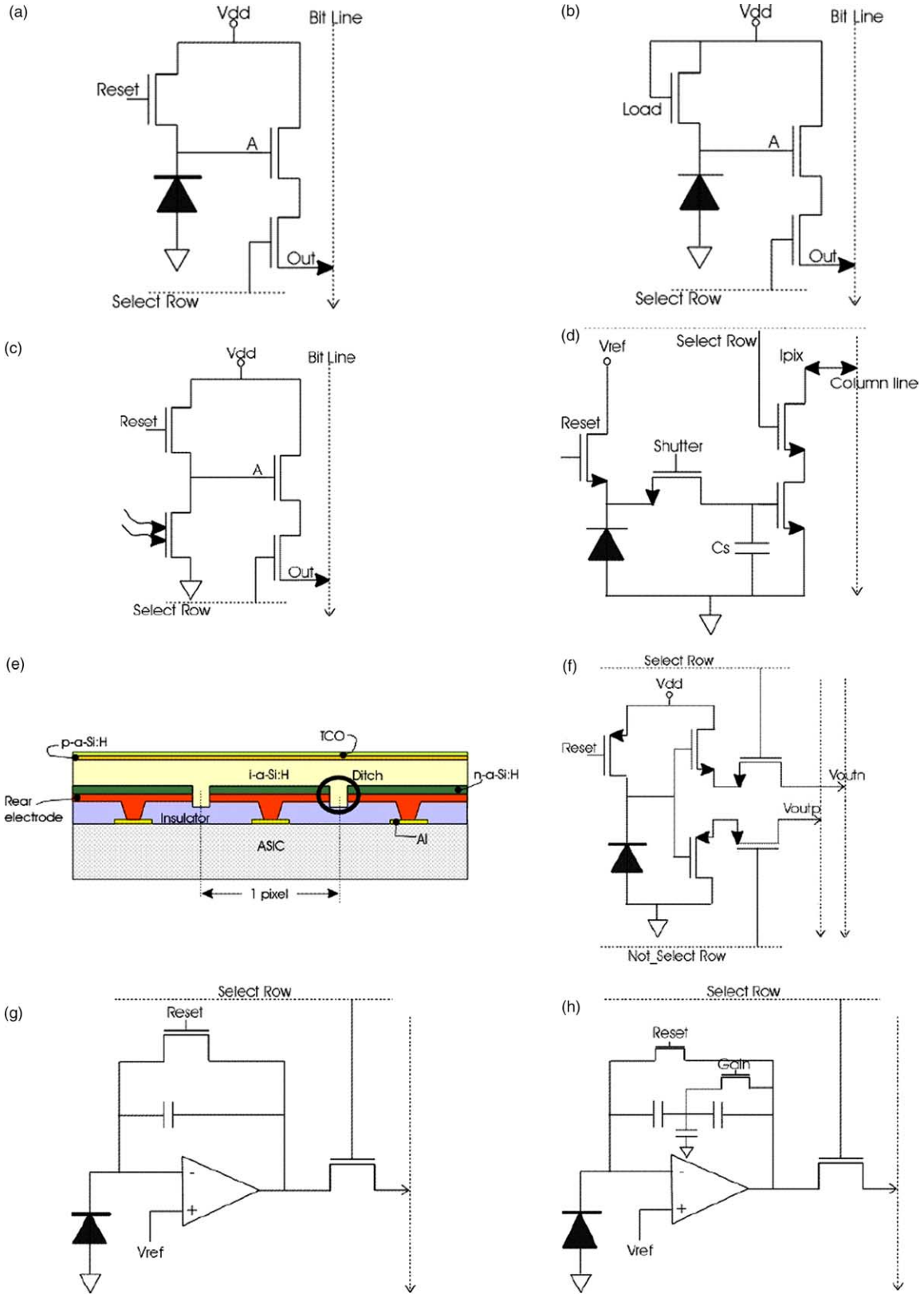

Fig. 5. (a) A photodiode- type APS schematic, (b) A photodiode- type logarithmic APS schematic, (c) A photogate- type APS schematic, (d) Photodiode- type shutter APS schematic, (e) TFA pixel, (f) A photodiode- type CAPS schematic, (g) A photodiode- type Low FPN CTIA APS schematic (h) A photodiode- type High FPN CTIA APS schematic.

have been reported. For instance, capacitive transimpedance amplifier (CTIA) pixels can achieve low FPN [43]. Besides this, the high gain and low read noise are advantages of using CTIAs as well. Fig. 5h and g show a high FPN and a low FPN CTIA APS pixel schematics respectively.

2.2.2.7. Pinned photodiode (PPD) pixel. The pinned photodiode [20], which was previously used in charge-coupled devices, was proposed early during the development of CMOS active-pixel image sensors. Besides lower pixel noise, the pinned photodiode offers reduced dark current. Therefore, they are a PG's alternative, because their architecture offers higher sensitivities than PG.

2.2.2.8. TFA pixels. The thin film on ASIC (TFA) pixels were developed in order to improve sensitivity [20–24]. They consist of an amorphous silicon (a-Si:H) multilayer system that is deposited on top of an ASIC.

Their absorption coefficient for visible light is approximately 20 times bigger than crystalline's silicon (c-Si). In fact, TFA pixels are suitable for High Dynamic Range applications. A typical TFA structure pixel is shown in Fig. 5e.

2.2.2.9. Complementary active pixels sensors CAPS. CAPS are a possible way to manufacture a highly integrated, high performance CMOS image sensor in the deep sub-quarter micron technology. Furthermore, CAPS architecture has low power consumption and a high low-voltage operation capability. A typical schematic is shown in Fig. 5f. The main new features are that the reset transistor is replaced by a PMOS. In addition, a complementary signal path is implemented and the pixel gives out two signal path outputs: V_{outn} and V_{outp} [25–31].

2.2.2.10. Other pixels. There is more pixel architectures [47], due to the huge number of possible applications. For instance, pixel circuits suitable for high speed operation by adding a shutter transistor [44] (see Fig. 5d). Also Diericks (Fillfactory) introduced a novel 100% fill factor pixel.

Overall, PG, PPD and TFA are detector structures to improve the sensitivity. Nevertheless, TFA provides significantly better values than PPD due to the higher fill factor and higher quantum efficiency [20].

2.3. Analog signal processing

Analog signal processing circuits are used in order to improve the performance and functionality of CMOS image sensors. However, they tend to involve less pixel density and increase the chip area due to the added functions. Some research has been done to overcome these problems [48].

Firstly, there are some well known traditional signal processing systems. For instance, additional analog-signal-processing circuitry located at the periphery of the array permits the suppression of both, temporal and fixed-pattern noise. As an example, *Correlated Double Sampling* (*CDS*) *or Double Differencing Sampling* (*DDS*) suppress FPN [49, 43,50,51]. Others achieve high *SNR* [52] and ADC for camera-on-a-chip. Secondly, there are also several signal processing systems depending on the application. For instance, signal processing such as K-winners-take-all, are suitable for 3D vision systems [53–58] and subpixel accuracy [59–65]. Smoothing [66], motion detection [67–69], programmable amplification, multiresolution imaging [70], video compression [71], dynamic range enhancement, discrete cosine transform (DCT), intensity sorting, etc. are other signal processing systems.

2.4. Readout methods

Readout methods have an important influence in the sensor performance. Thus, there are several readout methods depending on the desirable application. The main requirements are:

1. low power dissipation
2. high resolution
3. good linearity
4. stable detector bias
5. low noise
6. high injection efficiency
7. small pixel size
8. good dynamic range

APS readout structures fulfil 4 and 8 requirements, but not 3 and 7. On the other hand PPS readout structure fulfils 7 and not 3, 4, 6 and 8. Finally, share-buffered direct-injection (SBDI) [72] readout structure combine both imagers characteristics.

Therefore, it is possible to find suitable traditional readout methods for low FPN [73–76], for high frame rates [73], to increase linearity and DR [72], with high SNR and ultrahigh- sensitivity [77,78] and for infrared detectors [79]. Finally, there are also specialised readout methods suitable for ultra high sensitivity, for focal plane array, for X-ray imaging, for an emission-transmission medical imaging systems, for low-light levels, detectors with self-triggered readout, offset-free column readout circuit and transversal-readout architecture

2.5. Noise sources

CMOS Image sensors suffer from several noise sources. They set the fundamental limits on image sensor performance, especially under low illumination and in video applications. Therefore it is important to have an overview of all of them [80].

The noise sources in CMOS imagers can be divided into *Temporal Noise* [81] and *Fixed Pattern Noise* (*FPN*)[43].

2.5.1. Temporal noise

It can be divided into different kinds of noise, depending on its source:

- Pixel noise: photon shot noise, reset or kT/C noise (which is the thermal noise resulting from resetting after each pixel's readout. The k is Boltzmann's constant, T is the absolute temperature; and C is the junction parasitic capacitance), dark current shot noise and MOS device noise (thermal, $1/f$ or flicker, etc.)
- Column Amplifier noise
- Programmable gain amplifier noise
- ADC noise
- Overall temporal noise, noise floor or reading noise.

2.5.2. Fixed pattern noise (FPN)

It has been a huge CMOS imagers' limitation. FPN is the fixed variation in the output between pixels when a uniform input is applied. In a perfect image sensor, each pixel should have the same output provided that the same input is applied, but in current image sensors the output of each sensor is different. FPN does not change as a function of time and can be characterized, assuming a linear pixel response, as a variation in the offset and gain at each pixel.

$$Vij(t) = GijXij(t) + Oi,j$$

V	output,
G	gain of pixel,
X	input,
O	offset of pixel,
Gain FPN	pixel to pixel variation of Gij,
Offset FPN	pixel to pixel variation of Oij.

3. Latest developments in the field of CMOS imagers

The research has been mainly focused on APS in areas like Low noise, High dynamic range, High sensitivity and High fill factor, Low power consumption, Low voltage operation, High speed imaging. To remark is that all these features are difficult to achieve in one design. Hence, depending on the application, one feature will have more priority than another one.

3.1. High dynamic range (DR)

The ratio of the saturation signal to the rms noise floor of the sensor is known as dynamic range. This is limited by the *photosensitive-area size, integration time and noise floor*, which is the noise generated in the pixel and the signal processing electronics. DR is limited by the *integration time*, although high dynamic range image readout can be achieved by using different exposure or integration times [82]. Secondly, with respect to the *noise floor* the use of a linear readout is more suitable than a logarithmic one. So Dynamic Range of CMOS APS is strongly managed by the readout method. Finally, the *photosensitive-area size* is an important issue because of the well-known scaling effects.

The major problem of artificial image acquisition has been the extraordinary high optical dynamic range of natural scenes. For instance, the human vision system exhibits an enormous optical dynamic range of about 200 dB, due to the fact that it can adapt to an extremely high range of light intensity levels [83]. Nevertheless, artificial imagers have been much poorer in this aspect. With conventional CCD sensors it is hard to reach high dynamic range and CMOS imagers with logarithmic response suffer from excessive FPN and temperature drift. For instance, in year 2000 the conventional CCD imagers exhibited usually a DR of about 50–70 dB only and on the other hand, CMOS imagers would achieve better DR, up to 140 dB, than CCDs [82], although they used logarithmic readout, which has some disadvantages such as a high FPN.

In fact, some research has been done to obtain CMOS image sensors with high dynamic range:

3.1.1. Logarithmic

The use CMOS imagers with logarithmic readout or the non-linear output of the logarithmic pixel provides higher dynamic range (see Fig. 6). Nevertheless, logarithmic response has a large FPN and slower response time for low light levels, which bring down the image quality. Thus, some systems based on logarithmic response have been developed in order to offer high DR with low FPN. For instance, in 1998, the University of Heidelberg proposed a CMOS camera chip with logarithmic response and self-calibrating FPN correction [84]. Its results showed a significant FPN reduction. Fraunhofer Institute of Microelectronic Circuits and Systems of Duisburg suggested also a CMOS imager with Local Brightness adaptation [85]. It used logarithmic image sensors in order to reach high DR and FPN was also compensated. In year 2000, S. Kavadias reported a technique to remove the high FPN, due to its logarithmic response [86]. This CMOS image sensor, which

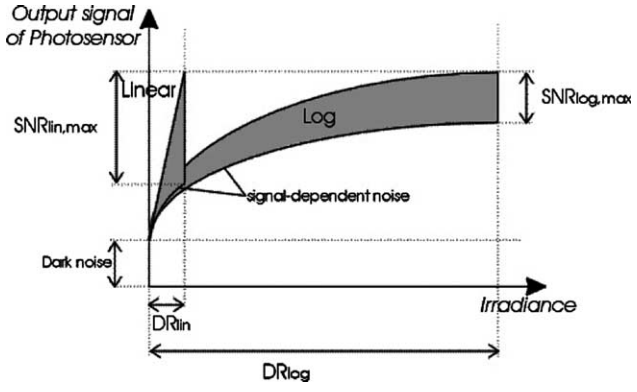

Fig. 6. Photoconversion characteristics: linear vs logarithmic.

was based on an active pixel structure, employed on-chip calibration and achieved a DR of 120 dB and the FPN was 2,5% of the output signal range. Finally in year 2003 a multiresolution scheme and a cost-effective architecture for nonlinear analog-to-digital conversion was presented. These two features combined together improve the sensors quality under low light intensity [87].

3.1.2. Linear

On the other hand, using CMOS imagers with linear readout can improve FPN, even though they can achieve lower DR (see Fig. 6) than logarithmic ones. For instance, in 1999 a new design, a 1280×1024 digital CMOS image sensor with enhanced dynamic range, was reported [51]. The response was linear, low FPN was achieved and DR was of 69 dB. In year 2000 a CMOS image sensor for automotive applications was proposed [83]. It offered a high dynamic range up to 120 dB and an excellent image quality due to its linear readout. Furthermore, it had good temperature behavior up to 85 °C. In year 2002 a high dynamic CMOS imager with spiking pixels, pixel-level ADC, and linear characteristics was reported [88]. It had a DR of 93 dB, although 120 dB was expected. Finally, it is reported of a mechanism [82], using linear readout, capable for adjusting its sensitivity depending on the absolute illumination level, like human vision. This is reached by using different integration times. The results demonstrate that with 1 integration time, a DR of 61 dB is reached. In contrast, with two integration times, the DR is of 92 dB.

3.1.3. Combined

In 1998, the University of Waterloo reported a CMOS APS with combined linear and logarithmic mode operation [89]. The results showed that it had good linearity, in the linear mode operation, and it reached wide dynamic range in the logarithmic mode.

So the issue is to determine which is the more convenient readout method in each application. Nevertheless, using linear readout methods with different integration times seems to be more suitable.

3.1.4. TFA technology

As outlined before, TFA technology [23,24] is suitable for achieving a high dynamic range and a high fill factor. In 1999–2000, T. Lulé reported a 100.000 pixel imager in TFA technology [21,22]. The main feature was that every pixel contained an automatic shutter, which adapted the integration time to the local intensity. This allowed obtaining a high DR of 120 dB.

3.2. High sensitivity (High fill-factor (FF) and high quantum efficiency)

3.2.1. Background

The basic quality criterion for pixel *sensitivity* is the product of its *Fill Factor* and its *Quantum Efficiency* (FF×QE). Where *Fill Factor* is the ratio of light-sensitive area to the pixel's total size; also known as aperture efficiency, and *Quantum efficiency* is the ratio of photon-generated electrons that the pixel captures to the photons incident on the pixel area. Photons are lost for conversion due to: reflection on dielectrics, no absorption in the acquisition layer and loss of charges and recombination.

It is well known that a good image quality is obtained if most of the chip area is dedicated to the photodetectors. Therefore in order to achieve a good image quality, a high Fill Factor (FF) is needed. Unlike CCDs, which achieve around 100% FF [90,91], CMOS APS FF are limited, because each pixel has an area devoted to the CMOS readout circuitry. Around 30% FF is a kind of standard. In CMOS APS pixel, the Fill Factor is limited by: (a) shadowing by metals or silicides, (b) collection of photons by the insensitive junctions of the active pixel, (c) the relatively small size of the useful photo-sensitive junction, (d) recombination of photo-generated carriers with majority carriers, limiting the diffusion length. Besides this, a high fill factor allows shorter exposure times for a given pixel size or smaller pixel sizes for a given sensitive area. Thus, FF plays an important role in the scaling perspectives and imager's performance.

In the wake of that, a lot of research has been done to increase the fill factor of CMOS APS. There are different methods used to improve the FF: one is to design active pixels with larger photodiodes, although small pixels can not be made and large photodiodes have low charge conversion sensitivity due to their higher capacitance [92]. The other method is to make passive pixels, but their performance with respect to active pixels is worse. On the other hand, microlenses, which help funneling photons to the light-sensitive portion of the pixel [93,1], are another alternative to overcome this problem. They could reach up to 90% Fill Factor. In spite of this 90% Fill Factor, they have some disadvantages such as the reduction of efficiency as microlens dimension decreases. In fact, some high fill-factor designs based on CMOS APS exist, which can enhance the FF: A. Bermak developed a 46% Fill Factor native logarithmic pixel [94] in 0.7 μm CMOS technology in 2000. In 2002, the Georgia Institute of Technology achieved a fill factor greater than 40% by using a matrix transform imager [95] Also in 2002, National Tsing-Hua University described an APS, with a fill factor of 55%, made in 0.25 μm technology [96]. In addition, this device has a high DR of 120 dB, thanks to its innovative tuneable injection current compensation architecture and a voltage operation of 1.9 V.

Finally, it is important to consider the downscaling effects, because small pixels mean lower light sensivity and dynamic range. Thus, conventional APS technology is limited. Nevertheless innovative architectures, ideas and technologies reaching a fill factor up to 90–100% have appeared: For instance, in 1997 Dierickx [97,98] introduced a near 100% Fill Factor CMOS active pixel, which was

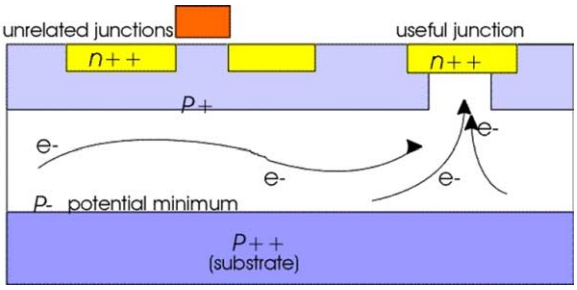

Fig. 7. Cross-section of Fill Factory's well pixel.

patented by FillFactory as High Fill Factor N-Well Pixel® (US Patent 6,225,670).

Photoelectrons are channeled by electrostatic barriers shielding them off the active pixel circuitry and substrate (see Fig. 7 left side), to the photodiode junction (see Fig. 7 right side). Virtually, all electrons diffuse down this drain, and as the diffusion time is short (typically 10–50 ns) negative effects like image lag must not be feared.

In addition, TFA Imagers [20–24] offer 100% FF. The photodiode is placed on top of the ASIC. So the whole pixel area is available for the photodiode and there are no further layers obstructing the light penetration such as further metallization, polysilicon or dielectrics.

Increasing the photosensitivity of the photodetector is another thing to be taken into account in order to improve the quantum efficiency. M. Furumiya [99] reported in 2001 a high photosensitivity and no-crosstalk pixel technology for an APS by using a 0.35 μm CMOS technology. A deep p-well photodiode, with a sensitivity improvement of 110% for 550 nm incident light, and an antireflective film to increase photosensitivity, consisting of Si_3N_4 film, with a sensitivity improvement of 24% are used. Finally, it is possible to increase the sensitivity by the cascoding method, which allows shielding of the integrating capacitor from the parasitic junction capacitance of the photodiode. This can be done with shutter APS [44] or CTIA pixel [43].

3.3. High performance (low power consumption and low voltage operation)

One of the most important advantages of CMOS image sensors compared to CCDs is the lower power consumption. Therefore, CMOS image sensors are suitable for portable applications [31,100,101], among which, cellular phones, portable digital assistants (PDAs), and wireless security systems, etc.

A lot of research has been carried out on this topic. Low power camera-on-a-chip using CMOS APS technology began to be developed in 1995 by NASA at the Jet Propulsion Laboratory [102,103] and in 1998, the first CMOS APS fabricated using a high performance 1.8 V, 0.25 μm technology was introduced by Hon-Sum Philip Wong [104]. In that paper, the impact of the device scaling was studied, because no process modifications were made to the CMOS logic technology. In 1999, a CMOS imager with a power consumption of 250 mW [105] with an acquisition rate of 60 frames/s and a resolution of 1280×720 pixels was reported. This has been useful for large-format high-speed imaging applications such as industrial vision systems. In 2000, a 1.2 V micropower CMOS Active Pixel Image Sensor for portable applications was proposed [106]. In 2001, a low voltage hybrid Bulk/SOI CMOS APS was manufactured [107]. Also, in 2001, Nara Institute of Science and Technology reported a CMOS pixel circuit based on a pulse frequency modulation (PFM) technique [108]. This device reached a quite good performance (DR over 50 dB) under very low operation voltage, less than 1 V, and was very robust against noise due to its A/D converter. In 2003, a 176×144 CMOS APS with micropower consumption [109,110] was reported, with a voltage operation of 1.5 V and power consumption of 550 μW. Thus, this amount enables the sensor to run using a watch battery.

Other novel designs have been introduced, like a CMOS imager with motion vector estimator for low power image compression [111], which was designed by Toyohashi University of Technology in 1999.

Someone states that APS will not function at 1.2 V or below [28]. However, CAPS [25,26,29,30] offer to work with a low voltage of 1 V or less using advanced technologies. They claim to obtain good performances [25,26,28–30]. Unlike APS, it must be stressed that CAPS are an alternative architecture which can be manufactured using top level technologies, below 0.25 μm, with great performance (see device scaling considerations). Thus, Low Voltage systems expect to continue downscaling by using CAPS, as an alternative to conventional APS.

3.4. High speed imaging

Acquiring high-speed images is becoming more and more important in some areas such as real time applications. Nevertheless CCD technology did not make enough progress in this aspect. During more than 3 decades CCDs have been developed and after spending millions of dollars, they reached 250 kilo-pixels with an acquisition speed of 1000 frames per second [19]. Comparatively, high speed CMOS sensor technology is just started, because the first high-speed sensors were introduced around 1998 [112,113] and they have reached already great results. In addition, high frame rates have been possible thanks to the CMOS downscaling. In conclusion, CMOS imagers appear to be a promising alternative to CCDs taken also into account other advantages such as less *Blooming* and *Smearing effects*.

3.4.1. Needs and problem solving

A typical CMOS APS contains three NMOS transistors in each pixel only. Therefore, a very compact implementation is possible although the sensor lacks of image data parallel acquisition, a feature often important in high-speed imaging. The alternative is a pixel that contains an analog

memory called SNAP (Shuttered-Node Active Pixel). Another important issue is how the data is multiplexed into the output pads. Multiplexing of digital data is much simpler than passing off analog data, so ADC are needed. Another architectural feature that allows high-speed operation is pipelining [19].

A CMOS image sensor needs to fulfill all the necessary requirements in order to provide fast image acquision. No *smear*, no *blooming* and global electronic shutter are some of the most valuable characteristics needed [114]. In addition, low lag and snap-shot mode are preferable. Low lag is essential in order to capture rapidly changing scenes. The rolling shutter method is very common in CMOS imagers where the rows of pixels in the image sensor are sequentially reset, starting at the top of the image and proceeding row by row till the bottom. When this reset process has moved some distance down the image, the readout process begins: rows of pixels are read out sequentially as well, starting at the top of the image and proceeding row by row till the bottom in exactly the same fashion and at the same speed as the reset process. So, this device is not appropriate at high frame rates, because the scene can significantly change during the frame reading time. Therefore, a non-rolling shutter or snap-shot mode is necessary [115]. It is also necessary to acquire images in a very short time and using short integration times. This requires the image sensors to be equipped with synchronous shutter in order to avoid *blur* (see Fig. 8). For instance, images acquisition of fast-moving objects requires imagers with high photoresponsivity at short integration times, synchronous exposure, and high-speed parallel readout [116].

3.4.2. Manufactured imagers

Several designs have been reported since 1997. In 1998, a 128×128 snap-shot photogate CMOS imager in 0.5 μm technology was implemented by Guang Yang [113]. It offered high speed (400 fps) and minimum exposure time 75 μm. It reproduces high quality, motion artifact-free images at high shutter-speeds (<75 μm exposure), with low noise, unmeasurable image lag and excellent blooming protection.

Between 1998 and 2000, N. Stevanovic and M. Hillebrand [6,116,117,114] reported a high speed

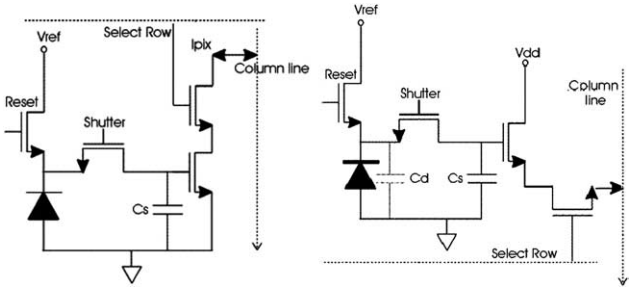

Fig. 8. Photodiode-type shutter APS schematics.

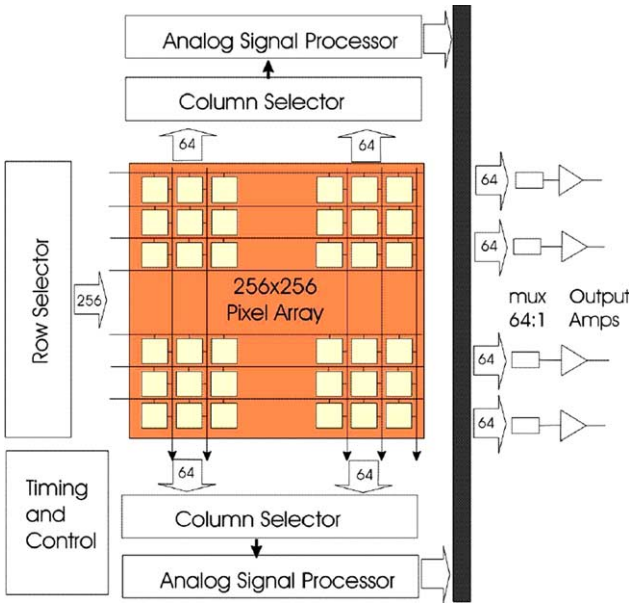

Fig. 9. Architecture of the high speed CMOS imager.

CMOS camera (see Fig. 9). It was able to acquire more than 1000 frame/s using a global shutter in each sensor cell. The integration time in synchronous exposure was variable between 1 μs and 150 instead of previous CMOS implementations, which had around 500 frames/s at integration times ranging from 75 to 200 μm [42,113,112]. So it offered a compact, portable, and low power (320 mW) solution for high speed video systems and had a resolution of 256×256 pixels.

DALSA Inc. Waterloo reported a VGA CMOS imager [115] in 2001, which can capture images at 1600 frames per second (see Fig. 10). Furthermore, it has exposure control functionality, antiblooming capability and a non-rolling shutter architecture to implement snap-shot image capture mode.

Also in 2001, S. Yoshimura, T. Sugiyama, K. Yonemoto and K. Ueda reported a 48 kframe/s CMOS Image sensor for

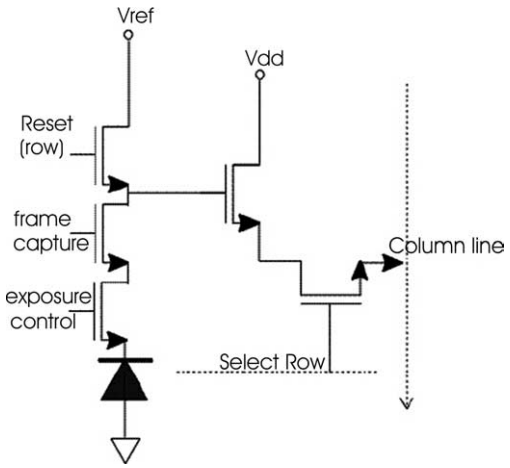

Fig. 10. Pixel of a DALSA VGA CMOS imager.

Real-time 3D Sensing and Motion Detection [118]. It had an array of 192×124 pixels, depth resolution of 500 μm, fast motion detection and 12b digital image output resolution.

E. Fossum and A. Krymski introduced first a 1280×720 pixel at 60 fps (60 Mpixel/s), then reported a 1024×1024 pixel at 500 fps (500 Mpixel/s). They continued enhancing their design, when in 2003 they presented [119] a high speed, 240 fps, 4.1 Mpixel(2352×1728) CMOS sensor (> 800 Mpixels/s) with on-chip parallel 10-b analog-to-digital converters (ADCs) and power dissipation of less than 700 mW. Besides this, in 2003, a High-responsivity 9-V/Lux-s, high speed 5000 fps at full 512×512 resolution CMOS sensor was manufactured [44]. The sensor was designed for a 0.35 μm process and consisted of a five transistor pixel to provide a true parallel shutter.

3.4.3. High speed market

High speed imaging systems are suitable for *automotive* applications such as occupancy detection, precrash sensing, collision avoidance, surveillance, crash test observation, or airbag control. For instance, a smart airbag solution based on a high speed camera system was designed by Fraunhofer Institute of Microelectronic Circuits and Systems [120]. The system continuously monitors the seats and quickly determines the occupancy status and passenger's position and size before the airbag is blasted. Another application is smart image sensor for *real-time*. For instance Yosuke Oike reported in 2003 a smart image sensor for real-time and high-resolution 3D measurement [121]. It does not only have enough high frame rate for real-time 3D measurement, but also high pixel resolution owing to a small pixel circuit and high subpixel accuracy due to gravity center calculation using a light intensity profile measurement trick. Finally, an application for high-speed video systems, for fast moving objects or for machinery vision is also suitable.

3.5. Low noise sensors

CMOS Image sensors suffer from several noise sources. These set the fundamental limits on image sensor performance, especially under low illumination and in video applications. Therefore, it is important to have an overview of all of them [80]. The noise sources in CMOS Imagers can be divided in Temporal Noise [81] and Fixed Pattern Noise (FPN) [43].

In fact, FPN is one of the major CMOS imager's disadvantages. Thus, a lot of research has been done in order to minimise FPN.

Many researchers have designed FPN-reduction circuits. For instance, *Correlated Double Sampling* (*CDS*) is one of the most suitable for suppressing FPN [50,76]. Fig. 11 shows a typical schematic of a CDS circuit. CDS technique consists of taking two samples from a signal, which are closely spaced in time. Then, the first signal is substratcted from the second one, hence, removing the low-frequency noise. Sampling occurs twice: first after reset and last after integrating the signal charge. The subtraction removes the reset noise and dc offset from the signal charge. The two values are then used as differential signals in further stages like programmable gain amplifiers (PGA) or ADC. Most of them are placed below each column of pixels (see Fig. 12a). However, CDS reduces the fixed pattern noise to a large extent, a component of the FPN due to mismatch in the CDS circuits at each column introduces column-FPN, which should be also removed. For instance, K. Yonemoto and H. Sumi proposed [50] that FPN reduction should be performed in a CDS circuit (see Fig. 12b), in order to avoid this column-FPN caused by CDS circuits. On the other hand, although the dark current variation of photodiodes appears as FPN in the output signal of a CMOS image sensor, which resembles FPN caused by threshold variation of transistors in pixel circuits, the dark current noise cannot be suppressed with CDS circuits. This is because the dark current does not appear in the reset level, but only in the signal level of the pixel signal. Therefore, the dark current of the photodiode itself should be reduced.

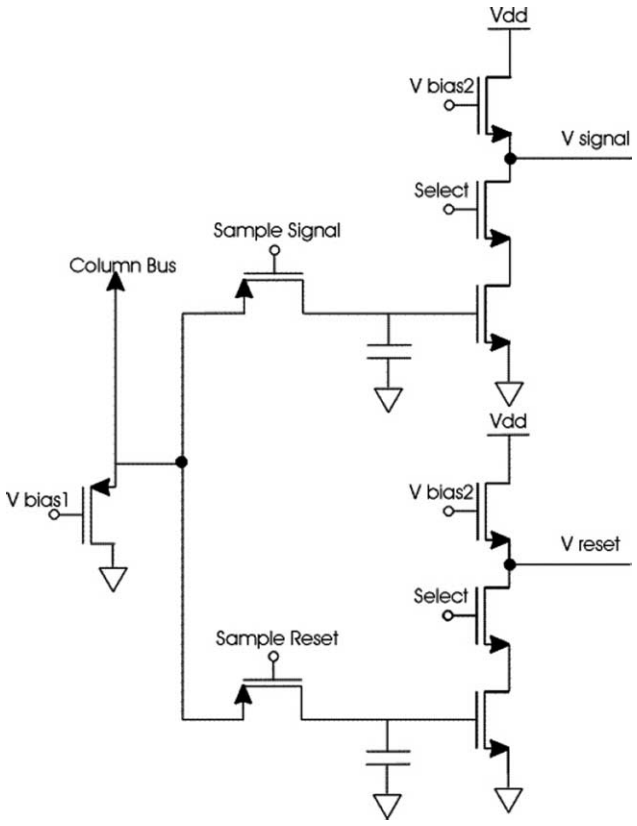

Fig. 11. Schematic diagram of the correlated double sampling circuit. There is one such circuit for every column.

One way of reducing the dark current is to employ a pinned photodiode [122]. Another method reported by K. Yonemoto and H. Sumi in 2000 is a pinned photodiode, in the form of hole accumulation diode (HAD) [50]. They achieved a reduction of the dark current to 150 pA/cm^2 instead of 6 nA/cm^2 of a pn-photodiode. As a result, the dark

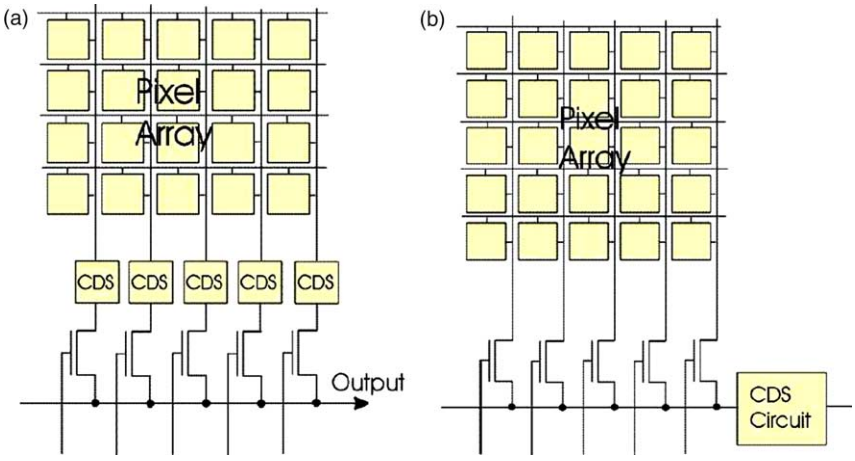

Fig. 12. (a) CMOS image sensor with column CDS circuit, (b) CMOS image sensor with proposed FPN-reduction scheme.

current variation at the output of the CMOS image sensor was 0.19 mV and the period of readout operation was about 20 ns at 30 frames/s. Two years later, K. Yonemoto and H. Sumi carried out [49] a numerical analysis of this CMOS Image sensor with a simple FPN reduction technology. They showed that the low-input-voltage I–V converter with a current-mirror circuit improves the amplification factor and linearity of the pixel circuit. In a five-transistor pixel circuit, the threshold voltage of the X–Y addressing transistor affects the amplitude and the level of the readout pulse. An analysis of the mechanism of the X–Y addressing transistor showed the basic concept behind the selection of the threshold voltage. An L-shaped readout gate for a pinned photodiode was compared with a straight readout gate, and was proved to be adequate for rapid charge transfer.

Another circuit to suppress FPN peak-to-peak to 0.15% of saturation level is *Delta-difference sampling* (*DDS*) [123].

On the other hand, B. Fowler [43] proposed a new APS, called Capacitive Transimpedance Amplifier (CTIA). *CTIA APS* that can achieve low FPN by using a divider circuit with switched capacitor voltage feedback. Besides this, the high gain and low read noise are advantages of using a CTIA as well (See Fig. 5h and g).

Moreover, other *readout methods* can also offer an improvement in order to suppress FPN. For instance, R&D Headquarters from Minolta Co. and Gazoh System Kaihatsu reported a CMOS APS with transversal readout architecture that eliminates the vertically striped FPN [73,75]. The possibility of high frame rate using a multiport structure was also demonstrated. In addition, the Photonics and Sensors Group of the Cambridge University suggested, in 2002 [74], a new readout circuit for a CMOS APS, which removes the FPN and reduces signal degradation while offering an increase in readout speed compared to the conventional approach.

As outlined before, CDS can not suppress the *dark current noise*, although it is a FPN's source. Thus, decreasing the dark current to suppress FPN has been an aim. Dark current (offset error) is the signal charge that the pixel collects in the absence of light divided by the integration time. Dark current is temperature-sensitive and typically normalised by area. Photobit Technology Corporation and Tokyo institute of Technology reported a low dark current stacked CMOS APS for charged particle detection [124,125]. A use of a p-MOSFET transistor for readout reduces the hot carrier effect; thereby the dark current within the low temperature region is greatly decreased. It also improves noise reading performance due to its lower flicker noise compared to n-MOSFETs'.

Thanks to the improvement of the noise performance, CMOS Image Sensors for *Low light level applications* are possible [18]. In 2000, a CDS noise analysis of readout circuits used in CMOS APS for low light levels was carried out [17]. In 2001, different pixel architectures were studied in order to increase the sensitivity and reduce the spatial (FPN) and temporal noise [16]. This study demonstrates that the N-well photodiode is the best light sensor, either for its parasitic capacitance value, for its quantum efficiency, or for its dark current. However, the design rules required by this photodiode (a wide space must be kept between N well and MOS transistors) limit their use in CMOS imagers. On the other hand, a new pixel architecture was also introduced. This architecture reduces kTC or reset noise and FPN. Therefore, this architecture is ideal for applications requiring very high sensitivity and low noise, which is necessary for low light level sensing.

Complete reset of the photodiode is needed in order to remove *kTC or reset noise* and decrease the *lag effect*. Note that the source of image lag in CMOS imagers is different from the source of image lag in CCDs. In CCDs, image lag is caused by incomplete charge transfer. This can be eliminated using a pinned photodiode. On the other hand, CMOS *image lag* is due to incomplete reset so, in 2001, H. Tian [81] reported a new reset method, which alleviates the lag without increasing the reset noise. The reset transistor gate is overdriven.

Finally, CMOS APS still has readout-noise problems because of irregular gain from mismatched transistor thresholds.

4. Applications

As highlighted before, improvement of CMOS image sensors has opened up new application areas [45]. Therefore, CMOS imagers are very suitable for Space, Automotive, Medical, Digital photography and 3D applications. Furthermore, there are more specific applications such as portable devices [100,101,31], security, industrial vision [126,127], consumer electronics, imaging phones, astronomy, surveillance [128], robotics and machine vision, guidance and navigation (e.g., stereovision [129]), computer inputs, etc.

4.1. Space applications

CMOS Imagers are widely used in the space environment for a varied range of applications [130,131]. These applications include robotic and navigation cameras, imagers for astronomy and earth observation, star trackers [132], tracking sensors in satellite constellations, lander and rover imagers, X-ray satellite missions [133,134], etc. Moreover, CMOS imagers are known to be tolerant to radiation, although true radiation tolerance can only be obtained using specific methods. Thus, there is a huge interest in radiation-tolerant imaging systems [32–39,135,136]

4.2. Automotive applications

There are a lot of applications [137] in the automotive field like occupancy detection, airbag control, precrash sensing, collision avoidance, surveillance, crash test observation, etc. Another one is a smart airbag solution based on a high speed camera system [120]. This system continuously monitors the seats and quickly determines the occupancy status and passenger's position and size before the airbag is blasted. Moreover, IR-vision systems for foggy and night driving conditions are also addressable.

4.3. Medical applications

Medical or Biomedical systems based on CMOS imagers have been successfully developed [138]. For instance, Microelectronic components for a retina-implant system that will provide visual sensations to patients suffering from photoreceptor degeneration was reported by M. Schwarz in 1999 [139]. On the other hand, the digitisation of medical images, especially in radiology, has been another demand in recent years. Ho Kyung Kim proposed an X-ray imaging system with large FOV (field-of-view) using CMOS image sensors [140]. S. Wook Lee reported a 3-D Xray microtomographic system [141] in 2001. It makes possible to see the internal structure of small objects in a non-destructive way. Finally, P. Lechner developed an APS for X-ray imaging Spectroscopy in 2001 [142].

4.4. Digital photography

A CMOS image sensor integrating the sensor itself and the digital control functions on a single chip was reported [1]. This demonstrates the viability of producing a camera-on-a-chip suitable for commercial and scientific applications [143,144]. Besides, cameras with nearly noise-free pictures [145] and low power consumption have been developed. In 1998, Toshiba Corp. reported a 3.7×3.7 μm^2 square pixel CMOS image sensor [146] for Digital Still Camera applications with high performance.

4.4.1. 3D range imaging applications

3D range imaging systems are more and more required due to the fact that 3D images acquisition is important in various sectors such as home, public and industrial domains. Furthermore, improvements in speed and resolution performance have opened up the possibility to obtain *real time* systems.3D *range imaging system*, also called 3D digitiser or Range finder, is a system capable to acquire range or depth information. These devices grab 'range images' or ' images', which are dense arrays of values related to the distance of the scene to a known point or plane [147]. Currently, there are some special 3D *measurement methods* available for scene reconstruction. These techniques rely on *triangulation* (see Fig. 13), *time-of-flight* (*TOF*) measurements or *interferometry*, etc. [148] The range of possible applications is wide. For instance, obtaining 3D Models from Range Scans [149], Space monitoring and surveillance [118], safety and security [148,120], Real time Sensing and Motion detection [118], Inspection [150], 3D X-ray imaging [141], Robot vision [151], etc.

4.5. Other applications

There are more suitable applications, such as portable applications [100,101,31], security, industrial vision (e.g., Imager with focal plane edge detection [127]), consumer electronics, surveillance devices [128], Smart vision system on-a-chip [143,144,129,152], Robotics and machine vision,

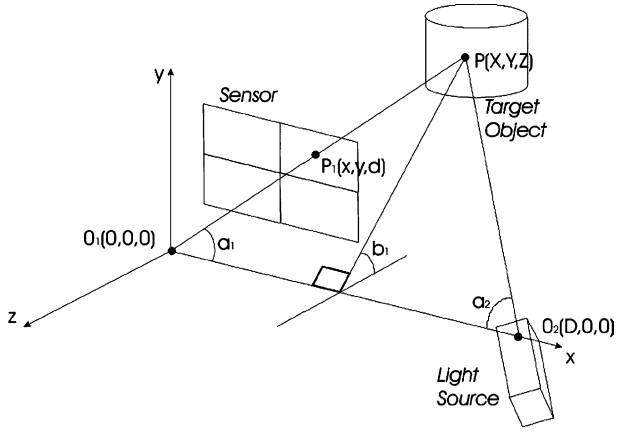

Fig. 13. 3D measurement system based on triangulation.

guidance and navigation (e.g., stereovision [129]), video phones, computer inputs, for charged particle imaging [124, 125] such as ion and electron imaging, IR-vision applications, low light level applications [16–18], electrostatic sensing, instrumentation, imaging phones, astronomy and low-end professional cameras.

5. Conclusions

A review of the most important advances in the field of CMOS image sensors has been carried out. These advantages have been mainly focused on fields such as sensitivity, low noise, low power consumption, low voltage operation, high-speed imaging and good dynamic range. This paper demonstrates that CMOS imagers are competitive with CCDs in many application areas, such as security, consumer digital cameras, automotive, computer video, imaging phones, etc. CMOS imagers will replace CCD devices in some cases, because of its low cost, low power consumption, integration capability, etc. Nevertheless, CCD technology will continue as predominant in high performance systems, such as medical imaging, astronomy, low-end professional cameras, etc. because of its better image quality. To sum up, State-of-the-art of CMOS image sensors has been provided.

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